**Purpose:**

Create a stop-watch module in Verilog that runs on the Nexys A7 development board.

**Scope:**

A stop-watch that runs from 0:00:00 to 9:59:99 formatted as M:ss:mm (M: minute, s: second, m: milli-second) , with one button to reset and one button to stop/start count.

**General Requirements:**

**Trigger Detection Circuit**

**1 Second Timer**

**12 Bit Up Counter**

**7-Segment Display**

1. The module shall have a 24-bit Binary-Coded-Decimal count input ‘i\_count’.
2. The module shall have five 8-bit output vectors representing each digit in the 7-segment display: ‘o\_segout1’ – ‘o\_segout6’.
3. Every four bits of the input shall represent a decimal digit in binary to be displayed on the 7-segment display.
4. The minimum decimal value every digit (4 bits) shall take is 0.
5. The maximum decimal value every digit (4 bits) shall take is 9.
6. The module shall convert every 4 bits of the 24-bit input signal to the corresponding 7-segment code to light the segments appropriately according to the FPGA datasheet.
7. The output signals shall be continually driven according to the input signal.
8. Each one of the outputs shall represent one digit to be displayed on the 7-segment display.

**7-Segment Adapter**

1. The module shall have a system clock input ‘i\_sclk’.
2. The module shall have an active low reset input ‘i\_reset\_n’.
3. The module shall implement an asynchronous reset.
4. When the ‘i\_reset\_n’ is set to 0, ‘o\_segments’ shall be set to 00000000.
5. When the ‘i\_reset\_n’ is set to 0, ‘o\_digits’ shall be set to 00000000.
6. The module shall have six 8-bit digit code inputs: ‘i\_segout1’ – ‘i\_segout6’ that represent each digit to be displayed.
7. The module shall have an 8-bit output to control the anodes of the 7-segment display segments ‘o\_segments’.
8. The module shall have an 8-bit output to control the cathodes of the 7-segment display digits ‘o\_digits’.
9. The module shall cycle through connecting the 8-bit inputs to the 8-bit output ‘o\_segments’.
10. Each input shall be connected to the output ‘o\_segments’ for a period of 1 millisecond.
11. The module shall set the bit corresponding to the input to be displayed in ‘o\_digits’ to 0 and all the rest of the bits to 1.
12. Total period of every cycle shall be 6 milliseconds.

**Traceability:**