General Requirements (Tag prefix: RTC)

1. Asynchronous, low active reset (Tag: RTC\_RESET)
   1. [RTC\_RESET\_01] The top-level input signal reset\_n shall be mapped to the internal signal i\_resetn.
   2. [RTC\_RESET\_02] All modules shall reset to their initial values on the negative edge of i\_reset\_n.
2. Positive edge clocking (Tag: RTC\_CLK)
   1. [RTC\_CLK\_01] The top-level input signal sys\_clk shall be mapped to the internal signal i\_sclk.
   2. [RTC\_CLK\_02] All synchronous operations shall be done on the positive edge of sys\_clk.

**Trigger Detection Circuit**

**1 Second Timer**

24-Bit BCD Up Counter (Tag prefix: COUNTER)

1. Top Level Wrapper (Tag: COUNTER\_TOP)
   1. Top level module sends the individual BCD digits to a single bus output.
      1. [COUNTER\_TOP\_01] The module shall instantiate six 4-bit counter submodules corresponding to each displayed digit.
      2. [COUNTER\_TOP\_02] o\_count (3:0) shall be set when the corresponding bits from o\_bcdcount0 are set.
      3. [COUNTER\_TOP\_03] o\_count (7:4) shall be set when the corresponding bits from o\_bcdcount1 are set.
      4. [COUNTER\_TOP\_04] o\_count (11:8) shall be set when the corresponding bits from o\_bcdcount2 are set.
      5. [COUNTER\_TOP\_05] o\_count (15:12) shall be set when the corresponding bits from o\_bcdcount3 are set.
      6. [COUNTER\_TOP\_06] o\_count (19:16) shall be set when the corresponding bits from o\_bcdcount4 are set.
      7. [COUNTER\_TOP\_07] o\_count (23:20) shall be set when the corresponding bits from o\_bcdcount5 are set.
2. 4-bit counter submodule (Tag: COUNTER)
   1. Reset condition
      1. [COUNTER\_RESET] o\_bcdcount shall be set to “0000” on the negative edge of i\_resetn.
   2. Parameterization of rollover value - Module shall use a generic parameter ‘rollover\_count’ to indicate what value the instantiation will count to before resetting.
      1. [COUNTER\_ROLLOVER] o\_bcdcount shall be reset to “0000” when o\_bcdcount equal to ‘rollover\_count + 1’.
   3. State machine that cycles through count and idle states (Tag: COUNTER\_FSM)
      1. [COUNTER\_FSM\_01] All state transitions shall occur on the positive edge of i\_rtcclk.
      2. [COUNTER\_FSM\_02] Module shall be initialized in the idle state.
      3. [COUNTER\_FSM\_03] Module shall transition from idle state to count state when i\_countenb and i\_countinit is set.
      4. [COUNTER\_FSM\_04] Module shall transition from count state to idle state when i\_latchcount is set.
   4. Idle State
      1. [COUNTER\_FSM\_05] When in the idle state, o\_bcdcount shall keep its current value.
   5. Count State
      1. [COUNTER\_FSM\_06] When in the count state, o\_bcdcount shall increment on the positive edge of i\_rtcclk.

**7-Segment Display**

**Traceability:**