**Purpose:**

Create a stop-watch module in Verilog that runs on the Nexys A7 development board.

**Scope:**

A stop-watch that runs from 00:00:00 to 59:59:99 formatted as MM:ss:mm (M: minute, s: second, m: milli-second) , with one button to reset and one button to stop/start count.

**General Requirements:**

**Trigger Detection Circuit**

**10-Millisecond Timer**

**Initial Conditions:**

Timer\_INT\_001: Internal counter shall be set to value of 1.

Timer\_INT\_002: Module shall output “o\_basetick” to logic low when initializing.

Timer\_INT\_003: Module shall set maximum counting value of counter to 500000.

**Timer-Enable Conditions:**

Timer\_ENB\_001: Module shall take 100MHz “i\_sclk” clock input.

Timer\_ENB\_002: Module shall be enabled when “i\_timerenb” and “i\_reset\_n” are set to logic high

Timer\_ENB\_003: Module shall increment internal counter by 1 at rising edge of clock signal until counter reaches maximum counting value 500000.

Timer\_ENB\_004: Module shall reset the value of internal counter to 1 when counter reaches maximum counting value 500000.

Timer\_ENB\_005: Module shall toggle the output of “o\_basetick” when counter reaches maximum counting value 500000.

**Reset condition:**

Timer\_RST\_001: Module shall be reset when “i\_reset\_n” is set to logic low.

Timer\_RST\_002: Module shall reset value of the internal counter to 1

Timer\_RST\_003: Module shall set output of “o\_basetick” to logic low.

**12 Bit Up Counter**

**7-Segment Display**

**Traceability:**