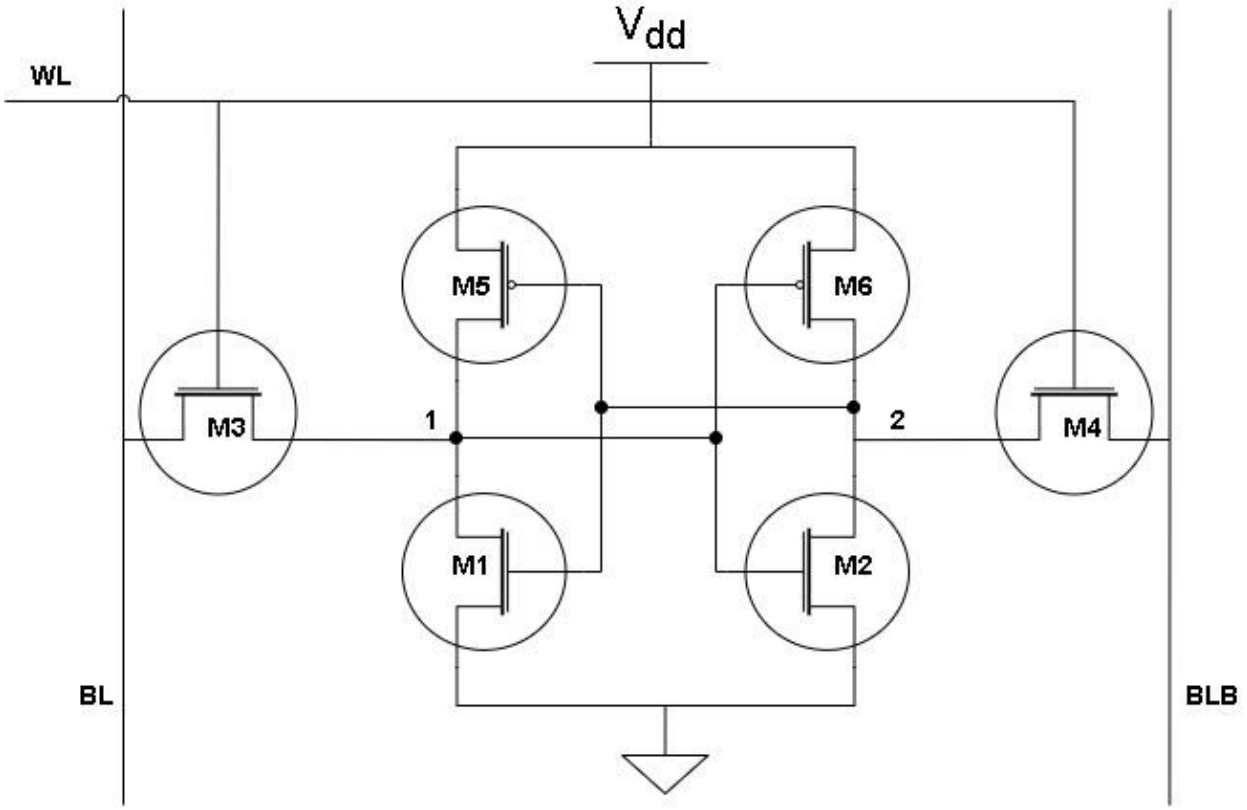
6-T SRAM Cell Sizing:

Typical MOS Parameters:

- Vdd = 5V
- Lmin = 0.4um
- Wmin = 0.6um
- Vtn = 0.49V (NMOS threshold voltage)
- Vtp = -0.66V (PMOS threshold voltage)
- un = 445 cm^2/Vs (NMOS mobility)
- up = 151 cm^2/Vs (PMOS mobility)

A schematic diagram of a standard 6-T SRAM cell is given below:



1. Read Operation:

Assuming logic 0 is stored in the cell i.e, V1=0V & V2=5V.
WL is connected to Vdd.

Transistor Region of Operation:

- M1 Linear Region
- M2 Cutoff Region

- M3 Saturation Region
- M4 Cutoff Region
- M5 Cutoff Region
- M6 Linear Region

The data read operation should not destroy the stored information.
The key design issue for the data-read operation is to guarantee that the voltage V1, does not exceed the threshold voltage of M2 so that the transistor M2 remains turned off during the read phase, i.e., **V1 ≤ Vtn.**

Now to maintain the stored data and considering the design constraint we can say that M1 should be stronger than M3.
After solving the Id equation for M1 and M3 we get:

$$\frac{(W/L)_3}{(W/L)_1} \prec \frac{[2(Vdd - Vtn)V1 - V1^2\ ]}{(Vdd - V1 - Vtn)^2}$$

Eq - 1

2. Write Operation:

Assuming logic 1 is stored in the cell i.e, V1=5V & V2=0.
WL is connected to Vdd.
BL = 0V & BLB = 5V. (Means we are trying to write logic 0 in the cell.)

Transistor Region of Operation:

- M1 Cutoff Region
- M2 Linear Region
- M3 Saturation Region
- M4 Saturation Region
- M5 Linear Region
- M6 Cutoff Region

The cell should allow modification of the stored information.
To change the stored information, i.e., to force V1 to 0 V, and V2 to *Vdd,* the node voltage V1, must be reduced below the threshold voltage of M2 so that M2 turns off first.

Now to modify the stored data and considering the design constraint we can say that M3 should be stronger than M5.
After solving the Id equation for M3 and M5 we get:

$$\frac{(W/L)_5}{(W/L)_3} \prec \frac{un}{up} * \frac{[2(Vdd - Vtn)V1 - V1^2\ ]}{(Vdd + Vtp)^2}$$

Eq - 2

Note: When circuit starts operating, and V1 node reaches to Vtn voltage then M3 will be in linear and M5 will be in saturation region.

Now using typical MOS parameters as given above and taking V1=Vtn=0.49V and **L=0.4um** (for all MOS).
From Eq -2 we get:

$$\frac{(W)_5}{(W)_3} \prec 0.654$$

From Eq - 1 we get:

$$\frac{(W)_3}{(W)_1} \prec 0.258$$

Taking $\mathbf{W_5}$ **= 0.6um** (since from above analysis we get strength of M1 > M3 > M5)
Then $\mathbf{W_3}$ **= 1um** and $\mathbf{W_1}$ **= 3.9um**.