Design and performance analysis of 6T SRAM cell on different CMOS technologies with stability characterization

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Design and performance analysis of 6T SRAM cell on different CMOS technologies with stability characterization

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Abstract: With the advent of portable devices, the demand for static random-access memory (SRAM) is increasing with large use of SRAM in System on Chip and high-performance VLSI circuits. SRAM optimization has become a focal point for research work, as 60% to 70% area of the chip is consumed by the memories. The performance parameters optimization can lead to the overall optimization of the performance of the chip. In this paper design and analysis of the 6T SRAM cell at different technologies using PTM (Predictive Technology Model) model has done with the aim of reducing power dissipation while maintaining stability. Then the performance of SRAM cell is compared on the basis of power dissipation i.e. dynamic power dissipation and static power dissipation, delay, Power Delay Product (PDP) and Static Noise Margin (SNM).SRAM cell read stability and write-stability are major concerns in nanometer CMOS technologies, due to the progressive increase in intra-die variability and Vdd scaling. Cell stability is also examined by the calculation of SNM with the help of the butterfly curve method at different CMOS technologies. Effect of variation of channel length on static power consumption, dynamic power consumption, delay, PDP and SNM is also measured. SNM variation is also observed with the variation of the supply voltage.

Keywords: Power dissipation (Static and Dynamic Power Dissipation), Delay, Power Delay Product, Static Noise Margin, Stability.

1. Introduction

Static Random Access (SRAM) constitutes a large percentage of area in the VLSI designs due to the high number of transistors for a single SRAM cell. Thus, the SRAM cell generally employsa minimum size transistor to have a high packing density [1].The size of the SRAM cell is being reduced using scaling over the past three decades [2].SRAM takes two design aspects: the power dissipation and propagation delay in reading and writing the value into the SRAM cell. The power dissipated during read and write operation is dynamic power dissipation. It helps to determine the battery life of portable devices. The speed of SRAM is determined by the delay in reading and writing [3]. In nanometre design, many design challenges occur due to device scaling [4]. The main concern for SRAM cell design is stability. Stability of memory is affected by the aspect ratio of MOSFET and operating conditions. The aim of stability in memory is to operate it correctly. The measure of stability in the SRAM cell is Static Noise Margin (SNM).The voltage transfer characteristics of the SRAM cell are used to obtain the SNM [5].SNM is the lowest voltage noise that can flip the state of SRAM [6]. While reading the stored data from SRAM, the stored value should not alter and SRAM should allow new data to be written into it during write phase [7]. Dynamic power dissipation and static power dissipation comprises the total power dissipation of SRAM.The dynamic power is consumed during the normal operation of the SRAM i.e. read and write whereas the standby power is consumed during the standby state [8]. The main objective of this paper is to design and analysis of 6T SRAM cell at different CMOS technologies with stability analysis. For this analysis, PTM model cards (Predictive Technology Model) are selected to explore the performance characterization in different modes of the cell. It provides accurate and compatible model files with a wide range of process variations [9, 10].The designs and simulations are carried out using Cadence Virtuoso Analog Design Environment.

Section 2 describes the design and stability analysis of conventional 6T SRAM. This section explains the architecture and working of conventional 6T SRAM. The various design metrics such as power dissipation i.e. static power dissipation and dynamic power dissipation, delay, and power delay product are discussed. The stability analysis determines the Static Noise Margin (SNM) with the help of the butterfly curve method used to arbitrate the stability of SRAM. The results drawn after the simulation are analyzedin section 3. Then finally conclusion is formulated in section 4.

2. Design and Stability Analysis of 6T SRAM

2.1 Architecture and Working of 6T SRAM

The architecture of the 6T SRAM Cell is shown in Figure1. The architecture consists of two-cross coupled CMOS inverters P1-N1 and P2-N2 used for storing a bit, and two access transistors N3-N4 used for performing read and write operations. The access transistors are activated/deactivated using the word line.The bit line acts as input while performing the write operation. The valueto be written into the memory cell is provided with the help of bit lines. However, the bit lines act as output during the read operation. The information is stored in the SRAM memory cell until power is supplied [8].To initiate read operation, the word lines are activated and bit lines are pre-charged[11].In read mode, the stored value either 0 or 1 in the SRAM cell is extracted. The word line is activated, which starts the access transistors i.e. N3 and N4. The voltage drop in the 'BL' or 'BLB' is sensed by the sense amplifier. Sense amplifier helps in determining the value of 'q'. In the write mode, the new value is stored in the SRAM cell. By applying 0 or 1 at 'q', new data is stored in the SRAM cell. In standby mode, the word lines are disabled, which in turn turns off the access transistors N3 and N4. The value stored in the SRAM cell retains its value in this condition [12].

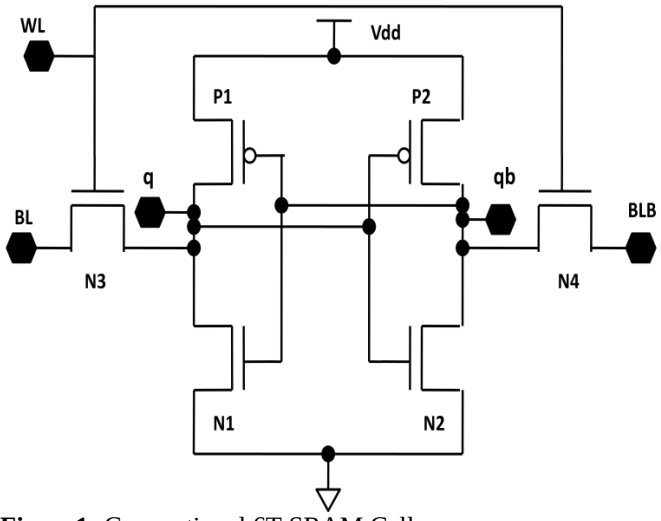


Figure1: Conventional 6T SRAM Cell

2.2 Design Metrics

2.2.1 Power Dissipation. The main requirement of the portable devices is long battery life with satisfactory performance. The main constraint for having a good battery is the dissipation of power. Static power dissipation and dynamic power dissipation constitutes total power dissipation [13].Static power dissipation occurs when the system is in standby mode and in SRAM, dynamic power dissipation is the power supply consumed during write and read operations. The power consumed is the product of the current consumed from the source and voltage consumed from the source [14].Mobile devices necessitate designs with low power dissipation. Dynamic power dissipation decreases as the technology node scales down. However, the static power dissipation increases in the deep submicron regions.

2.2.2 Delay. Delay is stated as the variation in the time at which input is applied and the time at which response is obtained. The main purpose of designing any system is to reduce delay that enhances the

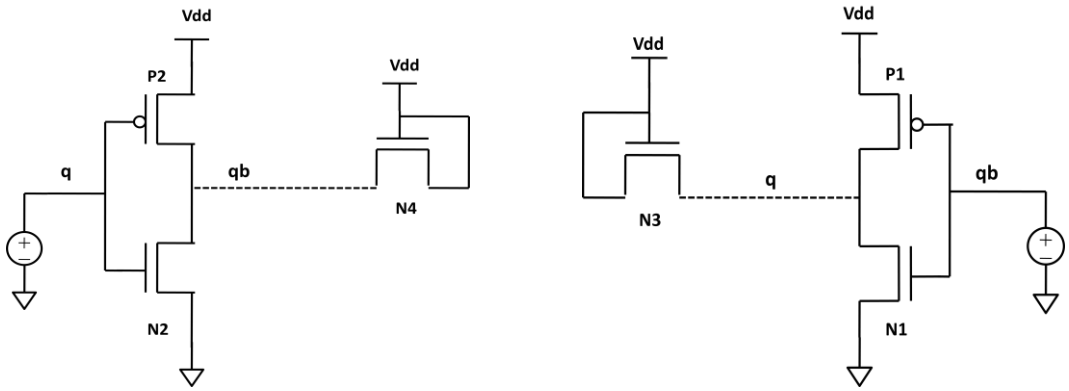
system speed. In SRAM, the speed is measured in terms of read access time and write access time.

2.2.3 Power Delay Product. Power delay Product (PDP) is defined as the multiplication of the average power consumption and the delay. It is also called switching energy because it measures the energy consumed in a switching event (that is, for 0 to 1 or 1 to 0 transition).The performance is determined by the Power Delay Product. Circuit design with low Power Delay Product is considered energy efficient.

2.3 Stability Analysis

2.3.1Static Noise Margin. Static Noise Margin helps to determine the stability of the SRAM [13, 14].The least noise voltage needed to change the cell state is SNM [15].One of the methods of calculating the Static Noise Margin (SNM) is by plotting the butterfly curve [13].Butterfly curve is plotted by drawing and mirroring the inverter characteristics and then finding the maximum possible square between them [13, 14, 16]. The length of the side of the square gives SNM. Greater the SNM better is stability.

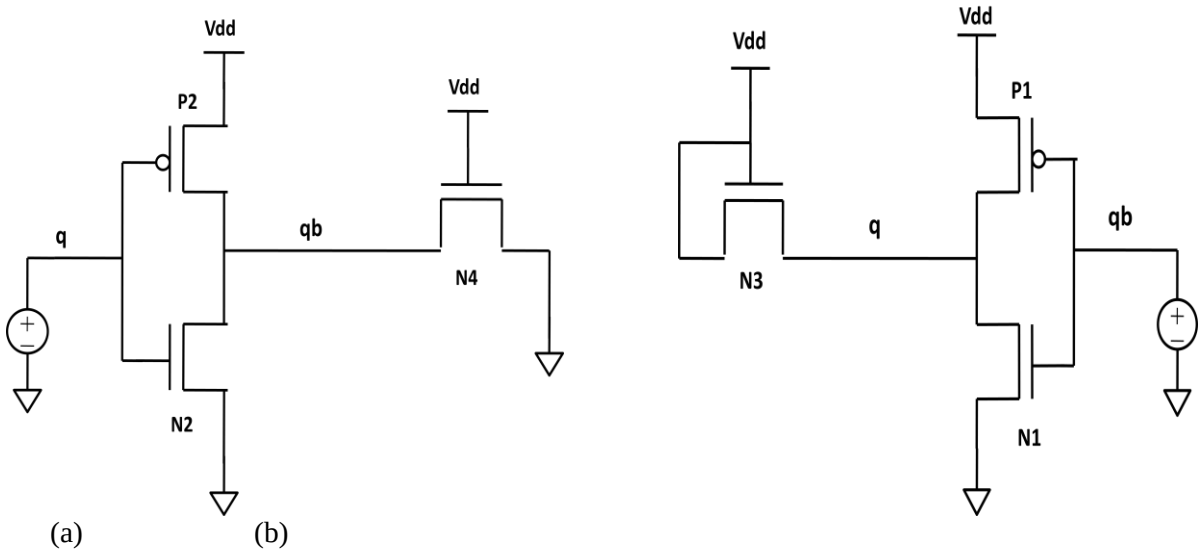
2.3.1.1Static Noise Margin in Hold Mode. Inabsence of word line voltage, the ability of SRAM to retain the stored data is defined as hold stability. The Schematics shown in Figure 2 are used for measuring SNM by using butterfly curve measurement method in hold mode [2].The dashed line in Figure 2 denotes that there is no connection between the circuits.



(a) (b)

Figure 2: The Schematic for determining Static Noise Margin in Hold Mode of SNM.

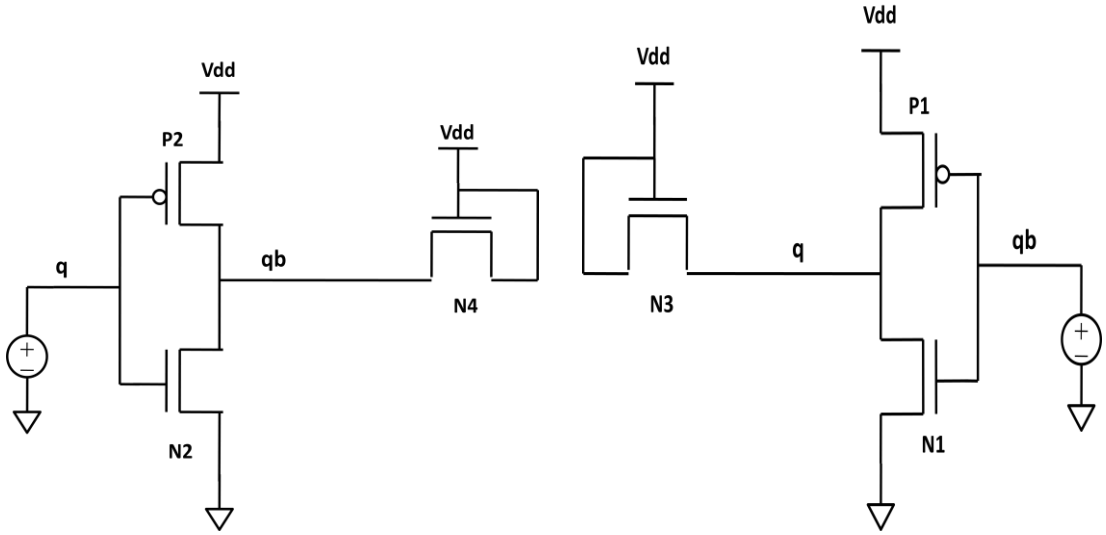
2.3.1.2 Static Noise Margin in Write Mode. The minimum voltage required to feed new value into the SRAM cell is known as write margin [14].Write stability is the ability of the SRAM to allow the changes in the stored value. Figure 3 shows the schematic for the calculation of SNM using the butterfly curve method in the write mode of SRAM.



(a) (b)

Figure 3: The Schematic for determining Static Noise Margin in Write Mode of SNM.

2.3.1.3 Read Margin. The read margin is used to find out read stability of the SRAM. Read Stability is the ability to prevent the SRAM cell to flip the stored value while the stored value is being read [14]. Figure 4 shows the schematics for the SNM measurement using the butterfly curve method in the read mode of SRAM [2].The value of SNM is least during the read operation which means the SRAM is most vulnerable during read operation [5].



(a) (b)

Figure 4: The Schematic for determining Static Noise Margin in Read Mode of SNM.

3. Simulation Results

This section discusses simulation result and performance analysis of conventional 6T SRAM cell at different CMOS technologies using PTM model with the help of Cadence Virtuoso tool. Transient response is investigated as a simulation result, which is shown in Figure 5.For the 6T SRAM cell, the power supply of 1.1V on45nm technology node, 1V on 32nm technology node, 950mV on 22nm technology node, and 900mV on 16nm technology node is chosen with keeping same cell ratio and pull up ratio. The cell ratio (CR) is the W/L ratio of the pull-down transistor to the access transistor and pull up ratio (PR) is the W/L ratio of pull-up transistor to the access transistor[4, 5].Stability of the data stored in SRAM degrades when the supply voltage is decreased [18].

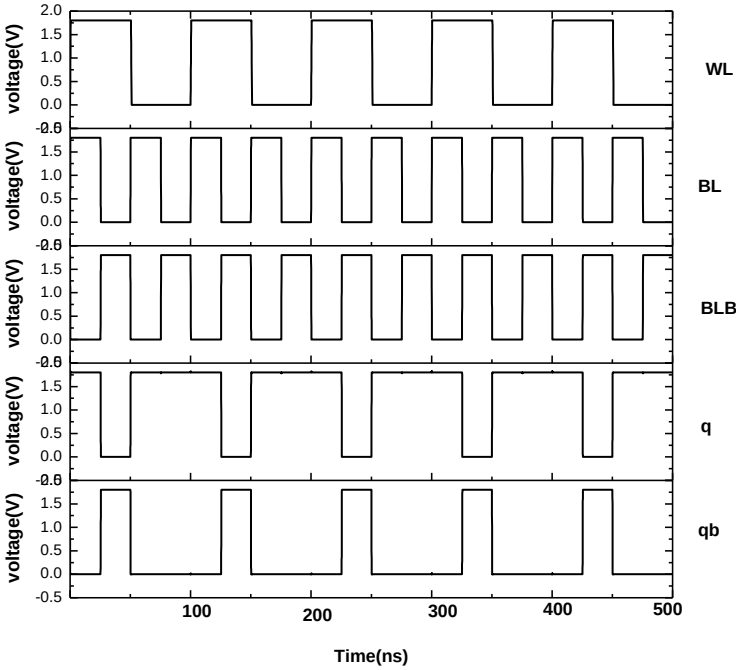


Figure 5: Transient Analysis of 6T SRAM.

SNM of SRAM cell is calculated with the help of graphical approach in which butterfly curve plotted for both inverters and then the length of the maximum possible square is observed that can be embedded in it, which is the value of SNM. Figure 6-8 shows the SNM plot for SRAM Cell in hold mode, read mode and write operation respectively.

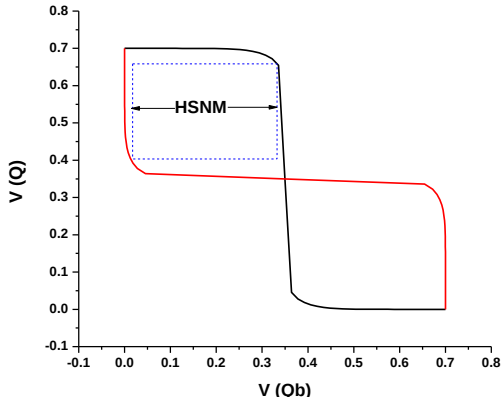


Figure 6:SNM curve for SRAM in hold mode

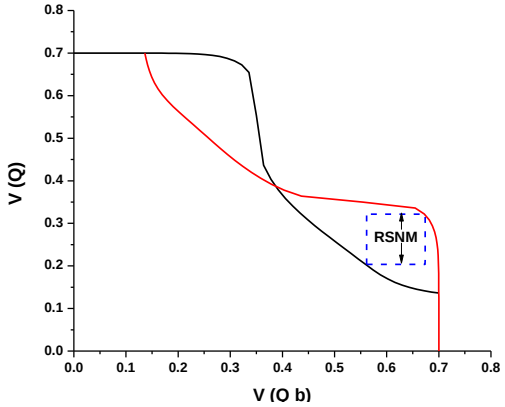


Figure 7:SNM curve for SRAM in read mode

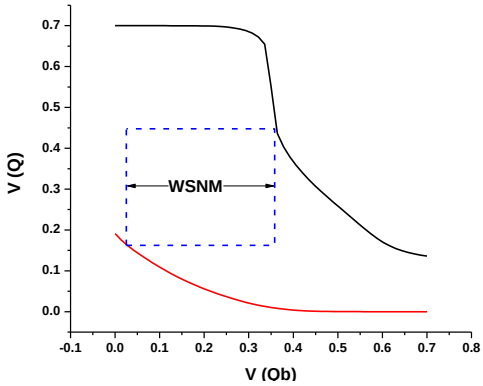


Figure 8: SNM curve for SRAM in write operation

It is interpreted from Table 1 that the total power dissipation decreases with the decreasing CMOS technology nodes. The static power dissipation is seen to increase in the deep submicron technologies as the short channel effects become dominating [19]. However, the dynamic power dissipation decreasesdue to low power concepts [20-22]. The results are obtained when the width of the CMOS devices is kept the same as the length of it. Delay comparison is shown in Table 2.

Table 1: Comparison of Power dissipation on different technology nodes

Technology	Static Power Dissipation (W)	Dynamic Power Dissipation (W)	Total Power Dissipation (W)
45 nm	12.991 p	4.720n	4.733 n
32 nm	15.773 p	2.103 n	2.119 n
22nm	23.782 p	0.910 n	0.934 n
16 nm	46.348 p	0.366 n	0.413 n

Table 2: Comparison of Delay on different technology nodes

Delay (s)	45 nm	32 nm	22 nm	16 nm
Delay (Falling) (s)	128.825 p	133.43 p	147.135 p	139.292 p
Delay (Rising) (s)	222.058 p	226.333 p	218.016 p	177.425 p

Table 3 depicts the power delay product which denotes the energy consumed by SRAM. The power-delay product is decreasing with the decreasing technology nodes.

Table 3: Comparison of Product Delay Product on different technology nodes

Power Delay Product (Ws)	45 nm	32 nm	22 nm	16 nm
Power Delay Product (Falling) (Ws)	610.714z	284.675z	134.673z	52.323z
Power Delay Product (Rising) (Ws)	1.05602a	483.887z	207.661z	81.189z

The static noise margin is decreasing with the decrease in the technology nodes. The side of the square of maximum size embedded in the butterfly curve gives the Static Noise Margin. SRAM is susceptible to lose its characteristics of read stability and write stability on further decrement in technology nodes. Table 4 shows the SNM analysis for the different technology nodes.

Table 4: Static Noise Margin comparison on different technology nodes

Technology	Write Mode SNM (mV)	Read Mode SNM (mV)	Standby Mode SNM (mV)
45 nm	480	50	190
32 nm	450	30	160
22nm	410	34	120
16 nm	370	40	80

Figure 9-12 shows the variability of Static Noise Margin with respect to supply voltage on 45nm, 32nm, 22nm and 16nm technology nodes respectively.

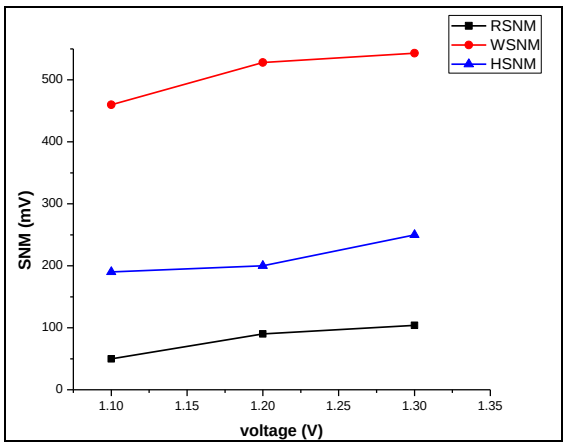


Figure 9: SNM variability with supply voltage on 45nm technology.

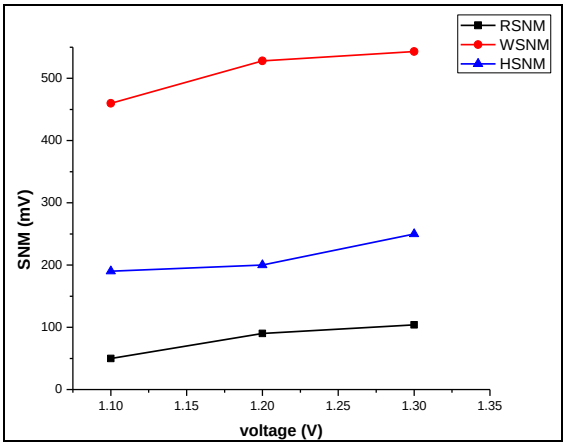


Figure 10: SNM variability with supply voltage on 32nm technology.

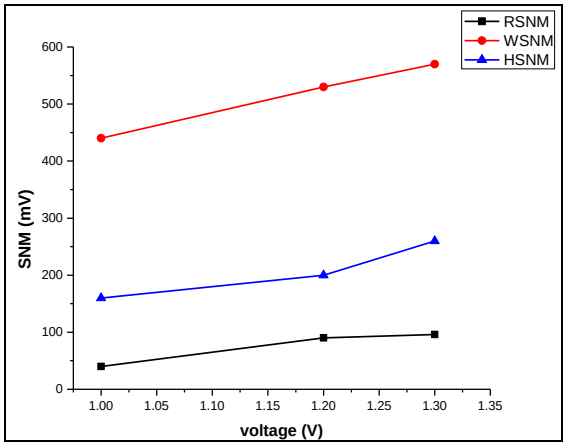


Figure 11: SNM variability with supply voltage on 22nm technology.

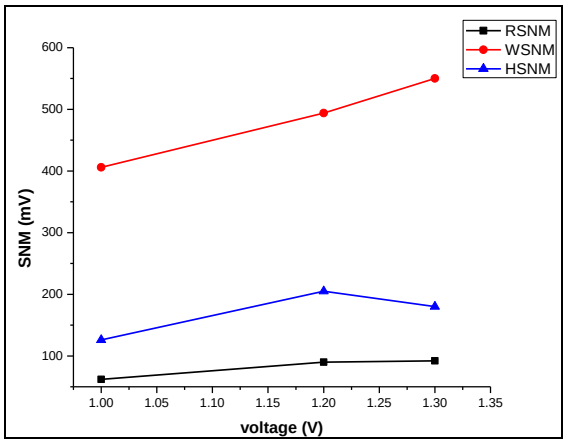


Figure 12: SNM variability with supply voltage on 16nm technology.

4. Conclusion

In this paper, we have analyzed the performance of conventional 6T SRAM cell at different technology nodes using PTM models in terms of power dissipation, delay, power-delay product, and static noise margin. The comparison of the results is done at 45nm, 32nm, 22nm and 16nm technology nodes, which shows that power dissipation and delay is improved as the channel length is reduced but stability is also main important concern. The percentage decrease in total power dissipation from 45nm to 16nm technology node is 91.27%. Stability is also examined for read, write, and standby modes at different technology nodes. However, the Static Noise Margin also decreases by 22.92% in write mode, 20% in read mode and 57.89% in hold mode with reducing channel length from 45nm to 16nm. SNM variation with respect to supply voltage shows that SNM is also a function of supply voltage, proper selection of supply voltage is also necessary to maintain the stability of memory cell. Stability should be maintained for reliability issues, although power dissipation and delay is improved with decreasing technology nodes. Further performance of 6T SRAM cell can be enhanced by applying different low power techniques.

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