Lab 2 Manual Scheduling Report
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Part 1 System Init

Briefly explain the clock path from start to finish (crystal to SYSCLK), including explanations for all your major register configurations.

The clock path begins by selecting the High-speed external clock signal (HSE) by setting the corresponding MCO mux bits. It continues to the HSE OSC 16 MHz. Then PLLSRC, PLLXTPRE, PLLMUL bits are reset, selecting the HSE Oscillator input into the mux. This is then passed to the PLLMUL block where the frequency is multiplied by a factor of 16. The PLLCLK output of this stage is then selected as the SYSCLK, at it's maximum frequency of 72 MHz.

Part 2 Motors

Describe how you determined your PWM frequency. Also describe how you would calculate CCR1 values for motors off, %50, and %100.

The TIM3 is running at 36 KHz: TIM3 Frequency = TIM3 counter clock/(ARR + 1) = 24 MHz / 666 = 36 KHz. We determined our PWM frequency with a 10% duty cycle because that gave us a safe motor spin. In order to set CCR1 values for motors off, set CCR1 to 0. For 50% set CCR1 to half the period of the timer period-1, or 332. For 100% set CCR1 to the period of the timer period-1, or 665.

Part 3 Manual Scheduling

Describe how a RTOS would make scheduling easier. What complications could arise if the high priority tasks had heavy computational requirements?

A RTOS system would make scheduling easier because it would introduce automatic scheduling, rather than having to handle scheduling and priorities manually in our code. If a high priority task has heavy computational requirements it can cause complications because its priority will pause lower priority tasks in order to run. Due to its heavy computational requirements, it will cause the lower priority tasks to be paused for longer while the high priority task completes. This could interfere with the timing of lower-priority operations.