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| **Test** | **Conditions** | **Procedures** | **Expected Results** | **Actual Results** |
| Verify reset | Fully Compiled Code on Quartus and Modelsim-Altera | Rst input is ‘0’ | All but PC and SP set to 0s | All but PC and SP set to 0s |
| Run | Previous tests passed. That given, conditions will be set for subsequent tests | Run => ‘1’ | NextState becomes Fetch | NextState becomes Fetch |
| Fetch | Previous tests passed. That given, conditions will be set for subsequent tests | Code should automatically advance  Asser databus value | Databus assigned to nextIR, nextPC incremented, next State to Decode | Databus assigned to nextIR, nextPC incremented, next State to Decode |
| Decode | Previous tests passed. That given, conditions will be set for subsequent tests | Read databus and analyze it | const\_out assigned to “C100” and ctl\_assigned to “25C0”, nextState is Exec | const\_out assigned to “C100” and ctl\_assigned to “25C0”, nextState is Exec |
| Execute,  sethi | Previous tests passed. That given, conditions will be set for subsequent tests | Determine nextStatus, do requisite actions for OP | nextStatus =”10”, nextState is Mem | nextStatus =”10”, nextState is Mem |
| Memory state | Previous tests passed. That given, conditions will be set for subsequent tests | Const\_out overwritten, | Const\_out =”000”, nextState WB | Const\_out =”000”, nextState WB |
| Write Back | Previous tests passed. That given, conditions will be set for subsequent tests | Vals reset to neutral | Vals reset to neutral, nextState is Fetch | Vals reset to neutral, nextState is Fetch |
| Bn | Previous tests passed. That given, conditions will be set for subsequent tests | Branch to to PC if N var is ‘1’ | CurrPC= “0084” | CurrPC= “0084” |
| Addx | Previous tests passed. That given, conditions will be set for subsequent tests | Assign a ctl wd equivalent to the instruction given on datapath | Output ctl\_wd “1D8A” | Output ctl\_wd “1D8A” |
| St | Previous tests passed. That given, conditions will be set for subsequent tests | St val in memory as specified in Instruction | St\_op and mem\_wr = 1 and correct ctl\_wd “0438” | St\_op and mem\_wr = 1 and correct ctl\_wd “0438” |
| call | Previous tests passed. That given, conditions will be set for subsequent tests | Move to specified PC location to execute more fun code SP decremented | Sp= 7FFD  PC= 0300 | Sp= 7FFD  PC= 0300 |
| Ld- data asserted during fetch | Previous tests passed. That given, conditions will be set for subsequent tests | Move val from mem to specified register | Ld\_op=’1’ctl wd(15 downto 8) = 4c | Ld\_op=’1’ctl wd(15 downto 8) = 4c |
| Ld- data asserted during execute | Previous tests passed. That given, conditions will be set for subsequent tests | Nothing should happen | No change | No change |
| ret- data asserted during fetch | Previous tests passed. That given, conditions will be set for subsequent tests | Return to previous sp location and move to specified PC loc | PC= (“0087”)  SP= 7FFE | PC= (“0087”)  SP= 7FFE |
| Ret- data asserted during execute | Previous tests passed. That given, conditions will be set for subsequent tests | Nothing should happen | No change | No change |
| Hlt | Previous tests passed. That given, conditions will be set for subsequent tests | STOP EVERYTHING | nextState becomes reset | nextState becomes reset |