|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Test** | **Conditions** | **Procedures** | **Expected Results** | **Actual Results** |
| Verify reset | Fully Compiled Code on Quartus and Modelsim-Altera |  | All but PC and SP set to 0s | All but PC and SP set to 0s |
| Run | Fully Compiled Code on Quartus and Modelsim-Altera |  | NextState becomes Fetch |  |
| Fetch | Fully Compiled Code on Quartus and Modelsim-Altera |  | Databus assigned to nextIR, nextPC incremented, next State to Decode |  |
| Decode | Fully Compiled Code on Quartus and Modelsim-Altera |  | const\_out assigned and ctl\_assigned and analyzed, nextState is Exec |  |
| Execute,  sethi | Fully Compiled Code on Quartus and Modelsim-Altera |  | nextStatus determined, nextState is Mem |  |
| Memory state | Fully Compiled Code on Quartus and Modelsim-Altera |  | Const\_out overwritten, nextState WB |  |
| Write Back |  |  | Vals reset to neutral, nextState is Fetch |  |
| Bn | Fully Compiled Code on Quartus and Modelsim-Altera |  | Branch to ‘immediate’ + current pc. (assign to nextPC) |  |
| Addx | Fully Compiled Code on Quartus and Modelsim-Altera |  | Output ctl\_wd “1D8A” representing the desired Datapath input |  |
| St | Fully Compiled Code on Quartus and Modelsim-Altera |  | St\_op and mem\_wr = 1 and correct ctl\_wd “0438” |  |
| call | Fully Compiled Code on Quartus and Modelsim-Altera |  | Reassigning PC to val specified in datapath/ IR (“0300” |  |
| Ld- data asserted during fetch | Fully Compiled Code on Quartus and Modelsim-Altera |  | Ld\_op=’1’ctl wd assigned |  |
| Ld- data asserted during execute | Fully Compiled Code on Quartus and Modelsim-Altera |  | No change |  |
| ret- data asserted during fetch |  |  | Return to position specifie din datapath (“0087”) |  |
| Ret- data asserted during execute |  |  | No change |  |
| Hlt |  |  | nextState becomes reset |  |