HLS-Assignment 5 B

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1 Problem Statement

Implement a DUT that takes 4 inputs in 4 clock cycles and then saves all the inputs in a BRAM (The BRAM should be contained within the DUT) at a single address. At the same time, it also gives out all the 4 inputs as a single bundle output in the same clock cycle when it receives the final input. The BRAM index will overflow after the BRAM is full and it should overwrite the old values as more inputs keep coming in.

2 Design Code

```
#include"hls_stream.h"
#include "ap_int.h"
//#include "ap_axi_sdata.h"
using namespace std;

struct bundle{
        ap_uint<8> data[4];
};

void a5b(hls::stream<bundle> &in, hls::stream<bundle> &out){
```

```
bundle input=in.read();

bundle output={0,0,0,0};
ap_uint<8> bram[8];
#pragma HLS RESOURCE variable=bram core=RAM_1P_BRAM
#pragma HLS ARRAY_RESHAPE variable=bram cyclic factor=4 dim=1
ap_uint<3> c=0,add=0;
int ind=0;

for (int i=0;i<4;i++){

        if (c<8){
        bram[add]=input.data[ind];
        c=c+1;
        add=add+1;
        ind=ind+1;

        if (c==4){
        output.data[0]=bram[0];
        output.data[1]=bram[1];
        output.data[2]=bram[2];
        output.data[3]=bram[3];
        }
        }
        else{
        c=0;
        add=0;
        }
        }
        out.write(output);
        }
```

3 Test Bench Code

```
#include<hls_stream.h>
#include <ap_int.h>
#include<iostream>
#include <fstream>
using namespace std;

struct bundle{
        ap_uint<8> data[4];
};


void a5b(hls::stream<bundle> &in, hls::stream<bundle> &out);
int main(){
hls::stream<bundle> indata;
hls::stream<bundle> outdata;
bundle input;
ifstream in;
ofstream out_d;

in.open("in.dat");
out_d.open("out.dat");

int i,index=0;
bool fail=0;

while (in>>i && index<4){
input.data[index]=i;
index=index+1;
}
indata.write(input);
a5b(indata,outdata);
bundle output=outdata.read();
for (int j=0;j<4;j++){
out_d<<output.data[j]<<" ";
}
if (input.data[0]==output.data[0] && input.data[1]==output.data[1] &&
 input.data[2]==output.data[2] && input.data[3]==output.data[3] ){
out_d<<"Pass"<<endl;
}
else{
out_d<<"Fail"<<endl;
fail++;
}
```

```
in.close();
out_d.close();
if (fail==0){
cout<<"ALL THE TEST CASES ARE PASSED!"<<endl;
}
else{
cout<<"ERROR! ALL THE TEST CASES ARE NOT PASSED!"<<endl;
}}
```

4 in.dat file

```
7 8 6 4
```

5 out.dat file

```
7 8 6 4 Pass
```

6 HLS Resource Consumption

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	1051
FIFO	-	-	-	-
Instance	-	-	0	21
Memory	1	-	0	0
Multiplexer	-	-	-	177
Register	-	-	89	-
Total	1	0	89	1249
Available	280	220	106400	53200
Utilization (%)	~0	0	~0	2

Figure 1: Resource Consumption

7 HLS Timing Report

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	7.397	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
9	9	9	9	none

Detail

Figure 2: Timing Report

8 Interfaces Report

Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	a5b	return value
ap_rst	in	1	ap_ctrl_hs	a5b	return value
ap_start	in	1	ap_ctrl_hs	a5b	return value
ap_done	out	1	ap_ctrl_hs	a5b	return value
ap_idle	out	1	ap_ctrl_hs	a5b	return value
ap_ready	out	1	ap_ctrl_hs	a5b	return value
in_V_data_0_V_dout	in	8	ap_fifo	in_V_data_0_V	pointer
in_V_data_0_V_empty_n	in	1	ap_fifo	in_V_data_0_V	pointer
in_V_data_0_V_read	out	1	ap_fifo	in_V_data_0_V	pointer
in_V_data_1_V_dout	in	8	ap_fifo	in_V_data_1_V	pointer
in_V_data_1_V_empty_n	in	1	ap_fifo	in_V_data_1_V	pointer
in_V_data_1_V_read	out	1	ap_fifo	in_V_data_1_V	pointer
in_V_data_2_V_dout	in	8	ap_fifo	in_V_data_2_V	pointer
in_V_data_2_V_empty_n	in	1	ap_fifo	in_V_data_2_V	pointer
in_V_data_2_V_read	out	1	ap_fifo	in_V_data_2_V	pointer
in_V_data_3_V_dout	in	8	ap_fifo	in_V_data_3_V	pointer
in_V_data_3_V_empty_n	in	1	ap_fifo	in_V_data_3_V	pointer
in_V_data_3_V_read	out	1	ap_fifo	in_V_data_3_V	pointer
out_V_data_0_V_din	out	8	ap_fifo	out_V_data_0_V	pointer
out_V_data_0_V_full_n	in	1	ap_fifo	out_V_data_0_V	pointer
out_V_data_0_V_write	out	1	ap_fifo	out_V_data_0_V	pointer
out_V_data_1_V_din	out	8	ap_fifo	out_V_data_1_V	pointer
out_V_data_1_V_full_n	in	1	ap_fifo	out_V_data_1_V	pointer
out_V_data_1_V_write	out	1	ap_fifo	out_V_data_1_V	pointer
out_V_data_2_V_din	out	8	ap_fifo	out_V_data_2_V	pointer
out_V_data_2_V_full_n	in	1	ap_fifo	out_V_data_2_V	pointer
out_V_data_2_V_write	out	1	ap_fifo	out_V_data_2_V	pointer
out_V_data_3_V_din	out	8	ap_fifo	out_V_data_3_V	pointer
out_V_data_3_V_full_n	in	1	ap_fifo	out_V_data_3_V	pointer
out_V_data_3_V_write	out	1	ap_fifo	out_V_data_3_V	pointer

Figure 3: Interface Summmary

9 C/RTL Cosimulation Output

```
Starting C/RTL cosimulation ...
/tools/Xilinx/Vivado/2018.3/bin/vivado_hls /home/sam-admin/git/Training/HLS_Assi
INFO: [HLS 200-10] Running '/tools/Xilinx/Vivado/2018.3/bin/unwrapped/lnx64.o/vi
INFO: [HLS 200-10] For user 'sam-admin' on host 'sampaths-lappie' (Linux_x86_64
INFO: [HLS 200-10] On os Ubuntu 22.04.2 LTS
INFO: [HLS 200-10] In directory '/home/sam-admin/git/Training/HLS_Assignments/A5
INFO: [HLS 200-10] Opening project '/home/sam-admin/git/Training/HLS_Assignments
INFO: [HLS 200-10] Opening solution '/home/sam-admin/git/Training/HLS_Assignment
INFO: [SYN 201-201] Setting up clock 'default' with a period of 10ns.
INFO: [HLS 200-10] Setting target device to 'xc7z020clg484-1'
INFO: [COSIM 212-47] Using XSIM for RTL simulation.
INFO: [COSIM 212-14] Instrumenting C test bench ...
   Build using "/tools/Xilinx/Vivado/2018.3/tps/lnx64/gcc-6.2.0/bin/g++"
   Compiling a5b.cpp_pre.cpp.tb.cpp
   Compiling a5b_tb.cpp_pre.cpp.tb.cpp
   Compiling apatb_a5b.cpp
   Generating cosim.tv.exe
INFO: [COSIM 212-302] Starting C TB testing ...
ALL THE TEST CASES ARE PASSED!
INFO: [COSIM 212-333] Generating C post check test bench ...
INFO: [COSIM 212-12] Generating RTL test bench ...
INFO: [COSIM 212-323] Starting verilog simulation.
INFO: [COSIM 212-15] Starting XSIM ...
INFO: [XSIM 43-3496] Using init file passed via -initfile option "/tools/Xilinx/
Vivado Simulator 2018.3
Copyright 1986-1999, 2001-2018 Xilinx, Inc. All Rights Reserved.
Running: /tools/Xilinx/Vivado/2018.3/bin/unwrapped/lnx64.o/xelab xil_defaultlib.
Multi-threading is on. Using 6 slave threads.
WARNING: [XSIM 43-3431] One or more environment variables have been detected whi
If errors occur, try running xelab with the "-mt off -v 1" switches to see more
   LIBRARY_PATH
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module glbl
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module apatb_a5b_top
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_in_V_data_2_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_out_V_data_0_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5b
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_out_V_data_3_V
```

```
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5b_mux_42_8_1_1
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_out_V_data_2_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_in_V_data_3_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5b_bram_V_ram
INFO: [VRFC 10-311] analyzing module a5b_bram_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_in_V_data_1_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_out_V_data_1_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_in_V_data_0_V
Starting static elaboration
Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module xil_defaultlib.a5b_bram_V_ram_default
Compiling module xil_defaultlib.a5b_bram_V(DataWidth=32,AddressR...
Compiling module xil_defaultlib.a5b_mux_42_8_1_1(ID=1,din0_WIDTH...
Compiling module xil_defaultlib.a5b
Compiling module xil_defaultlib.AESL_autofifo_in_V_data_0_V
Compiling module xil_defaultlib.AESL_autofifo_in_V_data_1_V
Compiling module xil_defaultlib.AESL_autofifo_in_V_data_2_V
Compiling module xil_defaultlib.AESL_autofifo_in_V_data_3_V
Compiling module xil_defaultlib.AESL_autofifo_out_V_data_0_V
Compiling module xil_defaultlib.AESL_autofifo_out_V_data_1_V
Compiling module xil_defaultlib.AESL_autofifo_out_V_data_2_V
Compiling module xil_defaultlib.AESL_autofifo_out_V_data_3_V
Compiling module xil_defaultlib.apatb_a5b_top
Compiling module work.glbl
Built simulation snapshot a5b


****** Webtalk v2018.3 (64-bit)
  **** SW Build 2405991 on Thu Dec  6 23:36:41 MST 2018
  **** IP Build 2404404 on Fri Dec  7 01:43:56 MST 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.


source /home/sam-admin/git/Training/HLS_Assignments/A5/5.2/codes/Assignment5b/so
INFO: [Common 17-206] Exiting Webtalk at Mon Apr  3 17:24:15 2023...
```

```
****** xsim v2018.3 (64-bit)
  **** SW Build 2405991 on Thu Dec  6 23:36:41 MST 2018
  **** IP Build 2404404 on Fri Dec  7 01:43:56 MST 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.


source xsim.dir/a5b/xsim_script.tcl
# xsim {a5b} -autoloadwcfg -tclbatch {a5b.tcl}
Vivado Simulator 2018.3
Time resolution is 1 ps
source a5b.tcl
## run all
////////////////////////////////////////////////////////////////////////////////
// Inter-Transaction Progress: Completed Transaction / Total Transaction
// Intra-Transaction Progress: Measured Latency / Latency Estimation * 100%
//
// RTL Simulation : "Inter-Transaction Progress" ["Intra-Transaction Progress"]
////////////////////////////////////////////////////////////////////////////////
// RTL Simulation : 0 / 1 [0.00%] @ "125000"
// RTL Simulation : 1 / 1 [100.00%] @ "235000"
////////////////////////////////////////////////////////////////////////////////
$finish called at time : 275 ns : File "/home/sam-admin/git/Training/HLS_Assignm
## quit
INFO: [Common 17-206] Exiting xsim at Mon Apr  3 17:24:23 2023...
INFO: [COSIM 212-316] Starting C post checking ...
ALL THE TEST CASES ARE PASSED!
INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***
INFO: [COSIM 212-211] II is measurable only when transaction number is greater t
Finished C/RTL cosimulation.
```

10 C/RTL Cosimulation Report

Cosimulation Report for 'a5b'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	9	9	9	NA	NA	NA

Export the report(.html) using the Export Wizard

Figure 4: Cosimulation Report