HLS-Assignment 9 (PART-1)

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VITIS-HLS

1 Problem Statement

Problem Statemt

Design a digital circuit using RTL and HLS for a 5G NR CRC bits generator.

Requirements:
1. The module should process 8 bits per clock cycle.
2. The input and output buses should use the AXIS interface.
3. Implement a pipelined design.
4. The implementation should use as minimum resources as possible.

Considerations:
1. Implement the module only for CRC24A
2. A last signal should be used to indicate the end of the input bit stream.
3. The design implementation should be targeted on the ZCU111 FPGA board.

2 Header File

header.h

```
#ifndef _HEADER_H_
#define _HEADER_H_

#include <hls_stream.h>
#include "ap_int.h"
#include "ap_axi_sdata.h"
using namespace std;

#define N 8      //input && ref
#define y 25     //length of divisor(parity)
#define x N+y-1  //length of crc (len of input+divisor-1)

typedef ap_uint<N> typo;


void crc24a(hls::stream<ap_axiu<N,0,0,0>>& input, hls::stream<typo>& output);

#endif

```

Figure 1: header.h

3 Crc bits Generator Code

crc.cpp ×

```cpp
#include "header.h"
void crc24a(hls::stream<ap_axiu<N,0,0,0>>& input, hls::stream<typo>& output) {

#pragma HLS INTERFACE mode=axis register_mode=both port=input register
#pragma HLS INTERFACE mode=axis register_mode=both port=output register

    ap_uint<1> crc[x],oput[x];
    ap_uint<1> divisor[y] = {1, 1, 0, 0, 0, 0, 1, 1, 0, 0, 1, 0, 0, 1, 1, 0, 0, 1, 1, 1, 1, 1, 0, 1, 1};
    typo o;

// Read input stream and do padding
    ap_axiu<N,0,0,0> d = input.read();
   loop1: for (int i = 0; i < x; i++) {
#pragma HLS UNROLL
        crc[i] = (i < N) ? d.data(i,i) : 0;
        oput[i] = (i < N) ? d.data(i,i) : 0;
    }

// Division is performed only when last is high
   loop2: for (int i = 0; i <= x - y; i++) {
#pragma HLS PIPELINE II=1
        if (crc[i] == 1 && d.last==1) {
          loop3:  for (int j = 0; j < y; j++) {
              int k=i+j;
#pragma HLS UNROLL
                crc[k] = crc[k] ^ divisor[j];
            }
        }
    }

// Write the result to output stream c
   loop4:for (int i = 0; i < x; i++) {
#pragma HLS UNROLL
       oput[i] = crc[i] ^ oput[i];
       o(i%N, i%N) = oput[i];
           if (i%N==7){
               output.write(o);
           } }}
```

Figure 2: crc.cpp

4 Design Choices

1. I Considered input message of length 8 and I designed the module accordingly.

2. The function takes two parameters: input and output.

   input is an AXIS input stream of ap_axiu type with a width of 8 bits and with a last signal.

   output is an AXIS output stream of ap_uint<8> type, since last signal is not requested.

3. The pragmas specify the interface properties for the function. mode=axis indicates that the function uses an AXI–Stream interface. register_mode=both specifies that both the input and output streams should be implemented using

registers.

4. divisor is an array of ap_uint<1> type with a size of 25(crc24a).

   crc and oput are arrays of ap_uint<1> type with a size of x(input length + divisor length − 1). crc array is used for crc computation and oput array is used to stream output data along with input message.

   o is a variable of type ap_uint<8> which is used for storing of output data and then streaming accordingly.

   d is a variable of type ap_uint<8> which reads input data. Since I had only 8 bits input data I read it only once.

5. loop1 initializes values to the crc and oput arrays based on the data present in d(from the input stream). It copies the i−th bit of d.data to crc[i] and oput[i] and it assigns all other indexes to zero.

   The loop is unrolled to improve the efficiency of copying bits from d.data to crc and oput arrays. Unrolling eliminates loop control overhead and allows multiple assignments to be performed in parallel.

6. loop2 and loop3 performs the division operation for the CRC algorithm. It checks if the i−th bit of crc is 1 and if d.last is also 1 (indicating it is the last element of the input stream). If both conditions are satisfied, it performs the XOR operation between crc[k] and divisor[j] and stores the result in crc[k] , where k iterates from i to i+y−1. At the end of loop3 crc array is loaded with crc computed values(remainder) of input message and divisor.

   For the loop2 the #pragma HLS PIPELINE II=1 directive is used to pipeline the loop iterations. By applying pipelining, the tool can overlap the execution of consecutive iterations, allowing the operations within the loop to be executed concurrently. This can result in increased throughput.

   Additionally, the #pragma HLS UNROLL directive is used for loop3. It instructs the tool to unroll the inner loop completely and multiple loop iterations are executed in parallel, which can further improve parallelism and increase performance.

7. loop4 performs the final XOR operation between crc(has crc computation output) and oput(has input message) arrays(since we need the output in form of input+crcoutput) and updates the o object with the XOR result.
   The line o(i%N, i%N) = oput[i]; assigns the i−th bit of oput to the corresponding position in o. Finally, if the current index i is a multiple of 8 (i.e., i%N == 7), it writes the o object to the output stream.

   This loop performs the final XOR operation between crc and oput arrays and updates the variable o. Unrolling the loop helps increase parallelism and pipeline the operations for better performance.

8. Overall, this code reads an input stream of AXI−Stream elements and performs the CRC−24 algorithm on the data, and writes the result to the output stream.

5 Testbench Code

crc_tb.cpp

```cpp
#include "header.h"
#include <vector>

int main() {
    hls::stream<ap_axiu<N,0,0,0>> a;
    hls::stream<typo> b;
    ap_axiu<N,0,0,0> w;

      w.data=0b00010110;                    //msbtolsb

           w.last=1;
           a.write(w);

// Perform binary divison
    crc24a(a, b);

// Read the result from the output stream
    vector<ap_uint<1>> p;
    cout << "CRC generator output : ";
    while(!b.empty()){
          typo d = b.read();
         for (int i = 0; i < N ; i++) {
            cout<< d(i,i);
            p.push_back(d(i,i));
          }
       }
       cout<<endl;
```

```cpp
// Checking if output is valid or not
           bool flag=0;
           ap_uint<1> divisor[y] = {1, 1, 0, 0, 0, 0, 1, 1, 0, 0, 1, 0, 0, 1, 1, 0, 0, 1, 1, 1, 1, 1, 0, 1, 1};


       //Output is valid only when remainder divison of output with divisor is 0
           for (int i = 0; i <= x - y; i++) {
               if (p[i] == 1) {
                   for (int j = 0; j < y; j++) {
                       p[i + j] = p[i+j] ^ divisor[j];
                   }
               }
           }
           cout<<"CRC detector output :  ";
           for (int i = 0; i < 32; i++) {
            cout<<p[i];
               if (p[i]==1){
                flag=1;
               }
           }
            cout<<endl;
           if ( flag==0) {
                      cout << "!PASS!CRC Check at detector is Success" << endl;
                  }
           else {
                      cout << "!ERROR!CRC Check at detector has Failed" << endl;
                  }
    return 0;
}
```

(a) crctb.cpp

6 C simulation Output

crc24a_csim.log

```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../../codes/crc_tb.cpp in debug mode
   Compiling ../../../../codes/crc.cpp in debug mode
   Generating csim.exe
CRC generator output : 01101000101101001111001100000010
CRC detector output :  00000000000000000000000000000000
!PASS!CRC Check at detector is Success
INFO [HLS SIM]: The maximum depth reached by any hls::stream() instance in the design is 4
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************

```

Figure 4: C Simulation Output

7 HLS Resource Consumption Report

crc.cpp header.h crc24a_csim.log Co-simulatic

Utilization Estimates

Summary

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	20	-
FIFO	-	-	-	-	-
Instance	-	-	38	768	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	87	-
Register	-	-	49	-	-
Total	0	0	87	875	0
Available	624	1728	460800	230400	96
Utilization (%)	0	0	~0	~0	0

Figure 5: Resource Consumption

8 HLS Timing and Fmax Report

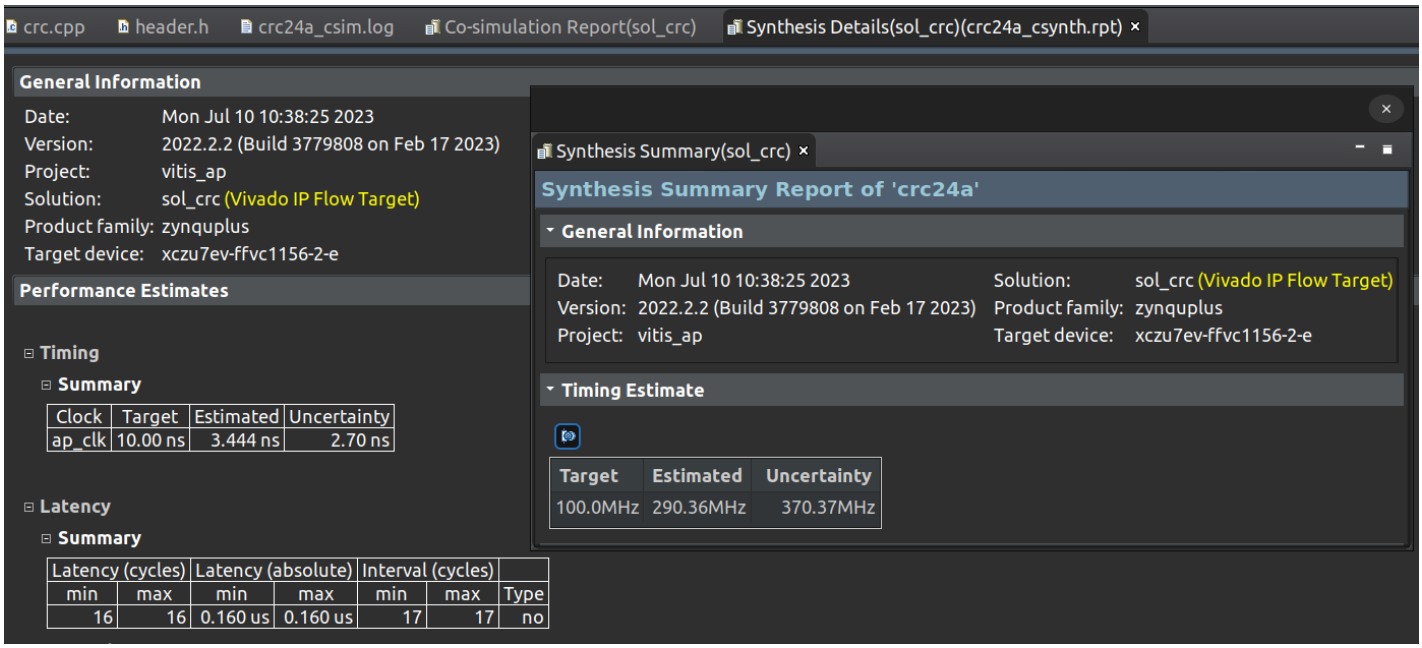


Figure 6: Timing and Fmax

9 CoSimulation Report

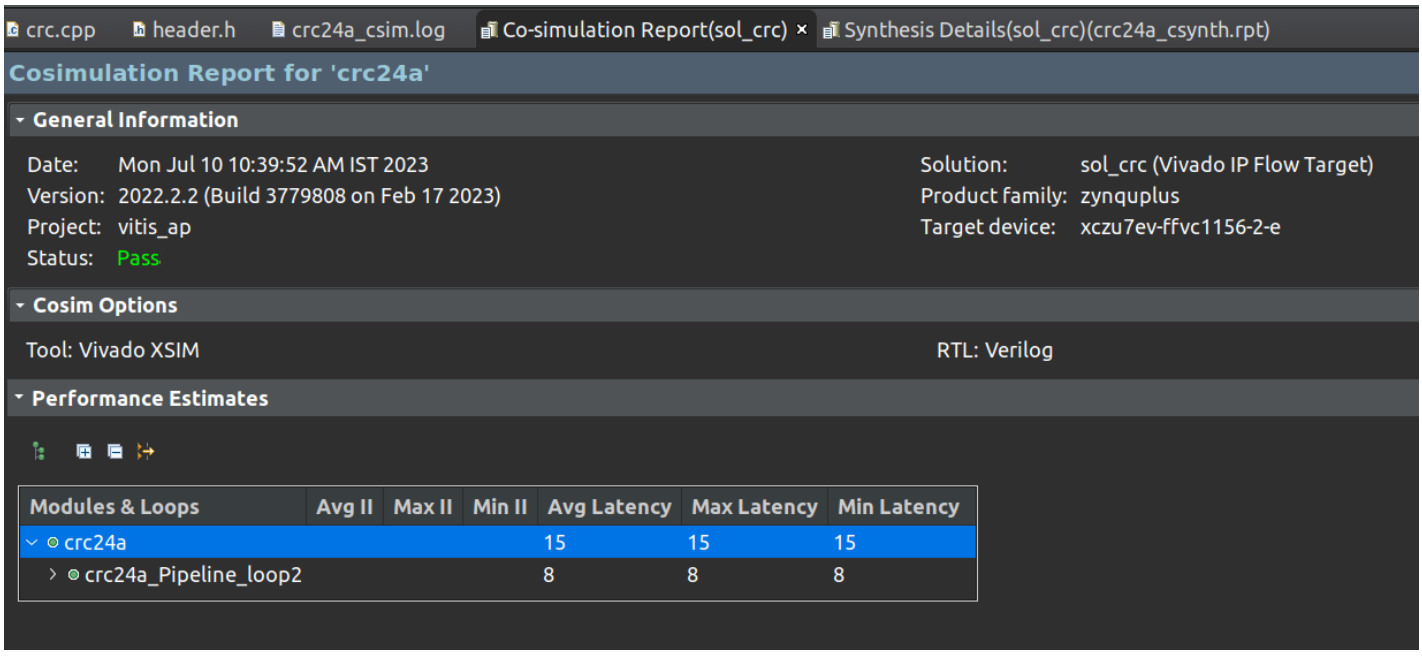


Figure 7: Cosimulation

10 Performance Evaluation

After synthesis source code has :

1. Execution Time: 12.65 seconds
2. Latency: 16
3. Resource Utilization: 87 FF & 875 LUT
4. Memory Usage: 76.434 MB
5. Fmax: 290.36 MHz
6. Iteration Interval: 17
7. Throughput: 0.632

VIVADO

11 Block Design

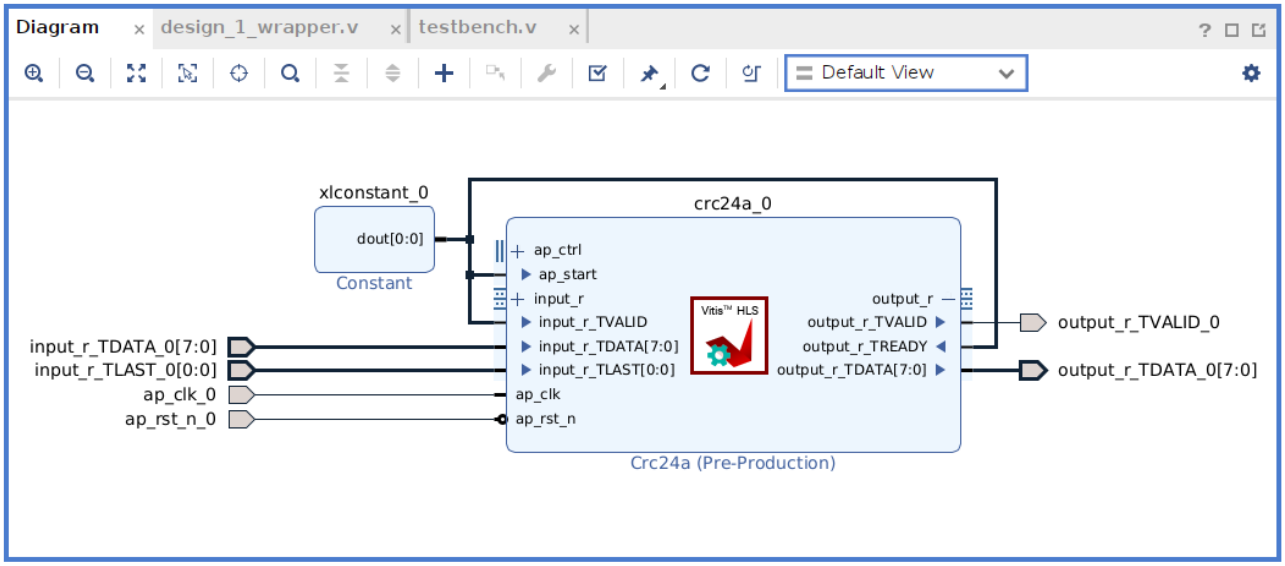
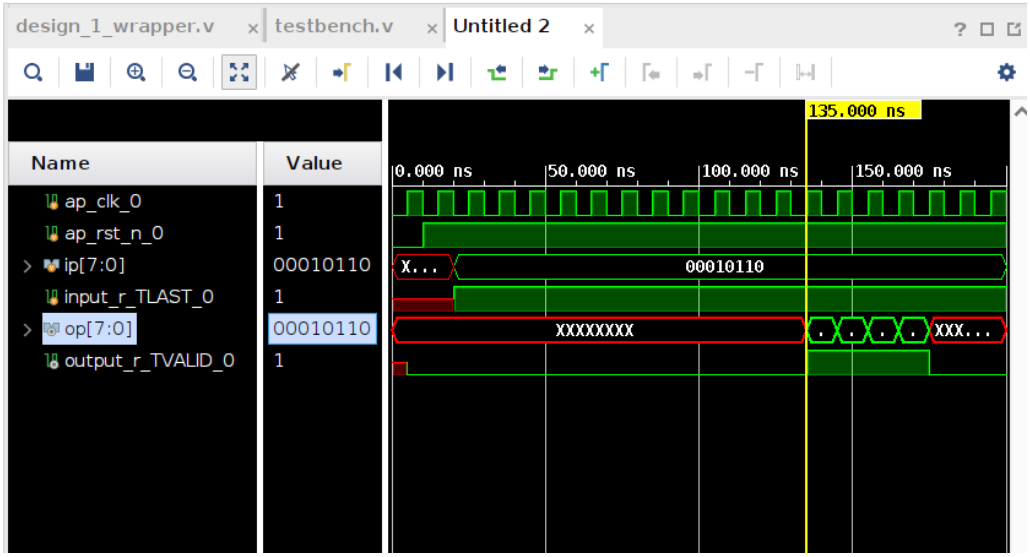


Figure 8: Block Diagram

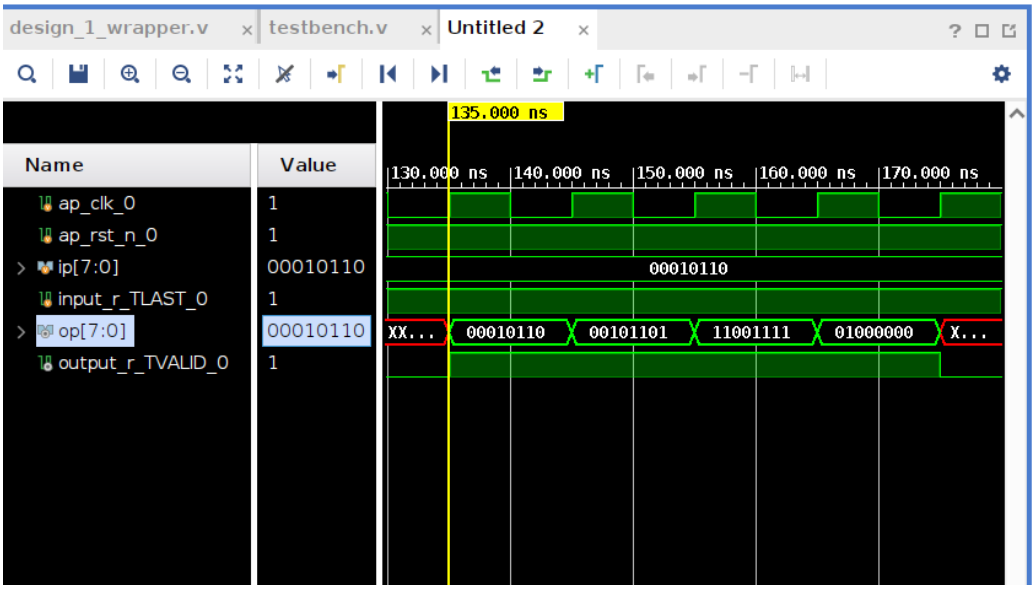
12 Verilog Testbench

```
//testbench.v
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 06/26/2023 11:35:30 AM
// Design Name:
// Module Name: testbench
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module testbench();
        reg ap_clk_0;
        reg ap_rst_n_0;
        reg [7:0] ip;
        reg input_r_TLAST_0;
        wire [7:0] op;
        wire output_r_TVALID_0;


   design_1_wrapper uut(.ap_clk_0(ap_clk_0),.input_r_TLAST_0(input_r_TLAST_0),
   .ap_rst_n_0(ap_rst_n_0),.input_r_TDATA_0(ip),.output_r_TDATA_0(op),
   .output_r_TVALID_0(output_r_TVALID_0));

        always #5 ap_clk_0=~ap_clk_0;

        initial begin
        ap_clk_0=0;ap_rst_n_0=0;
        #10
        ap_rst_n_0=1;
        #10
        ip=8'b00010110;//ascii "h"
        input_r_TLAST_0=1;
        #180
        $finish;
        end


endmodule
```

13 Output Waveform



(a) Output of IP



(b) Zoomed format of above figure

Rtl-Assignment 9 (PART-2)

July 10, 2023

RTL-VERILOG

1 CRC bits Generator Code

axistb.v | design_1_wrapper.v | crcaxis.v

/home/sam-admin/git/Training/HLS_Vivado/A9/PART-2_RTL/codes/crcaxis.v

```
1   `timescale 1ns / 1ps
2
3   module axis_reg #(
4           parameter integer N = 8
5       )
6       (
7
8           input wire clk,
9           input wire reset_n,
10          input wire [N - 1:0] s_tdata,
11          input wire s_tvalid,
12          input wire s_tlast,
13          output wire s_tready,
14          output wire [N - 1:0] m_tdata,
15          output wire m_tvalid,
16          input wire m_tready
17      );
18
19      reg [0:24] divisor = 25'b1100001100100110011111011;
20      reg [0:31] crc_reg,crc_own;
21      reg [4:0] cycle_counter;
22      reg [7:0] oup;
23      integer i, j;
24
25      always @(posedge clk) begin
26          if(!reset_n) begin
27              crc_reg <= 0;
28              crc_own<=0;
29              cycle_counter<=0;
30          end else if(s_tready) begin
31               crc_reg  = {s_tdata,{24{1'b0}}};
32
33      for (i = 0; i <=7; i = i + 1) begin
34        if (crc_reg[i] == 1 && s_tlast==1'b1) begin
35          for (j = 0; j < 25; j = j + 1) begin
36            crc_reg[i + j] = crc_reg[i + j] ^ divisor[j];
37          end
38        end
39      end
40      end
41      crc_own = {s_tdata,crc_reg[8:31]};
42      oup=crc_own[7+(8*cycle_counter) -:8];
43      cycle_counter = cycle_counter + 1;
44
45      end
46
47      assign m_tdata = oup;
48      assign m_tvalid = m_tdata?1:0;
49      assign s_tready = m_tready || !m_tvalid;
50  endmodule
51
```

(a) crcaxis.v

2 Design Choices

1. With same design Choices as PART–1, I designed PART–2 by defining all I/O buses manually.

2. s_tdata is the input data,
   s_tvalid indicates the input data validity,
   s_tlast marks the last input data,
   m_tdata represents the output data, and
   m_tready represents the activation of port
   m_tvalid indicates the output data validity.
   The clk and reset_n are clock and reset signals, respectively.
   The parameter N specifies the width of the data bus.

3. the crc_reg is updated by concatenating the input data s_tdata with 24 zeros.
   Same as part−1, here crc_reg performs crc computation and crc_own stores computed data in crc_reg along with input message(s_tdata+crc_reg).

   cycle_counter assigns 8 bits of data from crc_own to oup. where, oup is the output data.

4. always block sensitive to the positive edge of the clock signal. It handles the CRC calculation.
   When reset_n is low (active low reset signal), the registers are reset to their initial values.
   When s_tready is high (indicating that the downstream module is ready to accept data),

5. The two nested for loops are used as followes:
   The outer loop iterates from 0 to 7(to consider only 25 bits of data for computation for inner loop), and
   The inner loop iterates from 0 to 24.
   It checks if crc_reg[i] is 1 and s_tlast is high (indicating the last input data). If the condition is true, it performs the XOR operation between crc_reg[i + j] and divisor[j], updating the CRC value.

6. After the CRC calculation, the crc_own register is updated by concatenating s_tdata with crc_reg[8:31]. Then, oup is assigned the value of crc_own[7 + (8 * cycle_counter) −: 8], which selects the appropriate 8 bits from crc_own based on the cycle_counter. Finally, the cycle_counter is incremented by 1 to assign next values from crc_own array to oup array.

7. finally, m_tdata is assigned the value of oup, m_tvalid is assigned 1 if m_tdata is non−zero else 0, and s_tready is assigned as m_tready || !m_tvalid. This ensures that s_tready is high when m_tready is high or m_tvalid is low, indicating that the upstream module can send more data.

3 Test Bench Code

Diagram | axistb.v | design_1_wrapper.v

/home/sam-admin/git/Training/HLS_Vivado/A9/PART-2_RTL/codes/axistb.v

```
1  `timescale 1ns / 1ps
2
3  module axistb(
4
5      );
6      reg clk;
7      reg reset_n;
8      reg [7:0] s_tdata;
9      reg s_tlast;
10     reg s_tvalid;
11     reg m_tready;
12     wire s_tready;
13     wire [7:0] m_tdata;
14     wire m_tvalid;
15
16     // Instantiating
17    axis_reg #(
18        .N(8)
19     ) dut (
20         .clk(clk),
21         .reset_n(reset_n),
22         .s_tdata(s_tdata),
23         .s_tvalid(s_tvalid),
24         .s_tready(s_tready),
25         .s_tlast(s_tlast),
26         .m_tdata(m_tdata),
27         .m_tvalid(m_tvalid),
28         .m_tready(m_tready)
29     );
30    /*  design_1_wrapper uut
31    (.clk_0(clk),
32     .m_0_tdata(m_tdata),
33     .m_0_tvalid(m_tvalid),
34     .reset_n_0(reset_n),
35     .s_0_tdata(s_tdata),
36     .s_0_tlast(s_tlast),
37     .s_0_tready(s_tready),
38     .s_0_tvalid(s_tvalid),
39     .m_0_tready(m_tready));

40     */
41     // Clock generation
42     always #5 clk = ~clk;
43
44     initial begin
45         // Initialize inputs
46         clk = 0;
47         reset_n = 1;
48         s_tdata = 8'h00;
49         s_tvalid = 0;
50
51
52         // Apply reset
53         reset_n <= 0;
54         #10;
55         reset_n <= 1;
56         m_tready<=1;
57
58
59         // Send data and wait for it to be accepted
60         s_tdata <= 8'b01101000;
61         s_tlast <= 1'b1;
62
63         #1
64
65         s_tvalid <= 1;
66         #10;
67         s_tvalid <= 0;
68         #40
69         m_tready<=0;
70         #5
71         // Finish simulation
72         $finish;
73     end
74
75 endmodule
76
```

(a) axistb.v

4 Output Waveform

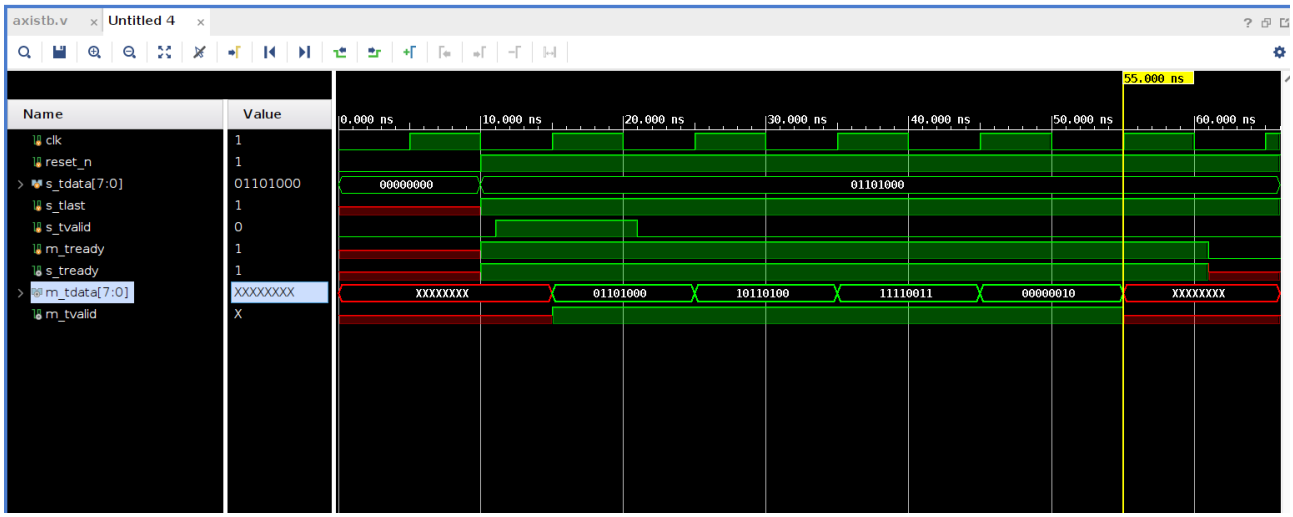


Figure 3: Output of RTL Testbench

5 Synthesis Report

```
#-----------------------------------------------------------
# Vivado v2022.2.2 (64-bit)
# SW Build 3788238 on Tue Feb 21 19:59:23 MST 2023
# IP Build 3783773 on Tue Feb 21 23:41:56 MST 2023
# Start of session at: Mon Jul 10 15:25:29 2023
# Process ID: 30364
# Current directory: /home/sam-admin/git/Training/HLS_Vivado/A9/PART-2_RTL/rtl_a9/
rtl_a9.runs/synth_1
# Command line: vivado -log design_1_wrapper.vds -product Vivado -mode batch -
messageDb vivado.pb -notrace -source design_1_wrapper.tcl
# Log file: /home/sam-admin/git/Training/HLS_Vivado/A9/PART-2_RTL/rtl_a9/
rtl_a9.runs/synth_1/design_1_wrapper.vds
# Journal file: /home/sam-admin/git/Training/HLS_Vivado/A9/PART-2_RTL/rtl_a9/
rtl_a9.runs/synth_1/vivado.jou
# Running On: sampaths-lappie, OS: Linux, CPU Frequency: 3398.075 MHz, CPU Physical
cores: 4, Host memory: 8096 MB
#-----------------------------------------------------------
source design_1_wrapper.tcl -notrace
create_project: Time (s): cpu = 00:00:05 ; elapsed = 00:00:05 . Memory (MB): peak =
1275.793 ; gain = 0.023 ; free physical = 1794 ; free virtual = 5966
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1700] Loaded user IP repository '/home/sam-admin/git/Training/
HLS_Vivado/A9/PART-2_RTL/RTL_IP'.
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/tools/Xilinx/Vivado/2022.2/
data/ip'.
Command: synth_design -top design_1_wrapper -part xczu7ev-ffvc1156-2-e
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xczu7ev'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xczu7ev'
INFO: [Device 21-403] Loading part xczu7ev-ffvc1156-2-e
INFO: [Synth 8-7079] Multithreading enabled for synth_design using a maximum of 4
```

```
processes.
INFO: [Synth 8-7078] Launching helper process for spawning children vivado
processes
INFO: [Synth 8-7075] Helper process launched with PID 30405
INFO: [Synth 8-11241] undeclared symbol 'REGCCE', assumed default net type
'wire' [/tools/Xilinx/Vivado/2022.2/data/verilog/src/unimacro/BRAM_SINGLE_MACRO.v:
2170]
---------------------------------------------------------------------------
Starting RTL Elaboration : Time (s): cpu = 00:00:04 ; elapsed = 00:00:05 . Memory
(MB): peak = 2580.367 ; gain = 241.801 ; free physical = 394 ; free virtual = 4565
Synthesis current peak Physical Memory [PSS] (MB): peak = 2057.646; parent =
1831.522; children = 226.124
Synthesis current peak Virtual Memory [VSS] (MB): peak = 3578.902; parent =
2580.371; children = 998.531
---------------------------------------------------------------------------
INFO: [Synth 8-6157] synthesizing module 'design_1_wrapper' [/home/sam-admin/git/
Training/HLS_Vivado/A9/PART-2_RTL/rtl_a9/rtl_a9.srcs/sources_1/imports/hdl/
design_1_wrapper.v:12]
INFO: [Synth 8-6157] synthesizing module 'design_1' [/home/sam-admin/git/Training/
HLS_Vivado/A9/PART-2_RTL/rtl_a9/rtl_a9.gen/sources_1/bd/design_1/synth/design_1.v:
12]
INFO: [Synth 8-6157] synthesizing module 'design_1_axis_reg_0_0' [/home/sam-admin/
git/Training/HLS_Vivado/A9/PART-2_RTL/rtl_a9/rtl_a9.runs/synth_1/.Xil/Vivado-30364-
sampaths-lappie/realtime/design_1_axis_reg_0_0_stub.v:5]
INFO: [Synth 8-6155] done synthesizing module 'design_1_axis_reg_0_0' (0#1) [/home/
sam-admin/git/Training/HLS_Vivado/A9/PART-2_RTL/rtl_a9/rtl_a9.runs/synth_1/.Xil/
Vivado-30364-sampaths-lappie/realtime/design_1_axis_reg_0_0_stub.v:5]
INFO: [Synth 8-6155] done synthesizing module 'design_1' (0#1) [/home/sam-admin/
git/Training/HLS_Vivado/A9/PART-2_RTL/rtl_a9/rtl_a9.gen/sources_1/bd/design_1/
synth/design_1.v:12]
INFO: [Synth 8-6155] done synthesizing module 'design_1_wrapper' (0#1) [/home/sam-
admin/git/Training/HLS_Vivado/A9/PART-2_RTL/rtl_a9/rtl_a9.srcs/sources_1/imports/
hdl/design_1_wrapper.v:12]
---------------------------------------------------------------------------
Finished RTL Elaboration : Time (s): cpu = 00:00:06 ; elapsed = 00:00:06 . Memory
(MB): peak = 2654.336 ; gain = 315.770 ; free physical = 463 ; free virtual = 4636
Synthesis current peak Physical Memory [PSS] (MB): peak = 2057.646; parent =
1831.522; children = 226.124
Synthesis current peak Virtual Memory [VSS] (MB): peak = 3652.871; parent =
2654.340; children = 998.531
---------------------------------------------------------------------------

---------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------

---------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:06 ; elapsed =
00:00:06 . Memory (MB): peak = 2672.148 ; gain = 333.582 ; free physical = 462 ;
free virtual = 4635
Synthesis current peak Physical Memory [PSS] (MB): peak = 2057.646; parent =
1831.522; children = 226.124
Synthesis current peak Virtual Memory [VSS] (MB): peak = 3670.684; parent =
2672.152; children = 998.531
---------------------------------------------------------------------------

---------------------------------------------------------------------------
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:06 ; elapsed = 00:00:06 .
Memory (MB): peak = 2672.148 ; gain = 333.582 ; free physical = 462 ; free virtual
= 4635
Synthesis current peak Physical Memory [PSS] (MB): peak = 2057.646; parent =
1831.522; children = 226.124
Synthesis current peak Virtual Memory [VSS] (MB): peak = 3670.684; parent =
2672.152; children = 998.531
```

```
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory
(MB): peak = 2672.148 ; gain = 0.000 ; free physical = 457 ; free virtual = 4629
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File [/home/sam-admin/git/Training/HLS_Vivado/A9/PART-2_RTL/rtl_a9/
rtl_a9.gen/sources_1/bd/design_1/ip/design_1_axis_reg_0_0/design_1_axis_reg_0_0/
design_1_axis_reg_0_0_in_context.xdc] for cell 'design_1_i/axis_reg_0'
Finished Parsing XDC File [/home/sam-admin/git/Training/HLS_Vivado/A9/PART-2_RTL/
rtl_a9/rtl_a9.gen/sources_1/bd/design_1/ip/design_1_axis_reg_0_0/
design_1_axis_reg_0_0/design_1_axis_reg_0_0_in_context.xdc] for cell 'design_1_i/
axis_reg_0'
Parsing XDC File [/home/sam-admin/git/Training/HLS_Vivado/A9/PART-2_RTL/rtl_a9/
rtl_a9.runs/synth_1/dont_touch.xdc]
Finished Parsing XDC File [/home/sam-admin/git/Training/HLS_Vivado/A9/PART-2_RTL/
rtl_a9/rtl_a9.runs/synth_1/dont_touch.xdc]
Completed Processing XDC Constraints

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory
(MB): peak = 2756.961 ; gain = 0.000 ; free physical = 403 ; free virtual = 4574
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 .
Memory (MB): peak = 2756.961 ; gain = 0.000 ; free physical = 403 ; free virtual =
4574
INFO: [Synth 8-11241] undeclared symbol 'REGCCE', assumed default net type
'wire' [/tools/Xilinx/Vivado/2022.2/data/verilog/src/unimacro/BRAM_SINGLE_MACRO.v:
2170]
---------------------------------------------------------------------------------
Finished Constraint Validation : Time (s): cpu = 00:00:12 ; elapsed = 00:00:13 .
Memory (MB): peak = 2756.961 ; gain = 418.395 ; free physical = 445 ; free virtual
= 4619
Synthesis current peak Physical Memory [PSS] (MB): peak = 2059.123; parent =
1832.999; children = 226.124
Synthesis current peak Virtual Memory [VSS] (MB): peak = 3723.480; parent =
2724.949; children = 998.531
---------------------------------------------------------------------------------

---------------------------------------------------------------------------------
Start Loading Part and Timing Information
---------------------------------------------------------------------------------
Loading part: xczu7ev-ffvc1156-2-e
INFO: [Synth 8-6742] Reading net delay rules and data
---------------------------------------------------------------------------------
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:12 ; elapsed =
00:00:13 . Memory (MB): peak = 2756.961 ; gain = 418.395 ; free physical = 445 ;
free virtual = 4619
Synthesis current peak Physical Memory [PSS] (MB): peak = 2059.123; parent =
1832.999; children = 226.124
Synthesis current peak Virtual Memory [VSS] (MB): peak = 3723.480; parent =
2724.949; children = 998.531
---------------------------------------------------------------------------------

---------------------------------------------------------------------------------
Start Applying 'set_property' XDC Constraints
---------------------------------------------------------------------------------
Applied set_property KEEP_HIERARCHY = SOFT for design_1_i. (constraint file  auto
generated constraint).
Applied set_property KEEP_HIERARCHY = SOFT for design_1_i/axis_reg_0. (constraint
file  auto generated constraint).
```

```
Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:12 ;
elapsed = 00:00:13 . Memory (MB): peak = 2756.961 ; gain = 418.395 ; free physical
= 445 ; free virtual = 4619
Synthesis current peak Physical Memory [PSS] (MB): peak = 2059.123; parent =
1832.999; children = 226.124
Synthesis current peak Virtual Memory [VSS] (MB): peak = 3723.480; parent =
2724.949; children = 998.531
```

```
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:12 ; elapsed = 00:00:13 .
Memory (MB): peak = 2756.961 ; gain = 418.395 ; free physical = 444 ; free virtual
= 4619
Synthesis current peak Physical Memory [PSS] (MB): peak = 2059.123; parent =
1832.999; children = 226.124
Synthesis current peak Virtual Memory [VSS] (MB): peak = 3723.480; parent =
2724.949; children = 998.531
```

```
Start RTL Component Statistics
```

```
Detailed RTL Component Info :
```

```
Finished RTL Component Statistics
```

```
Start Part Resource Summary
```

```
Part Resources:
DSPs: 1728 (col length:144)
BRAMs: 624 (col length: RAMB18 144 RAMB36 72)
```

```
Finished Part Resource Summary
```

```
Start Cross Boundary and Area Optimization
```

```
WARNING: [Synth 8-7080] Parallel synthesis criteria is not met
```

```
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:13 ; elapsed
= 00:00:15 . Memory (MB): peak = 2756.961 ; gain = 418.395 ; free physical = 417 ;
free virtual = 4606
Synthesis current peak Physical Memory [PSS] (MB): peak = 2059.123; parent =
1832.999; children = 226.124
Synthesis current peak Virtual Memory [VSS] (MB): peak = 3723.480; parent =
2724.949; children = 998.531
```

```
Start Applying XDC Timing Constraints
```

```
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:25 ; elapsed =
00:00:29 . Memory (MB): peak = 3217.227 ; gain = 878.660 ; free physical = 140 ;
free virtual = 4044
Synthesis current peak Physical Memory [PSS] (MB): peak = 2621.654; parent =
2398.049; children = 226.124
Synthesis current peak Virtual Memory [VSS] (MB): peak = 4215.762; parent =
3217.230; children = 998.531
```

```
Start Timing Optimization
```

Finished Timing Optimization : Time (s): cpu = 00:00:25 ; elapsed = 00:00:29 . Memory (MB): peak = 3217.227 ; gain = 878.660 ; free physical = 140 ; free virtual = 4044
Synthesis current peak Physical Memory [PSS] (MB): peak = 2621.717; parent = 2398.111; children = 226.124
Synthesis current peak Virtual Memory [VSS] (MB): peak = 4215.762; parent = 3217.230; children = 998.531

Start Technology Mapping

Finished Technology Mapping : Time (s): cpu = 00:00:25 ; elapsed = 00:00:29 . Memory (MB): peak = 3236.258 ; gain = 897.691 ; free physical = 135 ; free virtual = 4037
Synthesis current peak Physical Memory [PSS] (MB): peak = 2622.227; parent = 2398.633; children = 226.124
Synthesis current peak Virtual Memory [VSS] (MB): peak = 4234.793; parent = 3236.262; children = 998.531

Start IO Insertion

Start Flattening Before IO Insertion

Finished Flattening Before IO Insertion

Start Final Netlist Cleanup

Finished Final Netlist Cleanup

Finished IO Insertion : Time (s): cpu = 00:00:29 ; elapsed = 00:00:34 . Memory (MB): peak = 3242.195 ; gain = 903.629 ; free physical = 133 ; free virtual = 4035
Synthesis current peak Physical Memory [PSS] (MB): peak = 2622.613; parent = 2399.027; children = 226.124
Synthesis current peak Virtual Memory [VSS] (MB): peak = 4240.730; parent = 3242.199; children = 998.531

Start Renaming Generated Instances

Finished Renaming Generated Instances : Time (s): cpu = 00:00:29 ; elapsed = 00:00:34 . Memory (MB): peak = 3242.195 ; gain = 903.629 ; free physical = 133 ; free virtual = 4035
Synthesis current peak Physical Memory [PSS] (MB): peak = 2622.629; parent = 2399.043; children = 226.124
Synthesis current peak Virtual Memory [VSS] (MB): peak = 4240.730; parent = 3242.199; children = 998.531

Start Rebuilding User Hierarchy

```
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:29 ; elapsed =
00:00:34 . Memory (MB): peak = 3242.195 ; gain = 903.629 ; free physical = 133 ;
free virtual = 4035
Synthesis current peak Physical Memory [PSS] (MB): peak = 2622.645; parent =
2399.059; children = 226.124
Synthesis current peak Virtual Memory [VSS] (MB): peak = 4240.730; parent =
3242.199; children = 998.531
```

```
Start Renaming Generated Ports
```

```
Finished Renaming Generated Ports : Time (s): cpu = 00:00:29 ; elapsed = 00:00:34 .
Memory (MB): peak = 3242.195 ; gain = 903.629 ; free physical = 133 ; free virtual
= 4035
Synthesis current peak Physical Memory [PSS] (MB): peak = 2622.707; parent =
2399.121; children = 226.124
Synthesis current peak Virtual Memory [VSS] (MB): peak = 4240.730; parent =
3242.199; children = 998.531
```

```
Start Handling Custom Attributes
```

```
Finished Handling Custom Attributes : Time (s): cpu = 00:00:29 ; elapsed =
00:00:34 . Memory (MB): peak = 3242.195 ; gain = 903.629 ; free physical = 133 ;
free virtual = 4035
Synthesis current peak Physical Memory [PSS] (MB): peak = 2622.707; parent =
2399.121; children = 226.124
Synthesis current peak Virtual Memory [VSS] (MB): peak = 4240.730; parent =
3242.199; children = 998.531
```

```
Start Renaming Generated Nets
```

```
Finished Renaming Generated Nets : Time (s): cpu = 00:00:29 ; elapsed = 00:00:34 .
Memory (MB): peak = 3242.195 ; gain = 903.629 ; free physical = 133 ; free virtual
= 4035
Synthesis current peak Physical Memory [PSS] (MB): peak = 2622.723; parent =
2399.137; children = 226.124
Synthesis current peak Virtual Memory [VSS] (MB): peak = 4240.730; parent =
3242.199; children = 998.531
```

```
Start Writing Synthesis Report
```

```
Report BlackBoxes:
+------+-----------------------+----------+
|      |BlackBox name          |Instances |
+------+-----------------------+----------+
|1     |design_1_axis_reg_0_0  |         1|
+------+-----------------------+----------+

Report Cell Usage:
+------+---------------------+------+
|      |Cell                 |Count |
+------+---------------------+------+
|1     |design_1_axis_reg_0  |     1|
|2     |IBUF                 |    13|
```

```
|3      |OBUF                 |     10|
+-------+---------------------+-------+
```

```
Finished Writing Synthesis Report : Time (s): cpu = 00:00:29 ; elapsed = 00:00:34 .
Memory (MB): peak = 3242.195 ; gain = 903.629 ; free physical = 133 ; free virtual
= 4035
Synthesis current peak Physical Memory [PSS] (MB): peak = 2622.773; parent =
2399.188; children = 226.124
Synthesis current peak Virtual Memory [VSS] (MB): peak = 4240.730; parent =
3242.199; children = 998.531
```

```
Synthesis finished with 0 errors, 0 critical warnings and 1 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:27 ; elapsed = 00:00:32 .
Memory (MB): peak = 3242.195 ; gain = 818.816 ; free physical = 165 ; free virtual
= 4067
Synthesis Optimization Complete : Time (s): cpu = 00:00:29 ; elapsed = 00:00:34 .
Memory (MB): peak = 3242.203 ; gain = 903.629 ; free physical = 165 ; free virtual
= 4066
INFO: [Project 1-571] Translating synthesized netlist
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory
(MB): peak = 3249.133 ; gain = 0.000 ; free physical = 162 ; free virtual = 4064
INFO: [Netlist 29-17] Analyzing 13 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory
(MB): peak = 3275.883 ; gain = 0.000 ; free physical = 204 ; free virtual = 4108
INFO: [Project 1-111] Unisim Transformation Summary:
  A total of 13 instances were transformed.
  IBUF => IBUF (IBUFCTRL, INBUF): 13 instances

Synth Design complete, checksum: 96e7c2a8
INFO: [Common 17-83] Releasing license: Synthesis
26 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:38 ; elapsed = 00:00:42 . Memory (MB): peak =
3275.883 ; gain = 1969.121 ; free physical = 400 ; free virtual = 4304
INFO: [Common 17-1381] The checkpoint '/home/sam-admin/git/Training/HLS_Vivado/A9/
PART-2_RTL/rtl_a9/rtl_a9.runs/synth_1/design_1_wrapper.dcp' has been generated.
INFO: [runtcl-4] Executing : report_utilization -file
design_1_wrapper_utilization_synth.rpt -pb design_1_wrapper_utilization_synth.pb
INFO: [Common 17-206] Exiting Vivado at Mon Jul 10 15:26:23 2023...
```

6 Resource Utilization

```
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```

```
| Tool Version : Vivado v.2022.2.2 (lin64) Build 3788238 Tue Feb 21 19:59:23 MST
2023
| Date         : Mon Jul 10 15:26:23 2023
| Host         : sampaths-lappie running 64-bit Ubuntu 22.04.2 LTS
| Command      : report_utilization -file design_1_wrapper_utilization_synth.rpt -
pb design_1_wrapper_utilization_synth.pb
| Design       : design_1_wrapper
| Device       : xczu7ev-ffvc1156-2-e
| Speed File   : -2
| Design State : Synthesized
```

Utilization Design Information

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1. CLB Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
CLB LUTs*	0	0	0	230400	0.00
LUT as Logic	0	0	0	230400	0.00
LUT as Memory	0	0	0	101760	0.00
CLB Registers	0	0	0	460800	0.00
Register as Flip Flop	0	0	0	460800	0.00
Register as Latch	0	0	0	460800	0.00
CARRY8	0	0	0	28800	0.00
F7 Muxes	0	0	0	115200	0.00
F8 Muxes	0	0	0	57600	0.00
F9 Muxes	0	0	0	28800	0.00

* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.
Warning! LUT value is adjusted to account for LUT combining.

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	-	-	-
0	-	-	Set
0	-	-	Reset
0	-	Set	-
0	-	Reset	-
0	Yes	-	-
0	Yes	-	Set
0	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. BLOCKRAM

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	312	0.00
RAMB36/FIFO*	0	0	0	312	0.00
RAMB18	0	0	0	624	0.00
URAM	0	0	0	96	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E2 or one FIFO18E2. However, if a FIFO18E2 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E2

3. ARITHMETIC

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	0	0	0	1728	0.00

4. I/O

Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB	23	0	0	360	6.39

5. CLOCK

Site Type	Used	Fixed	Prohibited	Available	Util%
GLOBAL CLOCK BUFFERs	0	0	0	544	0.00
BUFGCE	0	0	0	208	0.00
BUFGCE_DIV	0	0	0	32	0.00
BUFG_GT	0	0	0	144	0.00
BUFG_PS	0	0	0	96	0.00
BUFGCTRL*	0	0	0	64	0.00
PLL	0	0	0	16	0.00
MMCM	0	0	0	8	0.00

* Note: Each used BUFGCTRL counts as two GLOBAL CLOCK BUFFERs. This table does not include global clocking resources, only buffer cell usage. See the Clock Utilization Report (report_clock_utilization) for detailed accounting of global clocking resource availability.

6. ADVANCED

Site Type	Used	Fixed	Prohibited	Available	Util%

GTHE4_CHANNEL	0	0	0	20	0.00
GTHE4_COMMON	0	0	0	5	0.00
OBUFDS_GTE4	0	0	0	10	0.00
OBUFDS_GTE4_ADV	0	0	0	10	0.00
PCIE40E4	0	0	0	2	0.00
PS8	0	0	0	1	0.00
SYSMONE4	0	0	0	1	0.00
VCU	0	0	0	1	0.00

7. CONFIGURATION

Site Type	Used	Fixed	Prohibited	Available	Util%
BSCANE2	0	0	0	4	0.00
DNA_PORTE2	0	0	0	1	0.00
EFUSE_USR	0	0	0	1	0.00
FRAME_ECCE4	0	0	0	1	0.00
ICAPE3	0	0	0	2	0.00
MASTER_JTAG	0	0	0	1	0.00
STARTUPE3	0	0	0	1	0.00

8. Primitives

Ref Name	Used	Functional Category
INBUF	13	I/O
IBUFCTRL	13	Others
OBUF	10	I/O

9. Black Boxes

Ref Name	Used
design_1_axis_reg_0_0	1

7 Block Design

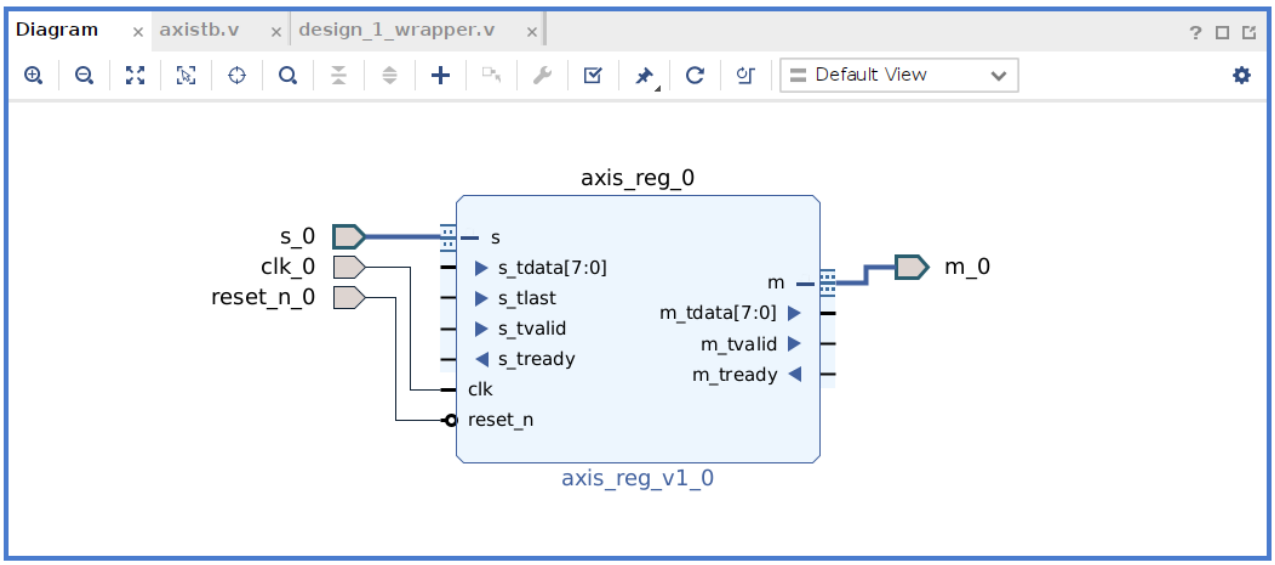

Figure 4: Block Diagram

8 Verilog Testbench

Diagram × axistb.v × design_1_wrapper.v ×

/home/sam-admin/git/Training/HLS_Vivado/A9/PART-2_RTL/codes/axistb.v

```
1  `timescale 1ns / 1ps
2
3  module axistb(
4
5      );
6      reg clk;
7      reg reset_n;
8      reg [7:0] s_tdata;
9      reg s_tlast;
10     reg s_tvalid;
11     reg m_tready;
12     wire s_tready;
13     wire [7:0] m_tdata;
14     wire m_tvalid;
15
16     // Instantiating
17 /*  axis_reg #(
18         .N(8)
19     ) dut (
20         .clk(clk),
21         .reset_n(reset_n),
22         .s_tdata(s_tdata),
23         .s_tvalid(s_tvalid),
24         .s_tready(s_tready),
25         .s_tlast(s_tlast),
26         .m_tdata(m_tdata),
27         .m_tvalid(m_tvalid),
28         .m_tready(m_tready)
29     );*/
30      design_1_wrapper uut
31    (.clk_0(clk),
32     .m_0_tdata(m_tdata),
33     .m_0_tvalid(m_tvalid),
34     .reset_n_0(reset_n),
35     .s_0_tdata(s_tdata),
36     .s_0_tlast(s_tlast),
37     .s_0_tready(s_tready),
38     .s_0_tvalid(s_tvalid),
39     .m_0_tready(m_tready));
40
41     // Clock generation
42     always #5 clk = ~clk;
43
44     initial begin
45         // Initialize inputs
46         clk = 0;
47         reset_n = 1;
48         s_tdata = 8'h00;
49         s_tvalid = 0;
50
51
52         // Apply reset
53         reset_n <= 0;
54         #10;
55         reset_n <= 1;
56         m_tready<=1;
57
58
59         // Send data and wait for it to be accepted
60         s_tdata <= 8'b01101000;
61         s_tlast <= 1'b1;
62
63         #1
64
65         s_tvalid <= 1;
66         #10;
67         s_tvalid <= 0;
68         #40
69         m_tready<=0;
70         #5
71         // Finish simulation
72         $finish;
73     end
74
75 endmodule
76
```

(a) axistb.v

9 Output Waveform

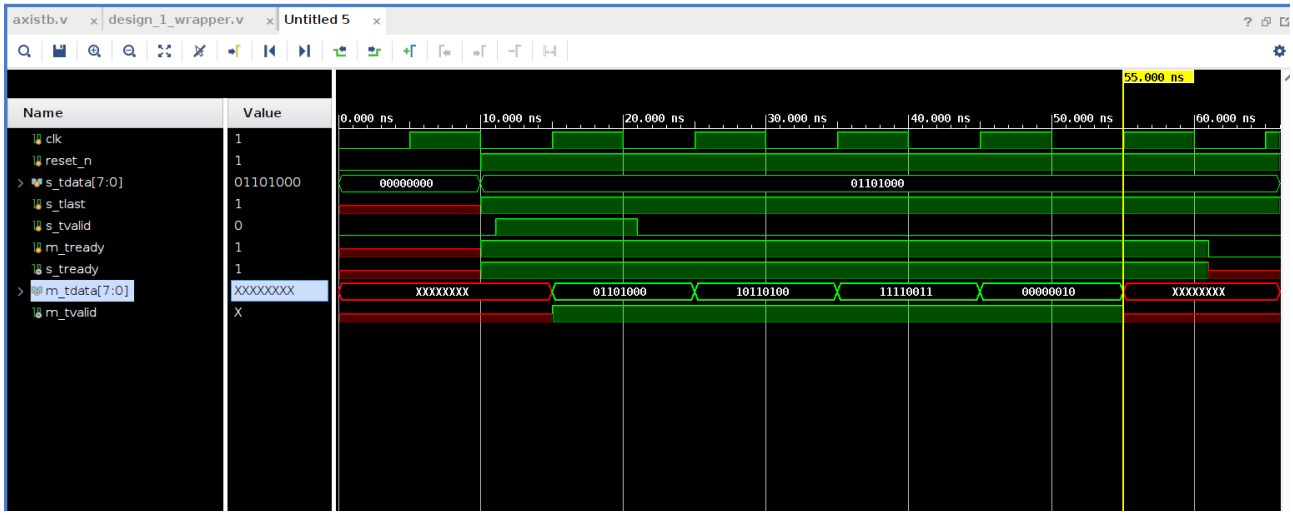

Figure 6: Output of IP Testbench

10 Matlab Reference

Figure 7: Matlab Reference

11 Conclusion

The Output of CRC IP in both PART–1 and Part–2 is matching with Output of reference Matlab code and also using this floating Point Converter Online :

https://www.h-schmidt.net/FloatConverter/IEEE754.html

GITHUB : https://github.com/dk-425/Training.git