Problem Statement: Sampath Govardhan

Design a digital circuit using RTL and HLS for a 5G NR CRC bits generator.

🎯 Requirements

- Refer to the 5.1 section in this document for the mathematical expressions of the CRC bits generation.
- The module should process 8 bits per clock cycle.
- The input and output buses should use the AXIS interface.
- Implement a pipelined design.
- The implementation should use as minimum resources as possible.

💼 Considerations

- Implement the module only for CRC24A
- A last signal should be used to indicate the end of the input bit stream.
- The design implementation should be targeted on the ZCU111 FPGA board.

🚚 Deliverables

- Source code implementation of the design.
- Simulation results.
- Resource utilization report analysis.
- Timing report which contains the latency, interval, throughput and the Fmax of the circuit.
- Documentation detailing the design choices, and performance evaluation.