Vivado/HLS Assignment

Due by: September 12, 2019

The purpose of this assignment is to familiarise you with the Vivado and HLS flow.

General Instructions:

1. Read about Cyclic Prefix removal in 5G NR from the PDF (pg. 11) attached with this mail.
2. Write an HLS module, along with testbench, for Cyclic Prefix removal from an incoming set of data inputs.
3. After HLS testing using HLS testbench and synthesis of the module in HLS, export the module to Vivado application.
4. The input to the CP removal module should be given from another HLS module which will act as a data generator. Use an array to store the input values from the attached data set file in the mail and perform synthesis in HLS to get the data generator module.
5. Interface both the modules with Xilinx FFT IP and perform FFT on the output of Cyclic Prefix Removal in the Vivado application.
6. Generate a wrapper for the block diagram in Vivado and then write a test bench in Verilog which will provide clock and reset to these modules and store the FFT output in a file.
7. Run simulation.
8. Compare the output obtained from Verilog by writing a code in MATLAB for the same functionality and check for correctness.

Vivado/HLS Guidelines:

1. Use AXI streaming interface for the input and output ports of all your modules.
2. Use three data files in HLS testbenches that you use: input, output and reference output.
    a. Input for reading inputs.
    b. Output for storing the generated outputs.
    c. Reference outputs for finding the error and for deciding if it's tolerable based on the precision required. Take 10e-3 as precision required.
3. Go through UG902 Vivado HLS user guide if you have any doubts regarding HLS.
4. Go through UG893 Vivado user guide if you have any doubts regarding Vivado.
5. Go through PG109 Xilinx FFT IP guide if you have any doubts regarding FFT IP.
6. Use Google if you have any other doubts.

Configuration for the System:

1. *Total number of symbols: 2;*
2. *First symbol CP length: 320;*
3. *Second symbol CP length: 288;*
4. *CP Input length for first symbol: 4096+320;*
5. *CP Input length for second symbol: 4096+288;*
6. *CP Output length for both the symbols: 4096;*
7. *FFT Input length: 4096;*
8. *FFT Output length: 4096;*