HLS-Assignment 2.3

March 21, 2023

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FWC22071

Contents

1 Problem Statement

Repeat the experiment in Assignment 1 with the following change:
Repeat Assignment 2.1 and 2.2 with the change mentioned in Assignment 3. Analyse change in timing report from Assignment 1, 2.1, 2.2, and report your understanding of why it changed.

2 Design Code

2.3.1

```
#include <iostream>
#include "hls_stream.h"


typedef int in;
typedef long out;

void mul(hls::stream<in> &x, hls::stream<in> &y, hls::stream<out> &z)
{

 in a,b;
 out c;
 a=x.read();
 b=y.read();
 c = a * b;
 z.write(c);
}
```

2.3.2

```
#include <iostream>
#include "hls_stream.h"
#include "ap_fixed.h"

typedef ap_fixed<28,4> in;
typedef ap_fixed<56,8> out;

void mul(hls::stream<in> &x, hls::stream<in> &y, hls::stream<out> &z)
{

 in a,b;
 out c;
 a=x.read();
 b=y.read();
 c = a * b;
 z.write(c);
}
```

3 Test Bench Code

2.3.1

```
#include <iostream>
#include "hls_stream.h"

using namespace std;

typedef int in;
typedef long out;

void mul(hls::stream<in> &x, hls::stream<in> &y, hls::stream<out> &z);
int main()
{
hls::stream<in> a,b;
hls::stream<out> c;

int i;

for (i=0;i<=9;i++){
a.write (i+1);
b.write (i+3);
mul(a,b,c);
cout << "\n" << c.read();
}
return 0;
}
```

2.3.2

```
#include <iostream>
#include "hls_stream.h"
#include "ap_fixed.h"
using namespace std;

typedef ap_fixed<28,4> in;
typedef ap_fixed<56,8> out;

void mul(hls::stream<in> &x, hls::stream<in> &y, hls::stream<out> &z);
int main()
{
hls::stream<in> a,b;
```

```
hls::stream<out> c;

int i;

for (i=0;i<=9;i++){
a.write (i+0.456789875);
b.write (i);
mul(a,b,c);
cout << "\n" << c.read();
}
return 0;
}
```

4 C Simulation Output

2.3.1

```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../../cpp_ap_fixed.cpp in debug mode
   Generating csim.exe

3
8
15
24
35
48
63
80
99
120
INFO: [SIM 1] CSim done with 0 errors.
```

```
INFO: [SIM 3] *************** CSIM finish ***************
```

2.3.2

```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../../cpp_ap_fixed_test.cpp in debug mode
   Generating csim.exe

0
1.45679
4.91358
10.3704
17.8272
27.2839
38.7407
52.1975
60.3457
45.8025
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************
```

5 HLS Resource Consumption

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	3	0	22
FIFO	-	-	-	-
Instance	-	-	-	-
Memory	-	-	-	-
Multiplexer	-	-	-	48
Register	-	-	99	-
Total	0	3	99	70
Available	280	220	106400	53200
Utilization (%)	0	1	~0	~0

(a) 3.2.1

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	4	0	38
FIFO	-	-	-	-
Instance	-	-	-	-
Memory	-	-	-	-
Multiplexer	-	-	-	48
Register	-	-	115	-
Total	0	4	115	86
Available	280	220	106400	53200
Utilization (%)	0	1	~0	~0

(b) 3.2.2

Here more resources are used compared to all previous Assignments this is because by using Streaming Interfaces we use single master and single slave at a time to transmit or recieve data in a serial manner (Serial Communication).

6 HLS Timing Report

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.510	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
2	2	2	2	none

Detail

(a) 3.2.1

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	7.447	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
2	2	2	2	none

Detail

(b) 3.2.2

Here Timing remains same but Latency is changed compared to all previous Assignments this is because by using Streaming Interfaces we changed our Combinational logic into a Sequential logic thus takes 1 clock cycle to produce overall output.

7 Interfaces Report

Interface

Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	mul	return value
ap_rst	in	1	ap_ctrl_hs	mul	return value
ap_start	in	1	ap_ctrl_hs	mul	return value
ap_done	out	1	ap_ctrl_hs	mul	return value
ap_idle	out	1	ap_ctrl_hs	mul	return value
ap_ready	out	1	ap_ctrl_hs	mul	return value
x_V_dout	in	32	ap_fifo	x_V	pointer
x_V_empty_n	in	1	ap_fifo	x_V	pointer
x_V_read	out	1	ap_fifo	x_V	pointer
y_V_dout	in	32	ap_fifo	y_V	pointer
y_V_empty_n	in	1	ap_fifo	y_V	pointer
y_V_read	out	1	ap_fifo	y_V	pointer
z_V_din	out	64	ap_fifo	z_V	pointer
z_V_full_n	in	1	ap_fifo	z_V	pointer
z_V_write	out	1	ap_fifo	z_V	pointer

(a) 3.2.1

Interface

Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	mul	return value
ap_rst	in	1	ap_ctrl_hs	mul	return value
ap_start	in	1	ap_ctrl_hs	mul	return value
ap_done	out	1	ap_ctrl_hs	mul	return value
ap_idle	out	1	ap_ctrl_hs	mul	return value
ap_ready	out	1	ap_ctrl_hs	mul	return value
x_V_V_dout	in	28	ap_fifo	x_V_V	pointer
x_V_V_empty_n	in	1	ap_fifo	x_V_V	pointer
x_V_V_read	out	1	ap_fifo	x_V_V	pointer
y_V_V_dout	in	28	ap_fifo	y_V_V	pointer
y_V_V_empty_n	in	1	ap_fifo	y_V_V	pointer
y_V_V_read	out	1	ap_fifo	y_V_V	pointer
z_V_V_din	out	56	ap_fifo	z_V_V	pointer
z_V_V_full_n	in	1	ap_fifo	z_V_V	pointer
z_V_V_write	out	1	ap_fifo	z_V_V	pointer

(b) 3.2.2

8 C/RTL Cosimulation Output

2.3.1

```
Starting C/RTL cosimulation ...
/tools/Xilinx/Vivado/2018.3/bin/vivado_hls /home/sam-admin/Xilinx/HLS/cpp_ap_fix
INFO: [HLS 200-10] Running '/tools/Xilinx/Vivado/2018.3/bin/unwrapped/lnx64.o/vi
INFO: [HLS 200-10] For user 'sam-admin' on host 'sampaths-lappie' (Linux_x86_64
INFO: [HLS 200-10] On os Ubuntu 22.04.2 LTS
INFO: [HLS 200-10] In directory '/home/sam-admin/Xilinx/HLS/cpp_ap_fixed'
INFO: [HLS 200-10] Opening project '/home/sam-admin/Xilinx/HLS/cpp_ap_fixed/proj
INFO: [HLS 200-10] Opening solution '/home/sam-admin/Xilinx/HLS/cpp_ap_fixed/pro
INFO: [SYN 201-201] Setting up clock 'default' with a period of 10ns.
INFO: [HLS 200-10] Setting target device to 'xc7z020clg484-1'
INFO: [COSIM 212-47] Using XSIM for RTL simulation.
INFO: [COSIM 212-14] Instrumenting C test bench ...
   Build using "/tools/Xilinx/Vivado/2018.3/tps/lnx64/gcc-6.2.0/bin/g++"
   Compiling apatb_mul.cpp
   Compiling cpp_ap_fixed.cpp_pre.cpp.tb.cpp
   Compiling cpp_ap_fixed_test.cpp_pre.cpp.tb.cpp
   Generating cosim.tv.exe
INFO: [COSIM 212-302] Starting C TB testing ...


3
8
15
24
35
48
63
80
99
120INFO: [COSIM 212-333] Generating C post check test bench ...
INFO: [COSIM 212-12] Generating RTL test bench ...
INFO: [COSIM 212-323] Starting verilog simulation.
INFO: [COSIM 212-15] Starting XSIM ...
INFO: [XSIM 43-3496] Using init file passed via -initfile option "/tools/Xilinx/
Vivado Simulator 2018.3
Copyright 1986-1999, 2001-2018 Xilinx, Inc. All Rights Reserved.
Running: /tools/Xilinx/Vivado/2018.3/bin/unwrapped/lnx64.o/xelab xil_defaultlib.
Multi-threading is on. Using 6 slave threads.
```

```
WARNING: [XSIM 43-3431] One or more environment variables have been detected whi
If errors occur, try running xelab with the "-mt off -v 1" switches to see more
    LIBRARY_PATH
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/Xilinx/HLS/cp
INFO: [VRFC 10-311] analyzing module glbl
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/Xilinx/HLS/cp
INFO: [VRFC 10-311] analyzing module AESL_autofifo_y_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/Xilinx/HLS/cp
INFO: [VRFC 10-311] analyzing module mul
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/Xilinx/HLS/cp
INFO: [VRFC 10-311] analyzing module AESL_autofifo_x_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/Xilinx/HLS/cp
INFO: [VRFC 10-311] analyzing module AESL_autofifo_z_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/Xilinx/HLS/cp
INFO: [VRFC 10-311] analyzing module apatb_mul_top
Starting static elaboration
Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module xil_defaultlib.mul
Compiling module xil_defaultlib.AESL_autofifo_x_V
Compiling module xil_defaultlib.AESL_autofifo_y_V
Compiling module xil_defaultlib.AESL_autofifo_z_V
Compiling module xil_defaultlib.apatb_mul_top
Compiling module work.glbl
Built simulation snapshot mul


****** Webtalk v2018.3 (64-bit)
  **** SW Build 2405991 on Thu Dec  6 23:36:41 MST 2018
  **** IP Build 2404404 on Fri Dec  7 01:43:56 MST 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.


source /home/sam-admin/Xilinx/HLS/cpp_ap_fixed/proj_cpp_ap_fixed/solution1/sim/v
webtalk_transmit: Time (s): cpu = 00:00:00.58 ; elapsed = 00:00:06 . Memory (MB)
INFO: [Common 17-206] Exiting Webtalk at Tue Mar 21 15:44:25 2023...


****** xsim v2018.3 (64-bit)
  **** SW Build 2405991 on Thu Dec  6 23:36:41 MST 2018
  **** IP Build 2404404 on Fri Dec  7 01:43:56 MST 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.
```

```
source xsim.dir/mul/xsim_script.tcl
# xsim {mul} -autoloadwcfg -tclbatch {mul.tcl}
Vivado Simulator 2018.3
Time resolution is 1 ps
source mul.tcl
## run all
////////////////////////////////////////////////////////////////////////////////
// Inter-Transaction Progress: Completed Transaction / Total Transaction
// Intra-Transaction Progress: Measured Latency / Latency Estimation * 100%
//
// RTL Simulation : "Inter-Transaction Progress" ["Intra-Transaction Progress"] @
////////////////////////////////////////////////////////////////////////////////
// RTL Simulation : 0 / 10 [0.00%] @ "125000"
// RTL Simulation : 1 / 10 [100.00%] @ "165000"
// RTL Simulation : 2 / 10 [100.00%] @ "195000"
// RTL Simulation : 3 / 10 [100.00%] @ "225000"
// RTL Simulation : 4 / 10 [100.00%] @ "255000"
// RTL Simulation : 5 / 10 [100.00%] @ "285000"
// RTL Simulation : 6 / 10 [100.00%] @ "315000"
// RTL Simulation : 7 / 10 [100.00%] @ "345000"
// RTL Simulation : 8 / 10 [100.00%] @ "375000"
// RTL Simulation : 9 / 10 [100.00%] @ "405000"
// RTL Simulation : 10 / 10 [100.00%] @ "435000"
////////////////////////////////////////////////////////////////////////////////
$finish called at time : 475 ns : File "/home/sam-admin/Xilinx/HLS/cpp_ap_fixed/
## quit
INFO: [Common 17-206] Exiting xsim at Tue Mar 21 15:44:33 2023...
INFO: [COSIM 212-316] Starting C post checking ...


3
8
15
24
35
48
63
80
99
120INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***
Finished C/RTL cosimulation.
```

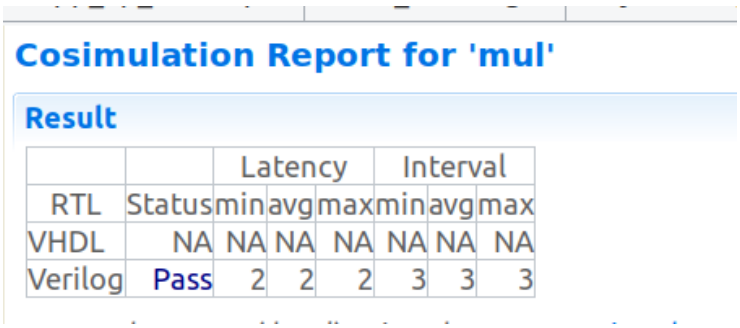
2.3.2

```
Starting C/RTL cosimulation ...
/tools/Xilinx/Vivado/2018.3/bin/vivado_hls /home/sam-admin/Xilinx/HLS/cpp_ap_fix
INFO: [HLS 200-10] Running '/tools/Xilinx/Vivado/2018.3/bin/unwrapped/lnx64.o/vi
INFO: [HLS 200-10] For user 'sam-admin' on host 'sampaths-lappie' (Linux_x86_64
INFO: [HLS 200-10] On os Ubuntu 22.04.2 LTS
INFO: [HLS 200-10] In directory '/home/sam-admin/Xilinx/HLS/cpp_ap_fixed'
INFO: [HLS 200-10] Opening project '/home/sam-admin/Xilinx/HLS/cpp_ap_fixed/proj
INFO: [HLS 200-10] Opening solution '/home/sam-admin/Xilinx/HLS/cpp_ap_fixed/pro
INFO: [SYN 201-201] Setting up clock 'default' with a period of 10ns.
INFO: [HLS 200-10] Setting target device to 'xc7z020clg484-1'
INFO: [COSIM 212-47] Using XSIM for RTL simulation.
INFO: [COSIM 212-14] Instrumenting C test bench ...
   Build using "/tools/Xilinx/Vivado/2018.3/tps/lnx64/gcc-6.2.0/bin/g++"
   Compiling apatb_mul.cpp
   Compiling cpp_ap_fixed.cpp_pre.cpp.tb.cpp
   Compiling cpp_ap_fixed_test.cpp_pre.cpp.tb.cpp
   Generating cosim.tv.exe
INFO: [COSIM 212-302] Starting C TB testing ...


0
1.45679
4.91358
10.3704
17.8272
27.2839
38.7407
52.1975
60.3457
45.8025INFO: [COSIM 212-333] Generating C post check test bench ...
INFO: [COSIM 212-12] Generating RTL test bench ...
INFO: [COSIM 212-323] Starting verilog simulation.
INFO: [COSIM 212-15] Starting XSIM ...
INFO: [XSIM 43-3496] Using init file passed via -initfile option "/tools/Xilinx/
Vivado Simulator 2018.3
Copyright 1986-1999, 2001-2018 Xilinx, Inc. All Rights Reserved.
Running: /tools/Xilinx/Vivado/2018.3/bin/unwrapped/lnx64.o/xelab xil_defaultlib.
Multi-threading is on. Using 6 slave threads.
WARNING: [XSIM 43-3431] One or more environment variables have been detected whi
If errors occur, try running xelab with the "-mt off -v 1" switches to see more
    LIBRARY_PATH
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/Xilinx/HLS/cp
```

```
INFO: [VRFC 10-311] analyzing module glbl
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/Xilinx/HLS/cp
INFO: [VRFC 10-311] analyzing module AESL_autofifo_y_V_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/Xilinx/HLS/cp
INFO: [VRFC 10-311] analyzing module mul
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/Xilinx/HLS/cp
INFO: [VRFC 10-311] analyzing module AESL_autofifo_x_V_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/Xilinx/HLS/cp
INFO: [VRFC 10-311] analyzing module apatb_mul_top
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/Xilinx/HLS/cp
INFO: [VRFC 10-311] analyzing module AESL_autofifo_z_V_V
Starting static elaboration
Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module xil_defaultlib.mul
Compiling module xil_defaultlib.AESL_autofifo_x_V_V
Compiling module xil_defaultlib.AESL_autofifo_y_V_V
Compiling module xil_defaultlib.AESL_autofifo_z_V_V
Compiling module xil_defaultlib.apatb_mul_top
Compiling module work.glbl
Built simulation snapshot mul


****** Webtalk v2018.3 (64-bit)
  **** SW Build 2405991 on Thu Dec  6 23:36:41 MST 2018
  **** IP Build 2404404 on Fri Dec  7 01:43:56 MST 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.


source /home/sam-admin/Xilinx/HLS/cpp_ap_fixed/proj_cpp_ap_fixed/solution1/sim/v
INFO: [Common 17-206] Exiting Webtalk at Tue Mar 21 15:52:52 2023...


****** xsim v2018.3 (64-bit)
  **** SW Build 2405991 on Thu Dec  6 23:36:41 MST 2018
  **** IP Build 2404404 on Fri Dec  7 01:43:56 MST 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.


source xsim.dir/mul/xsim_script.tcl
# xsim {mul} -autoloadwcfg -tclbatch {mul.tcl}
Vivado Simulator 2018.3
Time resolution is 1 ps
source mul.tcl
```

```
## run all
////////////////////////////////////////////////////////////////////////////////
// Inter-Transaction Progress: Completed Transaction / Total Transaction
// Intra-Transaction Progress: Measured Latency / Latency Estimation * 100%
//
// RTL Simulation : "Inter-Transaction Progress" ["Intra-Transaction Progress"] (
////////////////////////////////////////////////////////////////////////////////
// RTL Simulation : 0 / 10 [0.00%] @ "125000"
// RTL Simulation : 1 / 10 [100.00%] @ "165000"
// RTL Simulation : 2 / 10 [100.00%] @ "195000"
// RTL Simulation : 3 / 10 [100.00%] @ "225000"
// RTL Simulation : 4 / 10 [100.00%] @ "255000"
// RTL Simulation : 5 / 10 [100.00%] @ "285000"
// RTL Simulation : 6 / 10 [100.00%] @ "315000"
// RTL Simulation : 7 / 10 [100.00%] @ "345000"
// RTL Simulation : 8 / 10 [100.00%] @ "375000"
// RTL Simulation : 9 / 10 [100.00%] @ "405000"
// RTL Simulation : 10 / 10 [100.00%] @ "435000"
////////////////////////////////////////////////////////////////////////////////
$finish called at time : 475 ns : File "/home/sam-admin/Xilinx/HLS/cpp_ap_fixed/
## quit
INFO: [Common 17-206] Exiting xsim at Tue Mar 21 15:53:00 2023...
INFO: [COSIM 212-316] Starting C post checking ...


0
1.45679
4.91358
10.3704
17.8272
27.2839
38.7407
52.1975
60.3457
45.8025INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***
Finished C/RTL cosimulation.
```

9 C/RTL Cosimulation Report

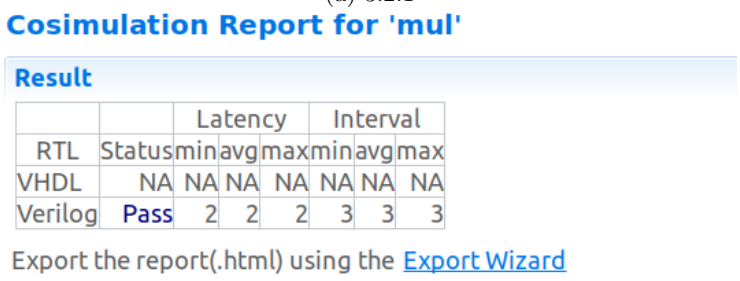


Cosimulation Report for 'mul'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	2	2	2	3	3	3

(a) 3.2.1



Cosimulation Report for 'mul'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	2	2	2	3	3	3

Export the report(.html) using the Export Wizard

(b) 3.2.2