HLS-Assignment 5A

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Sampath Govardhan
FWC22071

1 Problem Statement

Implement a DUT that accesses 8 elements from BRAM (the BRAM should be contained within the DUT, you can choose to populate the BRAM in any way you like) and gives out all 8 values as HLS streaming output in a single bundle in a single clock cycle. The starting index will be an input to the DUT and it will be a multiple of 8.

The way to access these 8 elements are as follows:

1. 8 consecutive elements are to be chosen and these elements will make up a bundle.
2. Every 8th element is to be chosen and 8 such elements will make up a bundle.

2 Design Code

5.1

```
#include "hls_stream.h"
#include "ap_int.h"
//#include "ap_axi_sdata.h"

typedef ap_uint<8> in;

struct bundle{
in data[8];
};


void a5a(int index,hls::stream<bundle> &output){

in bram[64]={0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,
22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42,43,44,45,46,47,48
49,50,51,52,53,54,55,56,57,58,59,60,61,62,63};

#pragma HLS RESOURCE variable=bram core=RAM_1P_BRAM
#pragma HLS ARRAY_PARTITION variable=bram cyclic factor=8 dim=1

bundle out={bram[index],bram[index+1],bram[index+2],bram[index+3],bram[index+4],
                bram[index+5],bram[index+6],bram[index+7]};
output.write(out);
}
```

5.2

```
#include "hls_stream.h"
#include "ap_int.h"
//#include "ap_axi_sdata.h"

typedef ap_uint<8> in;

struct bundle{
in data[8];
};


void a5a(int index,hls::stream<bundle> &output){

in bram[64]={0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,
22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42,43,44,45,46,47,48
49,50,51,52,53,54,55,56,57,58,59,60,61,62,63};

#pragma HLS RESOURCE variable=bram core=RAM_1P_BRAM
#pragma HLS ARRAY_PARTITION variable=bram block factor=8 dim=1

bundle out={bram[index],bram[index+8],bram[index+16],bram[index+24],bram[index+3
                bram[index+40],bram[index+48],bram[index+56]};
output.write(out);
}
```

3 Test Bench Code

5.1 and 5.2

```
#include <fstream>
#include "hls_stream.h"
#include "ap_int.h"
using namespace std;

typedef ap_uint<8> in;

struct bundle{
in data[8];
};

void a5a(int index,hls::stream<bundle> &output);

int main(){
hls::stream<bundle> out_stream;
int index,a,b,c,d,e,f,g,h;
bool fail=0;

ifstream ref("in.dat");
ofstream res("out.dat");

for (int i=0;i<8;i++){
        ref>>index>>a>>b>>c>>d>>e>>f>>g>>h;
a5a(index,out_stream);
bundle out=out_stream.read();
for (int j=0;j<8;j++){
res<<out.data[j]<<" ";
}
if (out.data[0]==a && out.data[1]==b && out.data[2]==c &&
out.data[3]==d && out.data[4]==e && out.data[5]==f && out.data[6]==g &&
out.data[7]==h ){
res<<"Pass"<<endl;
}
else{
res<<"Fail"<<endl;
fail=1;
}
}
ref.close();
res.close();
if (fail==0){
```

```
cout<<"ALL THE TEST CASES ARE PASSED!"<<endl;
}
else{
cout<<"ERROR! ALL THE TEST CASES ARE NOT PASSED!"<<endl;
}}
```

4 C Simulation Output

5.1

```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../../a5a_tb.cpp in debug mode
   Generating csim.exe
ALL THE TEST CASES ARE PASSED!
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************
```

5.2

```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../../a5a_tb.cpp in debug mode
   Compiling ../../../../a51a.cpp in debug mode
   Generating csim.exe
ALL THE TEST CASES ARE PASSED!
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************
```

5 C code for in.dat file

5.1

```
#include <stdio.h>
#include <stdlib.h>

int main() {
    int a,b,c,d,e,f,g,h;
    int op,i;

    FILE *fp;
    fp=fopen("in.dat","w");
    for (int j=0;j<8;j++){
    i=j*8;
    a=i;
    b=i+1;
    c=i+2;
    d=i+3;                                  //for 5.1
    e=i+4;
    f=i+5;
    g=i+6;
    h=i+7;
    op=i;

   fprintf(fp,"%d %d %d %d %d %d %d %d %d\n",op,a,b,c,d,e,f,g,h);
    }
   fclose(fp);

    return 0;
}
```

5.2

```
#include <stdio.h>
```

```
#include <stdlib.h>

int main() {
    int a,b,c,d,e,f,g,h;
    int op;

    FILE *fp;
    fp=fopen("in.dat","w");
    for (int i=0;i<8;i++){
    a=i;
    b=i+8;
    c=i+16;
    d=i+24;
    e=i+32;                          //for 5.2
    f=i+40;
    g=i+48;
    h=i+56;
    op=i;

   fprintf(fp,"%d %d %d %d %d %d %d %d %d\n",op,a,b,c,d,e,f,g,h);
    }
   fclose(fp);

    return 0;
}
```

6 in.dat file

5.1

```
0  0  1  2  3  4  5  6  7
8  8  9  10  11  12  13  14  15
16  16  17  18  19  20  21  22  23
24  24  25  26  27  28  29  30  31
32  32  33  34  35  36  37  38  39
40  40  41  42  43  44  45  46  47
48  48  49  50  51  52  53  54  55
56  56  57  58  59  60  61  62  63
```

5.2

```
0  0  8  16  24  32  40  48  56
1  1  9  17  25  33  41  49  57
2  2  10  18  26  34  42  50  58
3  3  11  19  27  35  43  51  59
4  4  12  20  28  36  44  52  60
5  5  13  21  29  37  45  53  61
6  6  14  22  30  38  46  54  62
7  7  15  23  31  39  47  55  63
```

7 out.dat file

5.1

```
0 1 2 3 4 5 6 7 Pass
8 9 10 11 12 13 14 15 Pass
16 17 18 19 20 21 22 23 Pass
24 25 26 27 28 29 30 31 Pass
32 33 34 35 36 37 38 39 Pass
40 41 42 43 44 45 46 47 Pass
48 49 50 51 52 53 54 55 Pass
56 57 58 59 60 61 62 63 Pass
```

5.2

```
0 8 16 24 32 40 48 56 Pass
1 9 17 25 33 41 49 57 Pass
2 10 18 26 34 42 50 58 Pass
3 11 19 27 35 43 51 59 Pass
4 12 20 28 36 44 52 60 Pass
5 13 21 29 37 45 53 61 Pass
6 14 22 30 38 46 54 62 Pass
7 15 23 31 39 47 55 63 Pass
```

8 HLS Resource Consumption

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	275
FIFO	-	-	-	-
Instance	-	-	0	360
Memory	8	-	0	0
Multiplexer	-	-	-	474
Register	-	-	109	-
Total	8	0	109	1109
Available	280	220	106400	53200
Utilization (%)	2	0	~0	2

(a) 5.1

Utilization Estimates

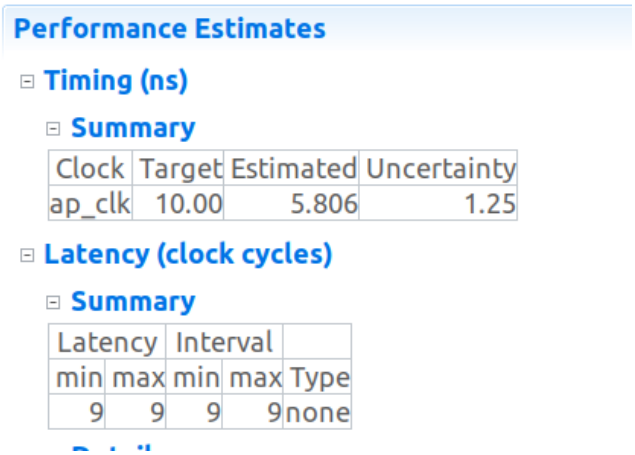
Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	275
FIFO	-	-	-	-
Instance	-	-	0	360
Memory	8	-	0	0
Multiplexer	-	-	-	93
Register	-	-	96	-
Total	8	0	96	728
Available	280	220	106400	53200
Utilization (%)	2	0	~0	1

Detail

(b) 5.2

9 HLS Timing Report



Performance Estimates

Timing (ns)

Summary

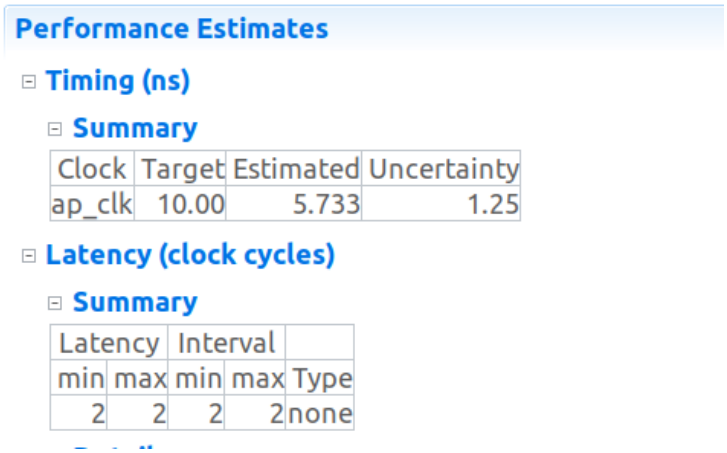
Clock	Target	Estimated	Uncertainty
ap_clk	10.00	5.806	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
9	9	9	9	none

(a) 5.1



Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	5.733	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
2	2	2	2	none

(b) 5.2

10 Interfaces Report

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	a5a	return value
ap_rst	in	1	ap_ctrl_hs	a5a	return value
ap_start	in	1	ap_ctrl_hs	a5a	return value
ap_done	out	1	ap_ctrl_hs	a5a	return value
ap_idle	out	1	ap_ctrl_hs	a5a	return value
ap_ready	out	1	ap_ctrl_hs	a5a	return value
index	in	32	ap_none	index	scalar
output_V_data_0_V_din	out	8	ap_fifo	output_V_data_0_V	pointer
output_V_data_0_V_full_n	in	1	ap_fifo	output_V_data_0_V	pointer
output_V_data_0_V_write	out	1	ap_fifo	output_V_data_0_V	pointer
output_V_data_1_V_din	out	8	ap_fifo	output_V_data_1_V	pointer
output_V_data_1_V_full_n	in	1	ap_fifo	output_V_data_1_V	pointer
output_V_data_1_V_write	out	1	ap_fifo	output_V_data_1_V	pointer
output_V_data_2_V_din	out	8	ap_fifo	output_V_data_2_V	pointer
output_V_data_2_V_full_n	in	1	ap_fifo	output_V_data_2_V	pointer
output_V_data_2_V_write	out	1	ap_fifo	output_V_data_2_V	pointer
output_V_data_3_V_din	out	8	ap_fifo	output_V_data_3_V	pointer
output_V_data_3_V_full_n	in	1	ap_fifo	output_V_data_3_V	pointer
output_V_data_3_V_write	out	1	ap_fifo	output_V_data_3_V	pointer
output_V_data_4_V_din	out	8	ap_fifo	output_V_data_4_V	pointer
output_V_data_4_V_full_n	in	1	ap_fifo	output_V_data_4_V	pointer
output_V_data_4_V_write	out	1	ap_fifo	output_V_data_4_V	pointer
output_V_data_5_V_din	out	8	ap_fifo	output_V_data_5_V	pointer
output_V_data_5_V_full_n	in	1	ap_fifo	output_V_data_5_V	pointer
output_V_data_5_V_write	out	1	ap_fifo	output_V_data_5_V	pointer
output_V_data_6_V_din	out	8	ap_fifo	output_V_data_6_V	pointer
output_V_data_6_V_full_n	in	1	ap_fifo	output_V_data_6_V	pointer
output_V_data_6_V_write	out	1	ap_fifo	output_V_data_6_V	pointer
output_V_data_7_V_din	out	8	ap_fifo	output_V_data_7_V	pointer
output_V_data_7_V_full_n	in	1	ap_fifo	output_V_data_7_V	pointer
output_V_data_7_V_write	out	1	ap_fifo	output_V_data_7_V	pointer

(a) 5.1

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	a5a	return value
ap_rst	in	1	ap_ctrl_hs	a5a	return value
ap_start	in	1	ap_ctrl_hs	a5a	return value
ap_done	out	1	ap_ctrl_hs	a5a	return value
ap_idle	out	1	ap_ctrl_hs	a5a	return value
ap_ready	out	1	ap_ctrl_hs	a5a	return value
index	in	32	ap_none	index	scalar
output_V_data_0_V_din	out	8	ap_fifo	output_V_data_0_V	pointer
output_V_data_0_V_full_n	in	1	ap_fifo	output_V_data_0_V	pointer
output_V_data_0_V_write	out	1	ap_fifo	output_V_data_0_V	pointer
output_V_data_1_V_din	out	8	ap_fifo	output_V_data_1_V	pointer
output_V_data_1_V_full_n	in	1	ap_fifo	output_V_data_1_V	pointer
output_V_data_1_V_write	out	1	ap_fifo	output_V_data_1_V	pointer
output_V_data_2_V_din	out	8	ap_fifo	output_V_data_2_V	pointer
output_V_data_2_V_full_n	in	1	ap_fifo	output_V_data_2_V	pointer
output_V_data_2_V_write	out	1	ap_fifo	output_V_data_2_V	pointer
output_V_data_3_V_din	out	8	ap_fifo	output_V_data_3_V	pointer
output_V_data_3_V_full_n	in	1	ap_fifo	output_V_data_3_V	pointer
output_V_data_3_V_write	out	1	ap_fifo	output_V_data_3_V	pointer
output_V_data_4_V_din	out	8	ap_fifo	output_V_data_4_V	pointer
output_V_data_4_V_full_n	in	1	ap_fifo	output_V_data_4_V	pointer
output_V_data_4_V_write	out	1	ap_fifo	output_V_data_4_V	pointer
output_V_data_5_V_din	out	8	ap_fifo	output_V_data_5_V	pointer
output_V_data_5_V_full_n	in	1	ap_fifo	output_V_data_5_V	pointer
output_V_data_5_V_write	out	1	ap_fifo	output_V_data_5_V	pointer
output_V_data_6_V_din	out	8	ap_fifo	output_V_data_6_V	pointer
output_V_data_6_V_full_n	in	1	ap_fifo	output_V_data_6_V	pointer
output_V_data_6_V_write	out	1	ap_fifo	output_V_data_6_V	pointer
output_V_data_7_V_din	out	8	ap_fifo	output_V_data_7_V	pointer
output_V_data_7_V_full_n	in	1	ap_fifo	output_V_data_7_V	pointer
output_V_data_7_V_write	out	1	ap_fifo	output_V_data_7_V	pointer

(b) 5.2

11 C/RTL Cosimulation Output

5.1

```
Starting C/RTL cosimulation ...
/tools/Xilinx/Vivado/2018.3/bin/vivado_hls /home/sam-admin/git/Training/HLS_Assi
INFO: [HLS 200-10] Running '/tools/Xilinx/Vivado/2018.3/bin/unwrapped/lnx64.o/vi
INFO: [HLS 200-10] For user 'sam-admin' on host 'sampaths-lappie' (Linux_x86_64
INFO: [HLS 200-10] On os Ubuntu 22.04.2 LTS
INFO: [HLS 200-10] In directory '/home/sam-admin/git/Training/HLS_Assignments/A5
INFO: [HLS 200-10] Opening project '/home/sam-admin/git/Training/HLS_Assignments
INFO: [HLS 200-10] Opening solution '/home/sam-admin/git/Training/HLS_Assignment
INFO: [SYN 201-201] Setting up clock 'default' with a period of 10ns.
INFO: [HLS 200-10] Setting target device to 'xc7z020clg484-1'
INFO: [COSIM 212-47] Using XSIM for RTL simulation.
INFO: [COSIM 212-14] Instrumenting C test bench ...
   Build using "/tools/Xilinx/Vivado/2018.3/tps/lnx64/gcc-6.2.0/bin/g++"
   Compiling a51a.cpp_pre.cpp.tb.cpp
   Compiling a5a_tb.cpp_pre.cpp.tb.cpp
   Compiling apatb_a5a.cpp
   Generating cosim.tv.exe
INFO: [COSIM 212-302] Starting C TB testing ...
ALL THE TEST CASES ARE PASSED!
INFO: [COSIM 212-333] Generating C post check test bench ...
INFO: [COSIM 212-12] Generating RTL test bench ...
INFO: [COSIM 212-323] Starting verilog simulation.
INFO: [COSIM 212-15] Starting XSIM ...
INFO: [XSIM 43-3496] Using init file passed via -initfile option "/tools/Xilinx/
Vivado Simulator 2018.3
Copyright 1986-1999, 2001-2018 Xilinx, Inc. All Rights Reserved.
Running: /tools/Xilinx/Vivado/2018.3/bin/unwrapped/lnx64.o/xelab xil_defaultlib.
Multi-threading is on. Using 6 slave threads.
WARNING: [XSIM 43-3431] One or more environment variables have been detected whi
If errors occur, try running xelab with the "-mt off -v 1" switches to see more
   LIBRARY_PATH
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module glbl
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_output_V_data_6_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_output_V_data_3_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5a_bram_4_rom
```

```
INFO: [VRFC 10-311] analyzing module a5a_bram_4
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_output_V_data_7_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5a_bram_7_rom
INFO: [VRFC 10-311] analyzing module a5a_bram_7
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5a_bram_0_rom
INFO: [VRFC 10-311] analyzing module a5a_bram_0
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5a_bram_6_rom
INFO: [VRFC 10-311] analyzing module a5a_bram_6
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_output_V_data_0_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_output_V_data_2_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5a_bram_2_rom
INFO: [VRFC 10-311] analyzing module a5a_bram_2
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5a_bram_5_rom
INFO: [VRFC 10-311] analyzing module a5a_bram_5
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5a_mux_832_8_1_1
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5a_bram_3_rom
INFO: [VRFC 10-311] analyzing module a5a_bram_3
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5a
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_output_V_data_4_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module apatb_a5a_top
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_output_V_data_5_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_output_V_data_1_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5a_bram_1_rom
INFO: [VRFC 10-311] analyzing module a5a_bram_1
Starting static elaboration
Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module xil_defaultlib.a5a_bram_0_rom
```

```
Compiling module xil_defaultlib.a5a_bram_0(DataWidth=6,AddressRa...
Compiling module xil_defaultlib.a5a_bram_1_rom
Compiling module xil_defaultlib.a5a_bram_1(DataWidth=6,AddressRa...
Compiling module xil_defaultlib.a5a_bram_2_rom
Compiling module xil_defaultlib.a5a_bram_2(DataWidth=6,AddressRa...
Compiling module xil_defaultlib.a5a_bram_3_rom
Compiling module xil_defaultlib.a5a_bram_3(DataWidth=6,AddressRa...
Compiling module xil_defaultlib.a5a_bram_4_rom
Compiling module xil_defaultlib.a5a_bram_4(DataWidth=6,AddressRa...
Compiling module xil_defaultlib.a5a_bram_5_rom
Compiling module xil_defaultlib.a5a_bram_5(DataWidth=6,AddressRa...
Compiling module xil_defaultlib.a5a_bram_6_rom
Compiling module xil_defaultlib.a5a_bram_6(DataWidth=6,AddressRa...
Compiling module xil_defaultlib.a5a_bram_7_rom
Compiling module xil_defaultlib.a5a_bram_7(DataWidth=6,AddressRa...
Compiling module xil_defaultlib.a5a_mux_832_8_1_1(ID=1,din0_WIDT...
Compiling module xil_defaultlib.a5a
Compiling module xil_defaultlib.AESL_autofifo_output_V_data_0_V
Compiling module xil_defaultlib.AESL_autofifo_output_V_data_1_V
Compiling module xil_defaultlib.AESL_autofifo_output_V_data_2_V
Compiling module xil_defaultlib.AESL_autofifo_output_V_data_3_V
Compiling module xil_defaultlib.AESL_autofifo_output_V_data_4_V
Compiling module xil_defaultlib.AESL_autofifo_output_V_data_5_V
Compiling module xil_defaultlib.AESL_autofifo_output_V_data_6_V
Compiling module xil_defaultlib.AESL_autofifo_output_V_data_7_V
Compiling module xil_defaultlib.apatb_a5a_top
Compiling module work.glbl
Built simulation snapshot a5a


****** Webtalk v2018.3 (64-bit)
  **** SW Build 2405991 on Thu Dec  6 23:36:41 MST 2018
  **** IP Build 2404404 on Fri Dec  7 01:43:56 MST 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.


source /home/sam-admin/git/Training/HLS_Assignments/A5/5.1/codes/Assignmnet5a/so
INFO: [Common 17-206] Exiting Webtalk at Mon Apr  3 12:40:39 2023...


****** xsim v2018.3 (64-bit)
  **** SW Build 2405991 on Thu Dec  6 23:36:41 MST 2018
  **** IP Build 2404404 on Fri Dec  7 01:43:56 MST 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.
```

```
source xsim.dir/a5a/xsim_script.tcl
# xsim {a5a} -autoloadwcfg -tclbatch {a5a.tcl}
Vivado Simulator 2018.3
Time resolution is 1 ps
source a5a.tcl
## run all
////////////////////////////////////////////////////////////////////////////////
// Inter-Transaction Progress: Completed Transaction / Total Transaction
// Intra-Transaction Progress: Measured Latency / Latency Estimation * 100%
//
// RTL Simulation : "Inter-Transaction Progress" ["Intra-Transaction Progress"]
////////////////////////////////////////////////////////////////////////////////
// RTL Simulation : 0 / 8 [0.00%] @ "125000"
// RTL Simulation : 1 / 8 [100.00%] @ "235000"
// RTL Simulation : 2 / 8 [100.00%] @ "335000"
// RTL Simulation : 3 / 8 [100.00%] @ "435000"
// RTL Simulation : 4 / 8 [100.00%] @ "535000"
// RTL Simulation : 5 / 8 [100.00%] @ "635000"
// RTL Simulation : 6 / 8 [100.00%] @ "735000"
// RTL Simulation : 7 / 8 [100.00%] @ "835000"
// RTL Simulation : 8 / 8 [100.00%] @ "935000"
////////////////////////////////////////////////////////////////////////////////
$finish called at time : 975 ns : File "/home/sam-admin/git/Training/HLS_Assignm
## quit
INFO: [Common 17-206] Exiting xsim at Mon Apr  3 12:40:57 2023...
INFO: [COSIM 212-316] Starting C post checking ...
ALL THE TEST CASES ARE PASSED!
INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***
Finished C/RTL cosimulation.
```

5.2

```
Starting C/RTL cosimulation ...
/tools/Xilinx/Vivado/2018.3/bin/vivado_hls /home/sam-admin/git/Training/HLS_Assi
INFO: [HLS 200-10] Running '/tools/Xilinx/Vivado/2018.3/bin/unwrapped/lnx64.o/vi
INFO: [HLS 200-10] For user 'sam-admin' on host 'sampaths-lappie' (Linux_x86_64
INFO: [HLS 200-10] On os Ubuntu 22.04.2 LTS
```

```
INFO: [HLS 200-10] In directory '/home/sam-admin/git/Training/HLS_Assignments/A5
INFO: [HLS 200-10] Opening project '/home/sam-admin/git/Training/HLS_Assignments
INFO: [HLS 200-10] Opening solution '/home/sam-admin/git/Training/HLS_Assignment
INFO: [SYN 201-201] Setting up clock 'default' with a period of 10ns.
INFO: [HLS 200-10] Setting target device to 'xc7z020clg484-1'
INFO: [COSIM 212-47] Using XSIM for RTL simulation.
INFO: [COSIM 212-14] Instrumenting C test bench ...
   Build using "/tools/Xilinx/Vivado/2018.3/tps/lnx64/gcc-6.2.0/bin/g++"
   Compiling a51a.cpp_pre.cpp.tb.cpp
   Compiling a5a_tb.cpp_pre.cpp.tb.cpp
   Compiling apatb_a5a.cpp
   Generating cosim.tv.exe
INFO: [COSIM 212-302] Starting C TB testing ...
ALL THE TEST CASES ARE PASSED!
INFO: [COSIM 212-333] Generating C post check test bench ...
INFO: [COSIM 212-12] Generating RTL test bench ...
INFO: [COSIM 212-323] Starting verilog simulation.
INFO: [COSIM 212-15] Starting XSIM ...
INFO: [XSIM 43-3496] Using init file passed via -initfile option "/tools/Xilinx/
Vivado Simulator 2018.3
Copyright 1986-1999, 2001-2018 Xilinx, Inc. All Rights Reserved.
Running: /tools/Xilinx/Vivado/2018.3/bin/unwrapped/lnx64.o/xelab xil_defaultlib.
Multi-threading is on. Using 6 slave threads.
WARNING: [XSIM 43-3431] One or more environment variables have been detected whi
If errors occur, try running xelab with the "-mt off -v 1" switches to see more
    LIBRARY_PATH
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module glbl
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_output_V_data_6_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_output_V_data_3_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5a_bram_4_rom
INFO: [VRFC 10-311] analyzing module a5a_bram_4
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_output_V_data_7_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5a_bram_0_rom
INFO: [VRFC 10-311] analyzing module a5a_bram_0
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_output_V_data_0_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_output_V_data_2_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5a_bram_2_rom
```

```
INFO: [VRFC 10-311] analyzing module a5a_bram_2
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5a_bram_5_rom
INFO: [VRFC 10-311] analyzing module a5a_bram_5
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5a_mux_832_8_1_1
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5a
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_output_V_data_4_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module apatb_a5a_top
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_output_V_data_5_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_output_V_data_1_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5a_bram_1_rom
INFO: [VRFC 10-311] analyzing module a5a_bram_1
Starting static elaboration
Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module xil_defaultlib.a5a_bram_0_rom
Compiling module xil_defaultlib.a5a_bram_0(DataWidth=3,AddressRa...
Compiling module xil_defaultlib.a5a_bram_1_rom
Compiling module xil_defaultlib.a5a_bram_1(DataWidth=4,AddressRa...
Compiling module xil_defaultlib.a5a_bram_2_rom
Compiling module xil_defaultlib.a5a_bram_2(DataWidth=5,AddressRa...
Compiling module xil_defaultlib.a5a_bram_4_rom
Compiling module xil_defaultlib.a5a_bram_4(DataWidth=6,AddressRa...
Compiling module xil_defaultlib.a5a_bram_5_rom
Compiling module xil_defaultlib.a5a_bram_5(DataWidth=6,AddressRa...
Compiling module xil_defaultlib.a5a_mux_832_8_1_1(ID=1,din0_WIDT...
Compiling module xil_defaultlib.a5a
Compiling module xil_defaultlib.AESL_autofifo_output_V_data_0_V
Compiling module xil_defaultlib.AESL_autofifo_output_V_data_1_V
Compiling module xil_defaultlib.AESL_autofifo_output_V_data_2_V
Compiling module xil_defaultlib.AESL_autofifo_output_V_data_3_V
Compiling module xil_defaultlib.AESL_autofifo_output_V_data_4_V
Compiling module xil_defaultlib.AESL_autofifo_output_V_data_5_V
Compiling module xil_defaultlib.AESL_autofifo_output_V_data_6_V
Compiling module xil_defaultlib.AESL_autofifo_output_V_data_7_V
Compiling module xil_defaultlib.apatb_a5a_top
Compiling module work.glbl
```

```
Built simulation snapshot a5a


****** Webtalk v2018.3 (64-bit)
  **** SW Build 2405991 on Thu Dec  6 23:36:41 MST 2018
  **** IP Build 2404404 on Fri Dec  7 01:43:56 MST 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.


source /home/sam-admin/git/Training/HLS_Assignments/A5/5.1/codes/Assignmnet5a/so
INFO: [Common 17-206] Exiting Webtalk at Mon Apr  3 13:47:26 2023...


****** xsim v2018.3 (64-bit)
  **** SW Build 2405991 on Thu Dec  6 23:36:41 MST 2018
  **** IP Build 2404404 on Fri Dec  7 01:43:56 MST 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.


source xsim.dir/a5a/xsim_script.tcl
# xsim {a5a} -autoloadwcfg -tclbatch {a5a.tcl}
Vivado Simulator 2018.3
Time resolution is 1 ps
source a5a.tcl
## run all
////////////////////////////////////////////////////////////////////////////////
// Inter-Transaction Progress: Completed Transaction / Total Transaction
// Intra-Transaction Progress: Measured Latency / Latency Estimation * 100%
//
// RTL Simulation : "Inter-Transaction Progress" ["Intra-Transaction Progress"]
////////////////////////////////////////////////////////////////////////////////
// RTL Simulation : 0 / 8 [0.00%] @ "125000"
// RTL Simulation : 1 / 8 [100.00%] @ "165000"
// RTL Simulation : 2 / 8 [100.00%] @ "195000"
// RTL Simulation : 3 / 8 [100.00%] @ "225000"
// RTL Simulation : 4 / 8 [100.00%] @ "255000"
// RTL Simulation : 5 / 8 [100.00%] @ "285000"
// RTL Simulation : 6 / 8 [100.00%] @ "315000"
// RTL Simulation : 7 / 8 [100.00%] @ "345000"
// RTL Simulation : 8 / 8 [100.00%] @ "375000"
////////////////////////////////////////////////////////////////////////////////
$finish called at time : 415 ns : File "/home/sam-admin/git/Training/HLS_Assignm
## quit
INFO: [Common 17-206] Exiting xsim at Mon Apr  3 13:47:44 2023...
INFO: [COSIM 212-316] Starting C post checking ...
ALL THE TEST CASES ARE PASSED!
```

INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***
Finished C/RTL cosimulation.

12 C/RTL Cosimulation Report

Cosimulation Report for 'a5a'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	9	9	9	10	10	10

Export the report(.html) using the Export Wizard

(a) 5.1

Cosimulation Report for 'a5a'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	2	2	2	3	3	3

Export the report(.html) using the Export Wizard

(b) 5.2

HLS-Assignment 5 B

April 3, 2023

Sampath Govardhan
FWC22071

1 Problem Statement

Implement a DUT that takes 4 inputs in 4 clock cycles and then saves all the inputs in a BRAM (The BRAM should be contained within the DUT) at a single address. At the same time, it also gives out all the 4 inputs as a single bundle output in the same clock cycle when it receives the final input. The BRAM index will overflow after the BRAM is full and it should overwrite the old values as more inputs keep coming in.

2 Design Code

```
#include"hls_stream.h"
#include "ap_int.h"
//#include "ap_axi_sdata.h"
using namespace std;

struct bundle{
        ap_uint<8> data[4];
};

void a5b(hls::stream<bundle> &in, hls::stream<bundle> &out){
```

```
bundle input=in.read();

bundle output={0,0,0,0};
ap_uint<8> bram[8];
#pragma HLS RESOURCE variable=bram core=RAM_1P_BRAM
#pragma HLS ARRAY_RESHAPE variable=bram cyclic factor=4 dim=1
ap_uint<3> c=0,add=0;
int ind=0;

for (int i=0;i<4;i++){

        if (c<8){
        bram[add]=input.data[ind];
        c=c+1;
        add=add+1;
        ind=ind+1;

        if (c==4){
        output.data[0]=bram[0];
        output.data[1]=bram[1];
        output.data[2]=bram[2];
        output.data[3]=bram[3];
        }
        }
        else{
        c=0;
        add=0;
        }
        }
        out.write(output);
        }
```

3 Test Bench Code

```
#include<hls_stream.h>
#include <ap_int.h>
#include<iostream>
#include <fstream>
using namespace std;

struct bundle{
        ap_uint<8> data[4];
};


void a5b(hls::stream<bundle> &in, hls::stream<bundle> &out);
int main(){
hls::stream<bundle> indata;
hls::stream<bundle> outdata;
bundle input;
ifstream in;
ofstream out_d;

in.open("in.dat");
out_d.open("out.dat");

int i,index=0;
bool fail=0;

while (in>>i && index<4){
input.data[index]=i;
index=index+1;
}
indata.write(input);
a5b(indata,outdata);
bundle output=outdata.read();
for (int j=0;j<4;j++){
out_d<<output.data[j]<<" ";
}
if (input.data[0]==output.data[0] && input.data[1]==output.data[1] &&
 input.data[2]==output.data[2] && input.data[3]==output.data[3] ){
out_d<<"Pass"<<endl;
}
else{
out_d<<"Fail"<<endl;
fail++;
}
```

```
in.close();
out_d.close();
if (fail==0){
cout<<"ALL THE TEST CASES ARE PASSED!"<<endl;
}
else{
cout<<"ERROR! ALL THE TEST CASES ARE NOT PASSED!"<<endl;
}}
```

4 in.dat file

```
7 8 6 4
```

5 out.dat file

```
7 8 6 4 Pass
```

6 HLS Resource Consumption

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	1051
FIFO	-	-	-	-
Instance	-	-	0	21
Memory	1	-	0	0
Multiplexer	-	-	-	177
Register	-	-	89	-
Total	1	0	89	1249
Available	280	220	106400	53200
Utilization (%)	~0	0	~0	2

Figure 1: Resource Consumption

7 HLS Timing Report

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	7.397	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
9	9	9	9	none

Detail

Figure 2: Timing Report

8 Interfaces Report

Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	a5b	return value
ap_rst	in	1	ap_ctrl_hs	a5b	return value
ap_start	in	1	ap_ctrl_hs	a5b	return value
ap_done	out	1	ap_ctrl_hs	a5b	return value
ap_idle	out	1	ap_ctrl_hs	a5b	return value
ap_ready	out	1	ap_ctrl_hs	a5b	return value
in_V_data_0_V_dout	in	8	ap_fifo	in_V_data_0_V	pointer
in_V_data_0_V_empty_n	in	1	ap_fifo	in_V_data_0_V	pointer
in_V_data_0_V_read	out	1	ap_fifo	in_V_data_0_V	pointer
in_V_data_1_V_dout	in	8	ap_fifo	in_V_data_1_V	pointer
in_V_data_1_V_empty_n	in	1	ap_fifo	in_V_data_1_V	pointer
in_V_data_1_V_read	out	1	ap_fifo	in_V_data_1_V	pointer
in_V_data_2_V_dout	in	8	ap_fifo	in_V_data_2_V	pointer
in_V_data_2_V_empty_n	in	1	ap_fifo	in_V_data_2_V	pointer
in_V_data_2_V_read	out	1	ap_fifo	in_V_data_2_V	pointer
in_V_data_3_V_dout	in	8	ap_fifo	in_V_data_3_V	pointer
in_V_data_3_V_empty_n	in	1	ap_fifo	in_V_data_3_V	pointer
in_V_data_3_V_read	out	1	ap_fifo	in_V_data_3_V	pointer
out_V_data_0_V_din	out	8	ap_fifo	out_V_data_0_V	pointer
out_V_data_0_V_full_n	in	1	ap_fifo	out_V_data_0_V	pointer
out_V_data_0_V_write	out	1	ap_fifo	out_V_data_0_V	pointer
out_V_data_1_V_din	out	8	ap_fifo	out_V_data_1_V	pointer
out_V_data_1_V_full_n	in	1	ap_fifo	out_V_data_1_V	pointer
out_V_data_1_V_write	out	1	ap_fifo	out_V_data_1_V	pointer
out_V_data_2_V_din	out	8	ap_fifo	out_V_data_2_V	pointer
out_V_data_2_V_full_n	in	1	ap_fifo	out_V_data_2_V	pointer
out_V_data_2_V_write	out	1	ap_fifo	out_V_data_2_V	pointer
out_V_data_3_V_din	out	8	ap_fifo	out_V_data_3_V	pointer
out_V_data_3_V_full_n	in	1	ap_fifo	out_V_data_3_V	pointer
out_V_data_3_V_write	out	1	ap_fifo	out_V_data_3_V	pointer

Figure 3: Interface Summmary

9 C/RTL Cosimulation Output

```
Starting C/RTL cosimulation ...
/tools/Xilinx/Vivado/2018.3/bin/vivado_hls /home/sam-admin/git/Training/HLS_Assi
INFO: [HLS 200-10] Running '/tools/Xilinx/Vivado/2018.3/bin/unwrapped/lnx64.o/vi
INFO: [HLS 200-10] For user 'sam-admin' on host 'sampaths-lappie' (Linux_x86_64
INFO: [HLS 200-10] On os Ubuntu 22.04.2 LTS
INFO: [HLS 200-10] In directory '/home/sam-admin/git/Training/HLS_Assignments/A5
INFO: [HLS 200-10] Opening project '/home/sam-admin/git/Training/HLS_Assignments
INFO: [HLS 200-10] Opening solution '/home/sam-admin/git/Training/HLS_Assignment
INFO: [SYN 201-201] Setting up clock 'default' with a period of 10ns.
INFO: [HLS 200-10] Setting target device to 'xc7z020clg484-1'
INFO: [COSIM 212-47] Using XSIM for RTL simulation.
INFO: [COSIM 212-14] Instrumenting C test bench ...
   Build using "/tools/Xilinx/Vivado/2018.3/tps/lnx64/gcc-6.2.0/bin/g++"
   Compiling a5b.cpp_pre.cpp.tb.cpp
   Compiling a5b_tb.cpp_pre.cpp.tb.cpp
   Compiling apatb_a5b.cpp
   Generating cosim.tv.exe
INFO: [COSIM 212-302] Starting C TB testing ...
ALL THE TEST CASES ARE PASSED!
INFO: [COSIM 212-333] Generating C post check test bench ...
INFO: [COSIM 212-12] Generating RTL test bench ...
INFO: [COSIM 212-323] Starting verilog simulation.
INFO: [COSIM 212-15] Starting XSIM ...
INFO: [XSIM 43-3496] Using init file passed via -initfile option "/tools/Xilinx/
Vivado Simulator 2018.3
Copyright 1986-1999, 2001-2018 Xilinx, Inc. All Rights Reserved.
Running: /tools/Xilinx/Vivado/2018.3/bin/unwrapped/lnx64.o/xelab xil_defaultlib.
Multi-threading is on. Using 6 slave threads.
WARNING: [XSIM 43-3431] One or more environment variables have been detected whi
If errors occur, try running xelab with the "-mt off -v 1" switches to see more
   LIBRARY_PATH
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module glbl
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module apatb_a5b_top
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_in_V_data_2_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_out_V_data_0_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5b
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_out_V_data_3_V
```

```
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5b_mux_42_8_1_1
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_out_V_data_2_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_in_V_data_3_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a5b_bram_V_ram
INFO: [VRFC 10-311] analyzing module a5b_bram_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_in_V_data_1_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_out_V_data_1_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_autofifo_in_V_data_0_V
Starting static elaboration
Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module xil_defaultlib.a5b_bram_V_ram_default
Compiling module xil_defaultlib.a5b_bram_V(DataWidth=32,AddressR...
Compiling module xil_defaultlib.a5b_mux_42_8_1_1(ID=1,din0_WIDTH...
Compiling module xil_defaultlib.a5b
Compiling module xil_defaultlib.AESL_autofifo_in_V_data_0_V
Compiling module xil_defaultlib.AESL_autofifo_in_V_data_1_V
Compiling module xil_defaultlib.AESL_autofifo_in_V_data_2_V
Compiling module xil_defaultlib.AESL_autofifo_in_V_data_3_V
Compiling module xil_defaultlib.AESL_autofifo_out_V_data_0_V
Compiling module xil_defaultlib.AESL_autofifo_out_V_data_1_V
Compiling module xil_defaultlib.AESL_autofifo_out_V_data_2_V
Compiling module xil_defaultlib.AESL_autofifo_out_V_data_3_V
Compiling module xil_defaultlib.apatb_a5b_top
Compiling module work.glbl
Built simulation snapshot a5b


****** Webtalk v2018.3 (64-bit)
  **** SW Build 2405991 on Thu Dec  6 23:36:41 MST 2018
  **** IP Build 2404404 on Fri Dec  7 01:43:56 MST 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.


source /home/sam-admin/git/Training/HLS_Assignments/A5/5.2/codes/Assignment5b/so
INFO: [Common 17-206] Exiting Webtalk at Mon Apr  3 17:24:15 2023...
```

```
****** xsim v2018.3 (64-bit)
  **** SW Build 2405991 on Thu Dec  6 23:36:41 MST 2018
  **** IP Build 2404404 on Fri Dec  7 01:43:56 MST 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.


source xsim.dir/a5b/xsim_script.tcl
# xsim {a5b} -autoloadwcfg -tclbatch {a5b.tcl}
Vivado Simulator 2018.3
Time resolution is 1 ps
source a5b.tcl
## run all
////////////////////////////////////////////////////////////////////////////////
// Inter-Transaction Progress: Completed Transaction / Total Transaction
// Intra-Transaction Progress: Measured Latency / Latency Estimation * 100%
//
// RTL Simulation : "Inter-Transaction Progress" ["Intra-Transaction Progress"]
////////////////////////////////////////////////////////////////////////////////
// RTL Simulation : 0 / 1 [0.00%] @ "125000"
// RTL Simulation : 1 / 1 [100.00%] @ "235000"
////////////////////////////////////////////////////////////////////////////////
$finish called at time : 275 ns : File "/home/sam-admin/git/Training/HLS_Assignm
## quit
INFO: [Common 17-206] Exiting xsim at Mon Apr  3 17:24:23 2023...
INFO: [COSIM 212-316] Starting C post checking ...
ALL THE TEST CASES ARE PASSED!
INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***
INFO: [COSIM 212-211] II is measurable only when transaction number is greater t
Finished C/RTL cosimulation.
```

10 C/RTL Cosimulation Report

Cosimulation Report for 'a5b'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	9	9	9	NA	NA	NA

Export the report(.html) using the Export Wizard

Figure 4: Cosimulation Report