HLS-Assignment 4

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1 Problem Statement

Design a basic integer ALU unit in HLS that takes 3 inputs: Two 8bit operands and one appropriately sized operator. The permitted operations are ADD, SUB, MUL, DIV, AND, OR and XOR. Use AXI–S ports for all I/O ports.The design should be pipelined.

2 Header file

```
#ifndef _cal_H_
#define _cal_H_

#include <iostream>
#include "ap_int.h"

typedef ap_int<8> in;
typedef ap_uint<3> op;
typedef ap_int<16> out;

void cal(in a, in b, op c, out *d);
```

```
#endif
```

3 Design Code

```
#include "cal.h"

void cal(in a, in b, op c, out *d)
{
#pragma HLS INTERFACE axis register both port=a
#pragma HLS INTERFACE axis register both port=b
#pragma HLS INTERFACE axis register both port=c
#pragma HLS INTERFACE axis register both port=d
#pragma HLS PIPELINE

 switch(c){
 case 0: *d=a+b; break;
 case 1: *d=a-b; break;
 case 2: *d=a*b; break;
 case 3: *d=a/b; break;
 case 4: *d=a&b; break;
 case 5: *d=a|b; break;
 case 6: *d=a^b; break;
 default: break;
 }

}
```

4 Test Bench Code

```
#include <fstream>
```

```
#include "cal.h"
using namespace std;

void cal(in a, in b, op c, out *d);

int main() {
    in m,n;
    op o;
    out ref,res;
    bool q;

    ifstream fo("in.dat");
    ofstream fi("out.dat");

    for (int i=1;i<20;i++){
        fo>>o>>m>>n>>ref;
        cal(m,n,o,&res);
         if (res==ref)
         {
        fi<<" "<<res<<" "<<"Pass"<<"\n";
        }
         else {
        q=1;
        fi<<" "<<res<<" "<<"Fail"<<"\n";
          }
    }
   fo.close();
   fi.close();
   if (q!=1){
            cout<<"ALL THE TEST CASES ARE PASSED!";
   }
   else{
            cout<<"ALL THE TEST CASES ARE NOT PASSED!";
   }
   return 0;
}
```

5 Code for generating in.dat file

```
#include <stdio.h>
#include <stdlib.h>

int main() {
    int a,b;
    int op;
    int r;
    FILE *fp;
    fp=fopen("in.dat","w");
    for (int i=1;i<20;i++){
    a=i;
    b=i*3;
    op=i%7;
     switch(op){
 case 0: r=a+b; break;
 case 1: r=a-b; break;
 case 2: r=a*b; break;
 case 3: r=a/b; break;
 case 4: r=a&b; break;
 case 5: r=a|b; break;
 case 6: r=a^b; break;
 default: break;
 }



   fprintf(fp,"%d  %d  %d  %d\n",op,a,b,r);
    }
   fclose(fp);

    return 0;
}
```

6 in.dat file

```
1  1  3  -2
2  2  6  12
3  3  9  0
4  4  12  4
5  5  15  15
6  6  18  20
0  7  21  28
```

```
1   8   24   −16
2   9   27   243
3   10   30   0
4   11   33   1
5   12   36   44
6   13   39   42
0   14   42   56
1   15   45   −30
2   16   48   768
3   17   51   0
4   18   54   18
5   19   57   59
```

7 out.dat file

```
−2 Pass
12 Pass
0 Pass
4 Pass
15 Pass
20 Pass
28 Pass
−16 Pass
243 Pass
0 Pass
1 Pass
44 Pass
42 Pass
56 Pass
−30 Pass
768 Pass
0 Pass
18 Pass
59 Pass
```

8 C Simulation Output

```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
make: 'csim.exe' is up to date.
ALL THE TEST CASES ARE PASSED!
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************
```

9 HLS Resource Consumption

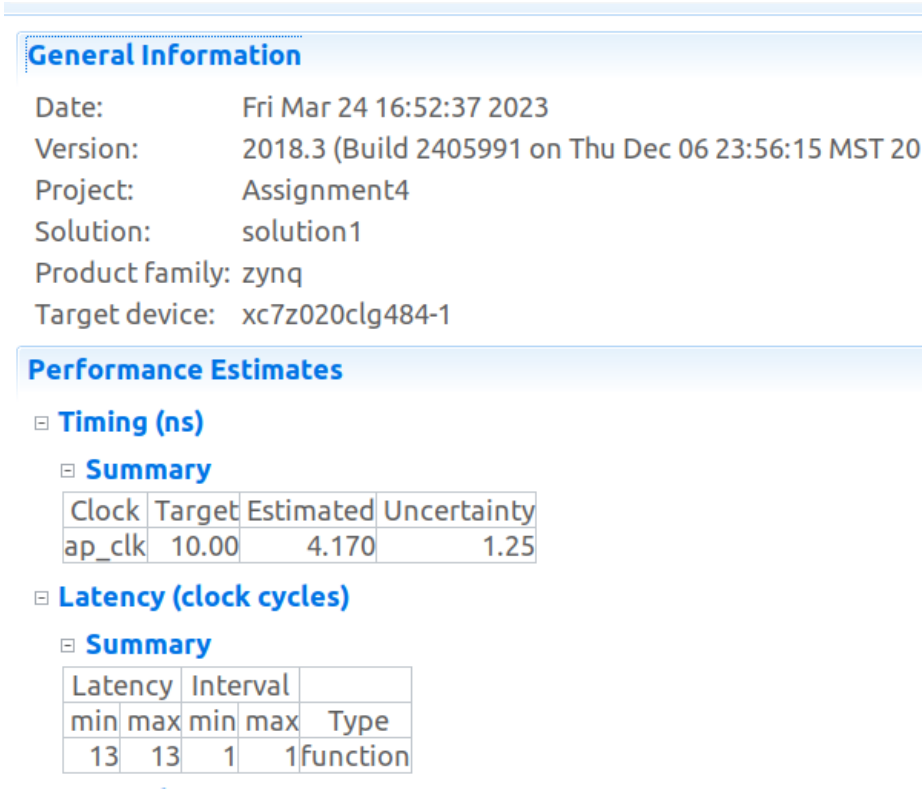
Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	0	0	155
FIFO	-	-	-	-
Instance	-	-	239	160
Memory	-	-	-	-
Multiplexer	-	-	-	173
Register	0	-	321	96
Total	0	0	560	584
Available	280	220	106400	53200
Utilization (%)	0	0	~0	1

Figure 1: Resource Consumption

10 HLS Timing Report



General Information

Date:	Fri Mar 24 16:52:37 2023
Version:	2018.3 (Build 2405991 on Thu Dec 06 23:56:15 MST 20
Project:	Assignment4
Solution:	solution1
Product family:	zynq
Target device:	xc7z020clg484-1

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	4.170	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
13	13	1	1	function

Figure 2: Timing Report

11 Interfaces Report

Interface

Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	cal	return value
ap_rst_n	in	1	ap_ctrl_hs	cal	return value
ap_start	in	1	ap_ctrl_hs	cal	return value
ap_done	out	1	ap_ctrl_hs	cal	return value
ap_idle	out	1	ap_ctrl_hs	cal	return value
ap_ready	out	1	ap_ctrl_hs	cal	return value
d_V_TREADY	in	1	axis	d_V	pointer
d_V_TDATA	out	16	axis	d_V	pointer
d_V_TVALID	out	1	axis	d_V	pointer
a_V_TDATA	in	8	axis	a_V	scalar
a_V_TVALID	in	1	axis	a_V	scalar
a_V_TREADY	out	1	axis	a_V	scalar
b_V_TDATA	in	8	axis	b_V	scalar
b_V_TVALID	in	1	axis	b_V	scalar
b_V_TREADY	out	1	axis	b_V	scalar
c_V_TDATA	in	8	axis	c_V	scalar
c_V_TVALID	in	1	axis	c_V	scalar
c_V_TREADY	out	1	axis	c_V	scalar

Figure 3: Interface Summmary

12 C/RTL Cosimulation Output

```
Starting C/RTL cosimulation ...
/tools/Xilinx/Vivado/2018.3/bin/vivado_hls /home/sam-admin/git/Training/HLS_Assi
INFO: [HLS 200-10] Running '/tools/Xilinx/Vivado/2018.3/bin/unwrapped/lnx64.o/vi
INFO: [HLS 200-10] For user 'sam-admin' on host 'sampaths-lappie' (Linux_x86_64
INFO: [HLS 200-10] On os Ubuntu 22.04.2 LTS
INFO: [HLS 200-10] In directory '/home/sam-admin/git/Training/HLS_Assignments/A4
INFO: [HLS 200-10] Opening project '/home/sam-admin/git/Training/HLS_Assignments
INFO: [HLS 200-10] Opening solution '/home/sam-admin/git/Training/HLS_Assignment
INFO: [SYN 201-201] Setting up clock 'default' with a period of 10ns.
INFO: [HLS 200-10] Setting target device to 'xc7z020clg484-1'
INFO: [COSIM 212-47] Using XSIM for RTL simulation.
INFO: [COSIM 212-14] Instrumenting C test bench ...
WARNING: [COSIM 212-75] Fifo port 'd_V' has a default depth of 1. Insufficient d
   Build using "/tools/Xilinx/Vivado/2018.3/tps/lnx64/gcc-6.2.0/bin/g++"
   Compiling a4.cpp_pre.cpp.tb.cpp
   Compiling a4_tb.cpp_pre.cpp.tb.cpp
   Compiling apatb_cal.cpp
   Generating cosim.tv.exe
INFO: [COSIM 212-302] Starting C TB testing ...
ALL THE TEST CASES ARE PASSED!INFO: [COSIM 212-333] Generating C post check test
INFO: [COSIM 212-12] Generating RTL test bench ...
INFO: [COSIM 212-323] Starting verilog simulation.
INFO: [COSIM 212-15] Starting XSIM ...
INFO: [XSIM 43-3496] Using init file passed via -initfile option "/tools/Xilinx/
Vivado Simulator 2018.3
Copyright 1986-1999, 2001-2018 Xilinx, Inc. All Rights Reserved.
Running: /tools/Xilinx/Vivado/2018.3/bin/unwrapped/lnx64.o/xelab xil_defaultlib.
Multi-threading is on. Using 6 slave threads.
WARNING: [XSIM 43-3431] One or more environment variables have been detected whi
If errors occur, try running xelab with the "-mt off -v 1" switches to see more
   LIBRARY_PATH
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module glbl
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module cal_sdiv_9s_8s_9_13_1_div_u
INFO: [VRFC 10-311] analyzing module cal_sdiv_9s_8s_9_13_1_div
INFO: [VRFC 10-311] analyzing module cal_sdiv_9s_8s_9_13_1
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module apatb_cal_top
```

```
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_axi_s_c_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_axi_s_b_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_axi_s_a_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module AESL_axi_s_d_V
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module fifo
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module cal
Starting static elaboration
Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module xil_defaultlib.cal_sdiv_9s_8s_9_13_1_div_u(in0_...
Compiling module xil_defaultlib.cal_sdiv_9s_8s_9_13_1_div(in0_WI...
Compiling module xil_defaultlib.cal_sdiv_9s_8s_9_13_1(ID=1,NUM_S...
Compiling module xil_defaultlib.cal
Compiling module xil_defaultlib.fifo(DEPTH=1)
Compiling module xil_defaultlib.AESL_axi_s_a_V
Compiling module xil_defaultlib.AESL_axi_s_b_V
Compiling module xil_defaultlib.AESL_axi_s_c_V
Compiling module xil_defaultlib.fifo(DEPTH=1,WIDTH=16)
Compiling module xil_defaultlib.AESL_axi_s_d_V
Compiling module xil_defaultlib.apatb_cal_top
Compiling module work.glbl
Built simulation snapshot cal


****** Webtalk v2018.3 (64-bit)
  **** SW Build 2405991 on Thu Dec  6 23:36:41 MST 2018
  **** IP Build 2404404 on Fri Dec  7 01:43:56 MST 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.


source /home/sam-admin/git/Training/HLS_Assignments/A4/codes/Assignment4/solutio
INFO: [Common 17-206] Exiting Webtalk at Fri Mar 24 16:53:26 2023...


****** xsim v2018.3 (64-bit)
  **** SW Build 2405991 on Thu Dec  6 23:36:41 MST 2018
  **** IP Build 2404404 on Fri Dec  7 01:43:56 MST 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.
```

```
source xsim.dir/cal/xsim_script.tcl
# xsim {cal} -autoloadwcfg -tclbatch {cal.tcl}
Vivado Simulator 2018.3
Time resolution is 1 ps
source cal.tcl
## run all
////////////////////////////////////////////////////////////////////////////////
// Inter-Transaction Progress: Completed Transaction / Total Transaction
// Intra-Transaction Progress: Measured Latency / Latency Estimation * 100%
//
// RTL Simulation : "Inter-Transaction Progress" ["Intra-Transaction Progress"]
////////////////////////////////////////////////////////////////////////////////
// RTL Simulation : 0 / 19 [0.00%] @ "125000"
// RTL Simulation : 1 / 19 [192.31%] @ "415000"
// RTL Simulation : 2 / 19 [192.31%] @ "435000"
// RTL Simulation : 3 / 19 [192.31%] @ "455000"
// RTL Simulation : 4 / 19 [192.31%] @ "475000"
// RTL Simulation : 5 / 19 [192.31%] @ "495000"
// RTL Simulation : 6 / 19 [192.31%] @ "515000"
// RTL Simulation : 7 / 19 [192.31%] @ "535000"
// RTL Simulation : 8 / 19 [192.31%] @ "555000"
// RTL Simulation : 9 / 19 [192.31%] @ "575000"
// RTL Simulation : 10 / 19 [192.31%] @ "595000"
// RTL Simulation : 11 / 19 [192.31%] @ "615000"
// RTL Simulation : 12 / 19 [192.31%] @ "635000"
// RTL Simulation : 13 / 19 [192.31%] @ "655000"
// RTL Simulation : 14 / 19 [192.31%] @ "675000"
// RTL Simulation : 15 / 19 [192.31%] @ "695000"
// RTL Simulation : 16 / 19 [192.31%] @ "715000"
// RTL Simulation : 17 / 19 [192.31%] @ "735000"
// RTL Simulation : 18 / 19 [192.31%] @ "755000"
// RTL Simulation : 19 / 19 [100.00%] @ "775000"
////////////////////////////////////////////////////////////////////////////////
$finish called at time : 815 ns : File "/home/sam-admin/git/Training/HLS_Assignm
## quit
INFO: [Common 17-206] Exiting xsim at Fri Mar 24 16:53:34 2023...
INFO: [COSIM 212-316] Starting C post checking ...
ALL THE TEST CASES ARE PASSED!INFO: [COSIM 212-1000] *** C/RTL co-simulation fin
Finished C/RTL cosimulation.
```

13 C/RTL Cosimulation Report

Cosimulation Report for 'cal'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	27	27	27	2	2	2

Export the report(.html) using the Export Wizard

Figure 4: Cosimulation Report