HLS-Assignment 6

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1 Problem Statement

Implement a 16bit shift register in HLS. The module should take 3 inputs: 16bit data value, 16bit shift value, and 1 bit left or right shift flag. Shift value is the value by which you need to shift (in the direction denoted by shift flag) the data value and produce the output (also 16bit). Implement it in the most efficient manner possible.

2 Design Code

```
#include"hls_stream.h"
#include "ap_int.h"
using namespace std;

typedef ap_uint<16> int16;

void a6(int16 a,int16 b, bool s, int16 &out){    //s=0?left:right;
          for(int i=1;i<=b;i++){
//#pragma HLS PIPELINE
#pragma HLS LOOP_TRIPCOUNT
                    if (s==0){
                    a=a*2;       //out = a<<b;    //out = a * 2^b //left shift
                    }

                    else{
                    a=a/2;      //out = a>>b;    //out = a / 2^b //right shift
                    }
          out=a;
          }
}
```

3 Test Bench Code

```
#include "hls_stream.h"
#include "ap_int.h"
#include <iostream>
#include <fstream>
using namespace std;

typedef ap_uint<16> int16;

void a6(int16 a,int16 b, bool s, int16 &out);

int main(){
        ap_uint<16> a,b,out,d;
        bool s,f;
        ifstream in("in.dat");
        ofstream res("out.dat");

        for (int i=0;i<6;i++){
        in>>a>>b>>s>>d;
        a6(a, b, s, out);
        res<<a<<"\t"<<b<<"\t"<<s<<"\t"<<d<<"\t";
        if (out==d){
                res<<out<<"\t"<<"Pass"<<endl;;
        }
        else{
                res<<out<<"\t"<<"Fail"<<endl;
                f++;
        }
        }
   if (f==0){
           cout<<"ALL TEST CASES ARE PASSED!"<<endl;
   }
   else{
           cout<<"ERROR! ALL TEST CASES ARE NOT PASSED"<<endl;
   }

        return 0;
}
```

4 C Simulation Output

```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../../a6.cpp in debug mode
   Generating csim.exe
ALL TEST CASES ARE PASSED!
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************
```

5 in.dat file

```
5 2 0 20
5 2 1 1
10 1 1 5
10 1 0 20
1 7 0 128
1 7 1 0
```

6 out.dat file

5	2	0	20	20	Pass
5	2	1	1	1	Pass
10	1	1	5	5	Pass
10	1	0	20	20	Pass
1	7	0	128	128	Pass
1	7	1	0	0	Pass

7 HLS Resource Consumption

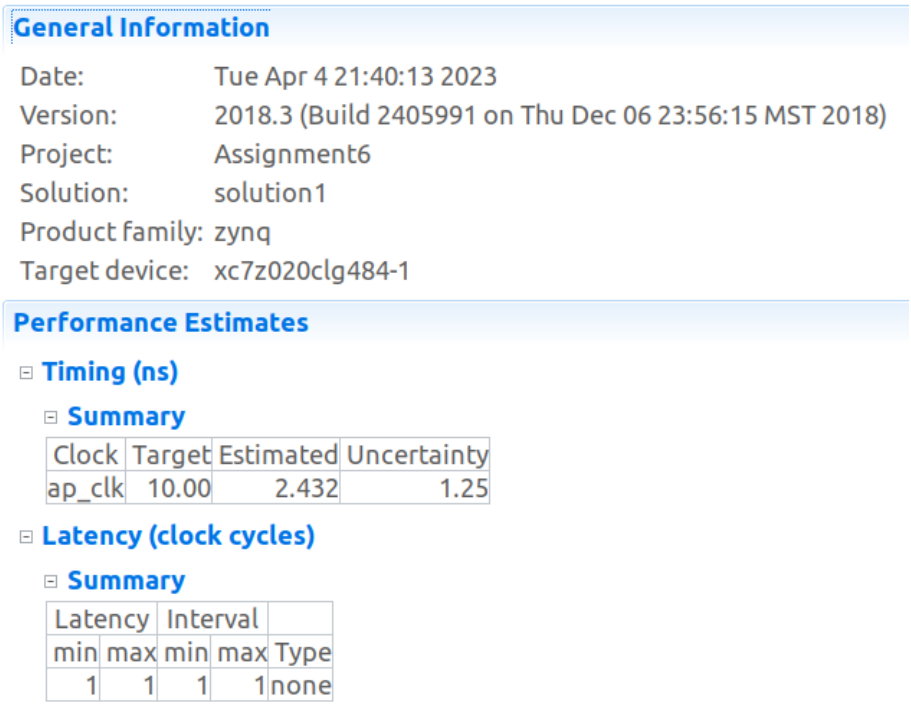
Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	82
FIFO	-	-	-	-
Instance	-	-	-	-
Memory	-	-	-	-
Multiplexer	-	-	-	33
Register	-	-	52	-
Total	0	0	52	115
Available	280	220	106400	53200
Utilization (%)	0	0	~0	~0

Figure 1: Resource Consumption

8 HLS Timing Report



General Information

Date:	Tue Apr 4 21:40:13 2023
Version:	2018.3 (Build 2405991 on Thu Dec 06 23:56:15 MST 2018)
Project:	Assignment6
Solution:	solution1
Product family:	zynq
Target device:	xc7z020clg484-1

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	2.432	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
1	1	1	1	none

Figure 2: Timing Report

9 Interfaces Report

Interface

Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	a6	return value
ap_rst	in	1	ap_ctrl_hs	a6	return value
ap_start	in	1	ap_ctrl_hs	a6	return value
ap_done	out	1	ap_ctrl_hs	a6	return value
ap_idle	out	1	ap_ctrl_hs	a6	return value
ap_ready	out	1	ap_ctrl_hs	a6	return value
a_V	in	16	ap_none	a_V	scalar
b_V	in	16	ap_none	b_V	scalar
s	in	1	ap_none	s	scalar
out_V	out	16	ap_vld	out_V	pointer
out_V_ap_vld	out	1	ap_vld	out_V	pointer

Figure 3: Interface Summmary

10 C/RTL Cosimulation Output

```
Starting C/RTL cosimulation ...
/tools/Xilinx/Vivado/2018.3/bin/vivado_hls /home/sam-admin/git/Training/HLS_Assi
```

```
INFO: [HLS 200-10] Running '/tools/Xilinx/Vivado/2018.3/bin/unwrapped/lnx64.o/vi
INFO: [HLS 200-10] For user 'sam-admin' on host 'sampaths-lappie' (Linux_x86_64
INFO: [HLS 200-10] On os Ubuntu 22.04.2 LTS
INFO: [HLS 200-10] In directory '/home/sam-admin/git/Training/HLS_Assignments/A6
INFO: [HLS 200-10] Opening project '/home/sam-admin/git/Training/HLS_Assignments
INFO: [HLS 200-10] Opening solution '/home/sam-admin/git/Training/HLS_Assignment
INFO: [SYN 201-201] Setting up clock 'default' with a period of 10ns.
INFO: [HLS 200-10] Setting target device to 'xc7z020clg484-1'
INFO: [COSIM 212-47] Using XSIM for RTL simulation.
INFO: [COSIM 212-14] Instrumenting C test bench ...
   Build using "/tools/Xilinx/Vivado/2018.3/tps/lnx64/gcc-6.2.0/bin/g++"
   Compiling a6.cpp_pre.cpp.tb.cpp
   Compiling a6_tb.cpp_pre.cpp.tb.cpp
   Compiling apatb_a6.cpp
   Generating cosim.tv.exe
INFO: [COSIM 212-302] Starting C TB testing ...
ALL TEST CASES ARE PASSED!
INFO: [COSIM 212-333] Generating C post check test bench ...
INFO: [COSIM 212-12] Generating RTL test bench ...
INFO: [COSIM 212-323] Starting verilog simulation.
INFO: [COSIM 212-15] Starting XSIM ...
INFO: [XSIM 43-3496] Using init file passed via -initfile option "/tools/Xilinx/
Vivado Simulator 2018.3
Copyright 1986-1999, 2001-2018 Xilinx, Inc. All Rights Reserved.
Running: /tools/Xilinx/Vivado/2018.3/bin/unwrapped/lnx64.o/xelab xil_defaultlib.
Multi-threading is on. Using 6 slave threads.
WARNING: [XSIM 43-3431] One or more environment variables have been detected whi
If errors occur, try running xelab with the "-mt off -v 1" switches to see more
    LIBRARY_PATH
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module glbl
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module a6
INFO: [VRFC 10-2263] Analyzing SystemVerilog file "/home/sam-admin/git/Training/
INFO: [VRFC 10-311] analyzing module apatb_a6_top
Starting static elaboration
Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module xil_defaultlib.a6
Compiling module xil_defaultlib.apatb_a6_top
Compiling module work.glbl
Built simulation snapshot a6
```

```
****** Webtalk v2018.3 (64-bit)
  **** SW Build 2405991 on Thu Dec  6 23:36:41 MST 2018
  **** IP Build 2404404 on Fri Dec  7 01:43:56 MST 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.


source /home/sam-admin/git/Training/HLS_Assignments/A6/codes/Assignment6/solution
INFO: [Common 17-206] Exiting Webtalk at Tue Apr  4 21:41:24 2023...


****** xsim v2018.3 (64-bit)
  **** SW Build 2405991 on Thu Dec  6 23:36:41 MST 2018
  **** IP Build 2404404 on Fri Dec  7 01:43:56 MST 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.


source xsim.dir/a6/xsim_script.tcl
# xsim {a6} -autoloadwcfg -tclbatch {a6.tcl}
Vivado Simulator 2018.3
Time resolution is 1 ps
source a6.tcl
## run all
////////////////////////////////////////////////////////////////////////////////
// Inter-Transaction Progress: Completed Transaction / Total Transaction
// Intra-Transaction Progress: Measured Latency / Latency Estimation * 100%
//
// RTL Simulation : "Inter-Transaction Progress" ["Intra-Transaction Progress"] @
////////////////////////////////////////////////////////////////////////////////
// RTL Simulation : 0 / 6 [0.00%] @ "125000"
// RTL Simulation : 1 / 6 [100.00%] @ "175000"
// RTL Simulation : 2 / 6 [100.00%] @ "215000"
// RTL Simulation : 3 / 6 [100.00%] @ "245000"
// RTL Simulation : 4 / 6 [100.00%] @ "275000"
// RTL Simulation : 5 / 6 [100.00%] @ "365000"
// RTL Simulation : 6 / 6 [100.00%] @ "455000"
////////////////////////////////////////////////////////////////////////////////
$finish called at time : 495 ns : File "/home/sam-admin/git/Training/HLS_Assignm
## quit
INFO: [Common 17-206] Exiting xsim at Tue Apr  4 21:41:32 2023...
INFO: [COSIM 212-316] Starting C post checking ...
ALL TEST CASES ARE PASSED!
INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***
Finished C/RTL cosimulation.
```

11 C/RTL Cosimulation Report

Cosimulation Report for 'a6'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	2	4	8	3	4	9

Export the report(.html) using the Export Wizard

Figure 4: Cosimulation Report