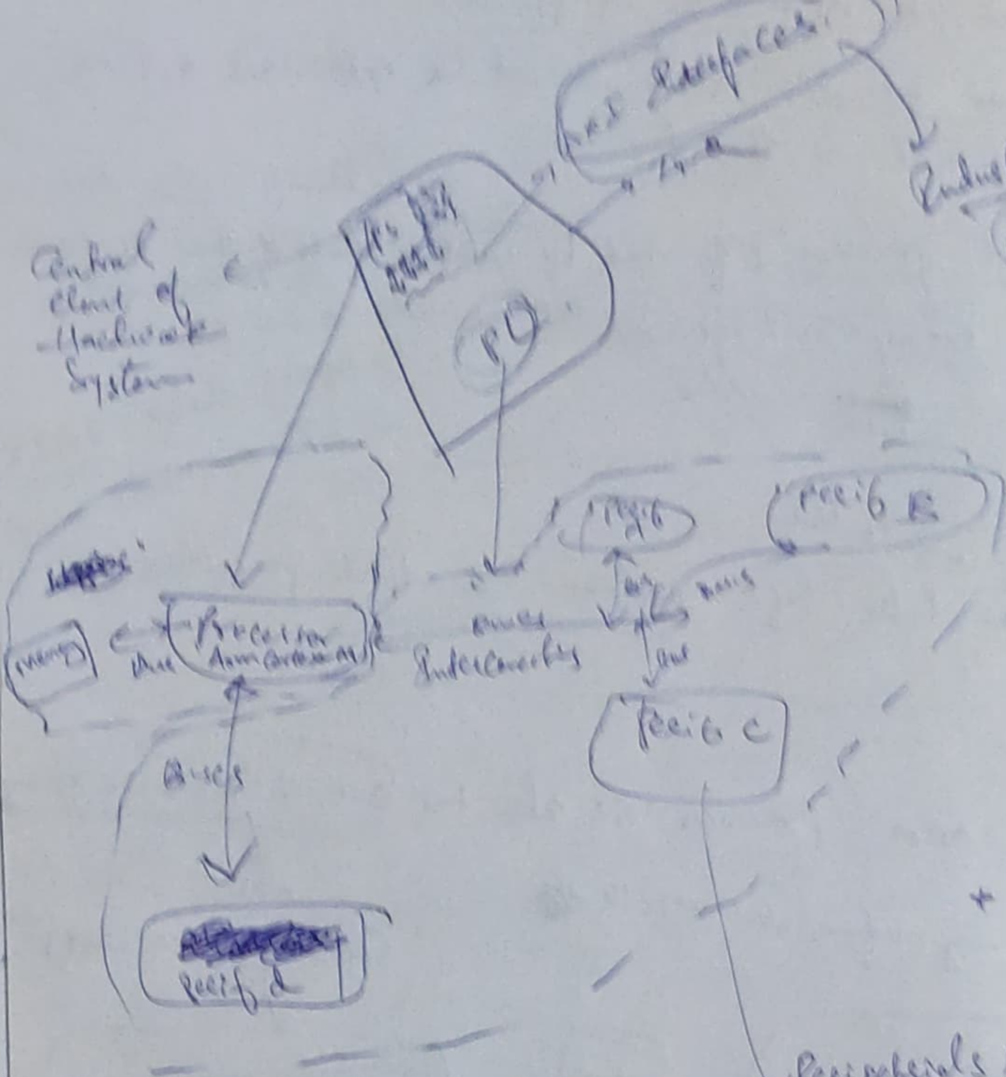


Industry Standard Connections

(Rules) -> Interfaces

* PS & PL Can be used independently or together

* Software run on Processor (Arm A9s)

Peripherals:

* functional Components residing away from Processor
* need to be connected if you want to use.
* 3 main functions:
  - i) Co-processors (ex: Arm)
  - ii) Interacting with external Interfaces (ex: led, Switch, Board)
  - iii) additional memory elements

Industry Standard format

Packed into IP-XACT format -> reusable blocks

* IP's Corresponds to peripheral Components

* Interconnections (<->) are implemented via AXI Interfaces.

* PS has fixed architecture and hosts processor & system memory

* PL completely flexible, we can create custom peripherals (or) reuse standard ones.

PS → Contain dual-core ARM Cortex A9 processor

"Hard Processor" } Has dedicated and optimised silicon element on the device

"Soft Processor" } formed by combining elements of the PL fabric.

Higher Performance than Soft processor

Soft processors

Advantage is that we can use multiple instances of a soft processor

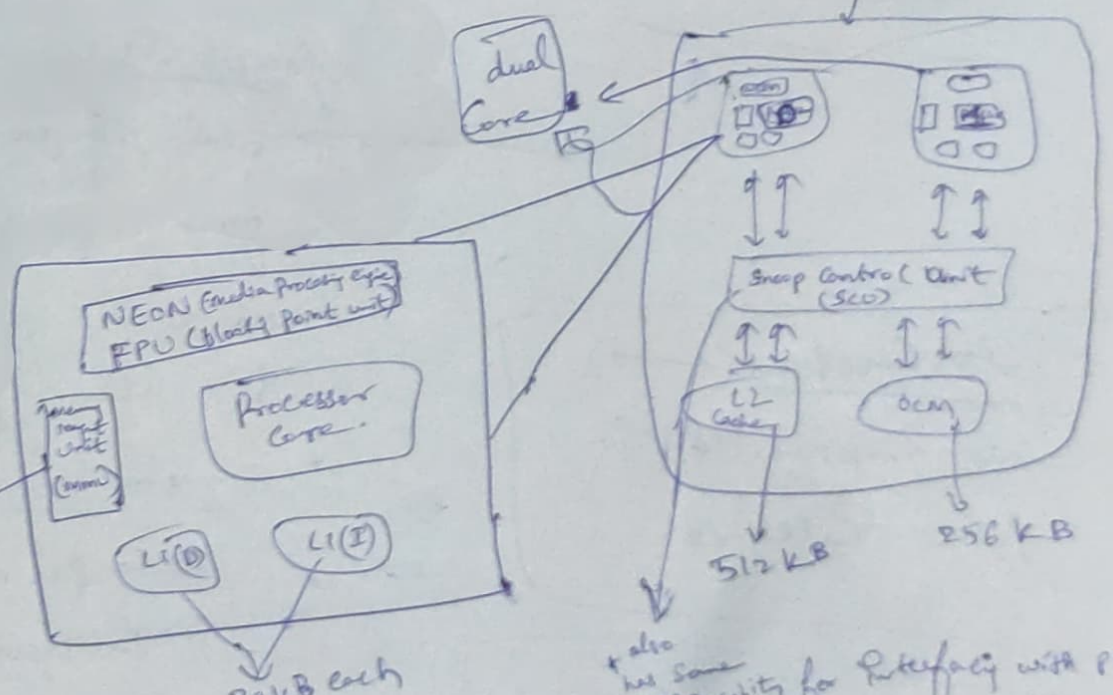
Ex: nios, microBlaze (Xilinx), Intel

* We can use & communicate b/w both Soft Processor & Hard Processor.

* PS is not just ARM processor it also has set of (Processing resources)

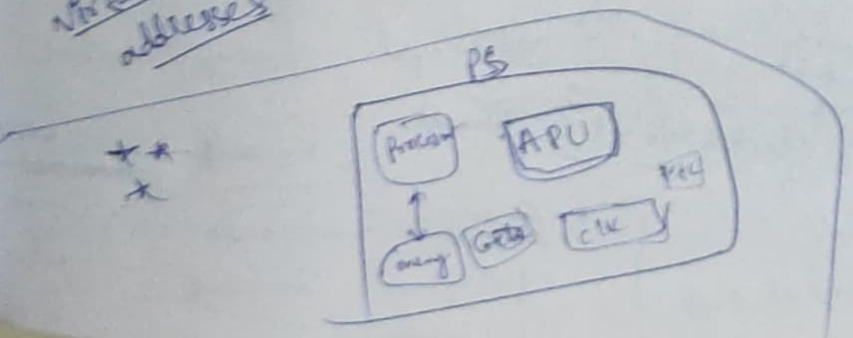
peripheral interfaces, Cache, many interfaces, interconnect, clk.

APU (Application processing unit)



MMU is responsible to translate between virtual & physical addresses.

* also has some responsibility for interface with PL
* ensures cache coherency



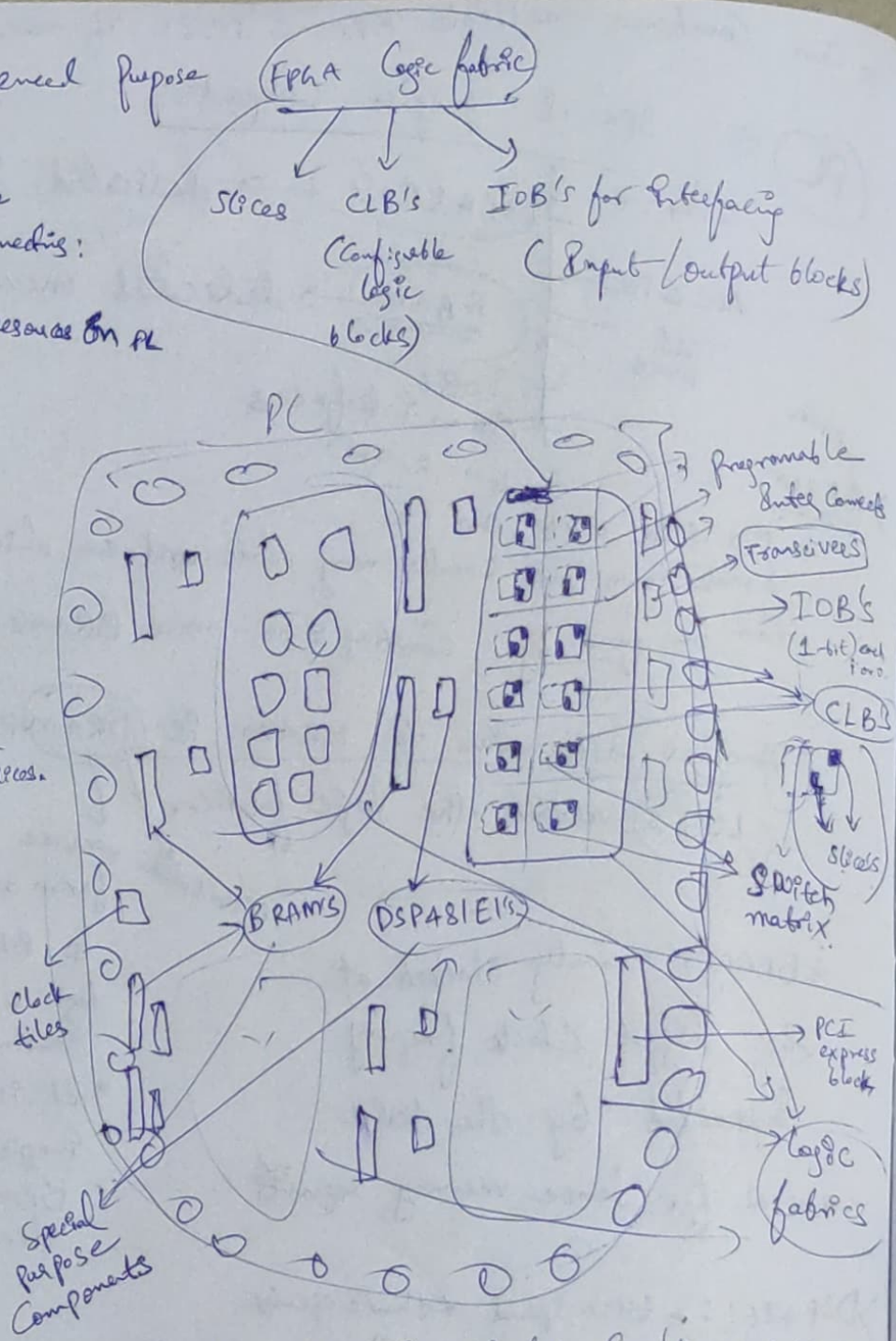
PL → Contain general Purpose FPGA Logic fabric

Slices | CLB's (Configurable logic blocks) | IOB's for Interfacing (Input/output blocks)

> Switch matrix: Provides flexible routing facility for making connections:
i) b/w elents within CLB
ii) from one CLB to other resources on PL

> CLB's: Small groups of logic elements that are laid out in a 2D array on PL & are connected to other similar resources via programable Interconnects.
* Each CLB is positioned next to a switch matrix & contains 2 slices.

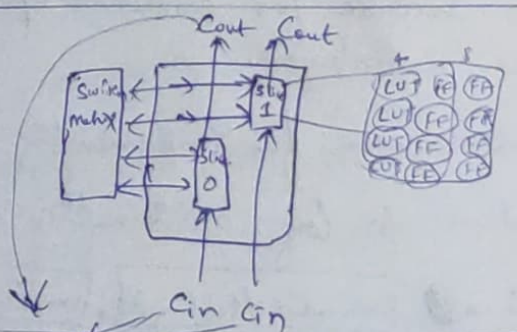
> Slices: Subunit within CLB, which contains resources for implmtg Combntl & Sequentl Ckts.
* Slices are composed of:
4 LUT,
8 F.F, &
other logic.



> LUT: a flexible resource capable of Implmtg
i) A logic fnctn of upto 6 i/ps.
ii) A small ROM
iii) A small RAM
iv) A Shift register

* LUT's can be combined together to form larger logic fnctns, memories, shift registers as required

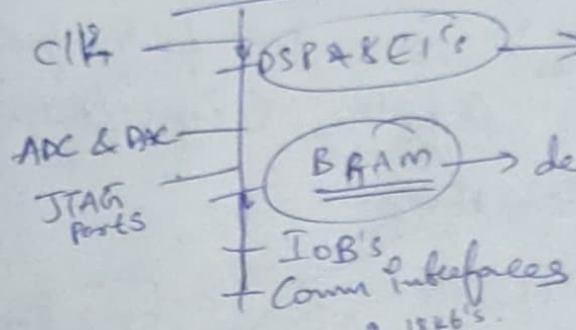
> FF: a Sequentl elt Implmtg a 1 bit reg with reset fncltty. One of the FF can optnlly used to Implmt a latch



> Carry logic: Intermediate Signals to be Propagated b/w adjacent slices.
* Carry logic has chain of routes & mux to link slices in vertical column

* Can Combined multiple BRAS & DSPs if needed.

PL ⇒ Special purpose Compats:



> BRAM: (Block)

* Max size 36kb. (or 2, 18kb's), Can be break down into smaller memy elmts (word) can also large Capacity memories Can be formed by Combng 2 or more BRAM's together.

* Another Alternative to BRAM is DRAM ⇒ Constructed from the LUT's within the logic fabric.

Distributed

* more LUT's Required to form a memory of Size Comparable to BRAM. This results, Increased logic & area & there will be routing delays.
* It is advantageous only to Implant Small memories using DRAM. for resource efficiency & also their placent is flexible. because they located Close to Compts that Interact with them, resulting fast thly performe

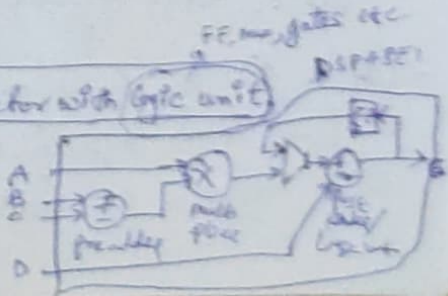
* BRAM's normally Clocked at the highest Clock frequncy Supported by the device
* used for dense memory requirts

> DSP48E1: * High Speed arithmetic operis

* LUT's Can be used to Implent arithmetic operators of any arbitrary length, but are more Suitable for arithmetic operators with short wordlengths.

* DSP48E1's are for implementing high-speed arithmetic on Signals with medium to long arithmetic word lengths.

* Has: • Pre-adder/subtractor, multiplier, post-adder/subtractor with logic unit



* Capable of SIMD Processing, Implenty 2 or 4 shorter addition/subtraction accumulation operations of 24 or 12 bits, respectively

> IOB's: (General purpose I/O).

* They are referred as Select IO Resources, and these are organized into banks of 50 IOB's each.

* Each IOB has 1 pad, which provides the physical connection to the outside world for signals I/P/O/P signal

* I/O banks are categorized as: ① HP (High Performance)
② HR (High Range)

& Support a Variety of I/O standards & voltages.

HP > * Limited to 1.8 V & are typically used for high-speed interfaces to memory & other chips,

HR > * Voltages up to 3.3 V and caters for a wider I/O standards.

* Each IOB also includes an IOSERDES resource for programmable conversion b/w parallel & serial data formats of b/w 2-8 bits.

> Communication Interfaces: → Implemented as quads: i.e, groups of 4 individual channels & each ch has dedicated PLL, Tx, Rx

* GTX Transceivers. } high speed Comm interface blocks which are embedded into the logic fabric.

↓
dedicated "Hard IP" blocks (Silicon blocks)

* Supporting Interfaces: PCI express, Serial rapid IO, SCSI, SATA

* In terms of working use IPs & select HW & parameters

Combinational → LUT
Sequential → FF

Other PL extend Interfaces:

> ADC [redacted]:

* XADC block ⟶ Hard IP.

Mixed Signal Hardware. } Has 2 seperate 12 bit ADC's

* Control of XADC is achieved using the PS-XADC Interface block. located within PS. & programed from s/w executing on APU.

> Clocks:

* PL recieves 4 seperate clock inputs from PS, and additionally has the facilities to generate and distribute its own clock signals independently of the PS.

> JTAG: (Programing & debug)

* A set of JTAG ports are provided in the PL Section to facilitate Configuration and debugging of the PL.

* JTAG Supports debugging with Both ARM & Xilinx tools.