RTL Training Module 1 Report

Assignment 1

- Report from HDL Bits - https://hdlbits.01xz.net/wiki/Special:VlgStats/4D508C5AD5657CD0

Assignment 2

- PPT on FPGA Architecture - https://docs.google.com/presentation/d/1zp_wFhso-R5EQaI97EVB1hKhvtdcXXMh2q-UWjQ5hss/edit?usp=sharing