


















































Stats for sam_fwc71

Problems solved:	142
Problems attempted:	143
Current rank:	3397
Link to this page  (4D508C5AD5657CD0)	

Problem	Success	Incorrect	Compile error	Simulation error	Total attempts	Success rate (%)
1 step_one  (/wiki/step_one)	1	0	0	0	1	100%
2 zero  (/wiki/zero)	1	0	0	0	1	100%
3 wire  (/wiki/wire)	1	0	1	0	2	50%
4 wire4  (/wiki/wire4)	1	0	0	0	1	100%
5 notgate  (/wiki/notgate)	1	0	0	0	1	100%
6 andgate  (/wiki/andgate)	1	0	0	0	1	100%
7 norgate  (/wiki/norgate)	1	0	0	0	1	100%
8 xnorgate  (/wiki/xnorgate)	1	0	0	0	1	100%
9 wire_decl  (/wiki/wire_decl)	1	0	0	0	1	100%
10 7458  (/wiki/7458)	1	0	0	0	1	100%
11 vector0  (/wiki/vector0)	1	0	0	0	1	100%
12 vector1  (/wiki/vector1)	2	0	0	0	2	100%
13 vector2  (/wiki/vector2)	1	0	0	0	1	100%
14 vectorgates  (/wiki/vectorgates)	1	2	1	0	4	25%
15 gates4  (/wiki/gates4)	1	0	1	0	2	50%
16 vector3  (/wiki/vector3)	1	0	1	0	2	50%
17 vectorr  (/wiki/vectorr)	1	0	8	0	9	11%
18 vector4  (/wiki/vector4)	1	2	1	0	4	25%
19 vector5  (/wiki/vector5)	1	0	0	0	1	100%
20 module  (/wiki/module)	2	0	2	0	4	50%
21 module_pos  (/wiki/module_pos)	1	0	1	0	2	50%
22 module_name  (/wiki/module_name)	1	0	2	0	3	33%
23 module_shift  (/wiki/module_shift)	1	0	1	0	2	50%
24 module_shift8  (/wiki/module_shift8)	1	4	0	0	5	20%
25 module_add  (/wiki/module_add)	1	9	5	0	15	7%
26 module_fadd  (/wiki/module_fadd)	1	1	0	0	2	50%
27 module_cseladd  (/wiki/module_cseladd)	1	0	0	0	1	100%
28 module_addsub  (/wiki/module_addsub)	1	1	1	0	3	33%
29 alwaysblock1  (/wiki/alwaysblock1)	1	0	1	0	2	50%
30 alwaysblock2  (/wiki/alwaysblock2)	1	0	0	0	1	100%
31 always_if  (/wiki/always_if)	1	0	0	0	1	100%
32 always_if2  (/wiki/always_if2)	1	0	0	0	1	100%
33 always_case  (/wiki/always_case)	2	0	2	0	4	50%
34 always_case2  (/wiki/always_case2)	2	0	2	0	4	50%
35 always_casez  (/wiki/always_casez)	1	1	1	0	3	33%
36 always_nolatches  (/wiki/always_nolatches)	1	3	0	0	4	25%
37 conditional  (/wiki/conditional)	1	1	0	0	2	50%
38 reduction  (/wiki/reduction)	1	1	1	0	3	33%
39 gates100  (/wiki/gates100)	1	0	0	0	1	100%
40 vector100r  (/wiki/vector100r)	4	3	8	0	15	27%
41 popcount255  (/wiki/popcount255)	1	4	3	0	8	13%
42 adder100i  (/wiki/adder100i)	1	2	7	0	10	10%
43 bcdadd100  (/wiki/bcdadd100)	1	0	0	0	1	100%
44 exams/m2014_q4h  (/wiki/exams/m2014_q4h)	1	0	0	0	1	100%
45 exams/m2014_q4i  (/wiki/exams/m2014_q4i)	1	0	0	0	1	100%
46 exams/m2014_q4e  (/wiki/exams/m2014_q4e)	1	0	0	0	1	100%
47 exams/m2014_q4f  (/wiki/exams/m2014_q4f)	1	0	0	0	1	100%
48 exams/m2014_q4g  (/wiki/exams/m2014_q4g)	1	0	0	0	1	100%
Attempts:	157	116	108	9	390	40%
Problems:	142				143	99%

Problem	Success	Incorrect	Compile error	Simulation error	Total attempts	Success rate (%)
49 gates👍 (/wiki/gates)	1	0	0	0	1	100%
50 7420👍 (/wiki/7420)	1	0	0	0	1	100%
51 truthtable1👍 (/wiki/truthtable1)	1	1	0	0	2	50%
52 mt2015_eq2👍 (/wiki/mt2015_eq2)	1	0	0	0	1	100%
53 mt2015_q4a👍 (/wiki/mt2015_q4a)	1	0	0	0	1	100%
54 mt2015_q4b👍 (/wiki/mt2015_q4b)	1	0	0	0	1	100%
55 mt2015_q4👍 (/wiki/mt2015_q4)	1	2	0	0	3	33%
56 ringer👍 (/wiki/ringer)	1	2	3	0	6	17%
57 thermostat👍 (/wiki/thermostat)	1	1	0	0	2	50%
58 popcount3👍 (/wiki/popcount3)	1	0	0	0	1	100%
59 gatesv👍 (/wiki/gatesv)	1	1	0	0	2	50%
60 gatesv100👍 (/wiki/gatesv100)	1	0	0	0	1	100%
61 mux2to1👍 (/wiki/mux2to1)	2	0	0	0	2	100%
62 mux2to1v👍 (/wiki/mux2to1v)	2	0	0	0	2	100%
63 mux9to1v👍 (/wiki/mux9to1v)	2	0	0	0	2	100%
64 mux256to1👍 (/wiki/mux256to1)	1	0	1	0	2	50%
65 mux256to1v👍 (/wiki/mux256to1v)	1	0	2	0	3	33%
66 hadd👍 (/wiki/hadd)	1	0	0	0	1	100%
67 fadd👍 (/wiki/fadd)	1	0	0	0	1	100%
68 adder3👍 (/wiki/adder3)	1	2	3	0	6	17%
69 exams/m2014_q4j👍 (/wiki/exams/m2014_q4j)	1	1	2	0	4	25%
70 exams/ece241_2014_q1c👍 (/wiki/exams/ece241_2014_q1c)	1	1	1	0	3	33%
71 adder100👍 (/wiki/adder100)	1	0	0	0	1	100%
72 bcdadd4👍 (/wiki/bcdadd4)	1	0	0	0	1	100%
73 kmap1👍 (/wiki/kmap1)	1	0	0	0	1	100%
74 kmap2👍 (/wiki/kmap2)	1	0	0	0	1	100%
75 kmap3👍 (/wiki/kmap3)	1	2	0	0	3	33%
76 kmap4👍 (/wiki/kmap4)	1	1	0	0	2	50%
77 exams/ece241_2013_q2👍 (/wiki/exams/ece241_2013_q2)	1	1	2	0	4	25%
78 exams/m2014_q3👍 (/wiki/exams/m2014_q3)	1	0	0	0	1	100%
79 exams/2012_q1g👍 (/wiki/exams/2012_q1g)	1	0	0	0	1	100%
80 exams/ece241_2014_q3👍 (/wiki/exams/ece241_2014_q3)	1	0	0	0	1	100%
81 dff👍 (/wiki/dff)	1	0	0	0	1	100%
82 dff8👍 (/wiki/dff8)	1	0	0	0	1	100%
83 dff8r👍 (/wiki/dff8r)	1	0	1	0	2	50%
84 dff8p👍 (/wiki/dff8p)	1	0	2	0	3	33%
85 dff8ar👍 (/wiki/dff8ar)	1	1	0	0	2	50%
86 dff16e👍 (/wiki/dff16e)	1	2	0	0	3	33%
87 exams/m2014_q4a👍 (/wiki/exams/m2014_q4a)	1	0	0	0	1	100%
88 exams/m2014_q4b👍 (/wiki/exams/m2014_q4b)	1	0	0	0	1	100%
89 exams/m2014_q4c👍 (/wiki/exams/m2014_q4c)	1	0	0	0	1	100%
90 exams/m2014_q4d👍 (/wiki/exams/m2014_q4d)	1	0	0	0	1	100%
91 mt2015_muxdff👍 (/wiki/mt2015_muxdff)	1	0	0	0	1	100%
92 exams/2014_q4a👍 (/wiki/exams/2014_q4a)	1	0	0	0	1	100%
93 exams/ece241_2014_q4👍 (/wiki/exams/ece241_2014_q4)	1	0	0	0	1	100%
94 exams/ece241_2013_q7👍 (/wiki/exams/ece241_2013_q7)	1	0	0	0	1	100%
95 edgedetect👍 (/wiki/edgedetect)	1	0	0	0	1	100%
96 edgedetect2👍 (/wiki/edgedetect2)	1	1	2	0	4	25%
97 edgecapture👍 (/wiki/edgecapture)	1	1	0	0	2	50%
98 dualedge👍 (/wiki/dualedge)	1	0	1	0	2	50%
99 count15👍 (/wiki/count15)	1	0	0	0	1	100%
100 count10👍 (/wiki/count10)	1	0	0	0	1	100%
101 count1to10👍 (/wiki/count1to10)	1	0	0	0	1	100%
102 countslow👍 (/wiki/countslow)	2	8	2	0	12	17%
103 exams/ece241_2014_q7a👍 (/wiki/exams/ece241_2014_q7a)	1	0	2	0	3	33%
104 exams/ece241_2014_q7b👍 (/wiki/exams/ece241_2014_q7b)	1	0	0	0	1	100%
105 countbcd👍 (/wiki/countbcd)	1	0	0	0	1	100%
Attempts:	157	116	108	9	390	40%
Problems:	142				143	99%

Problem	Success	Incorrect	Compile error	Simulation error	Total attempts	Success rate (%)
106 count_clock👍 (/wiki/count_clock)	1	10	0	0	11	9%
107 shift4👍 (/wiki/shift4)	2	0	1	3	6	33%
108 rotate100👍 (/wiki/rotate100)	1	2	1	0	4	25%
109 shift18👍 (/wiki/shift18)	1	1	0	0	2	50%
110 lfsr5👍 (/wiki/lfsr5)	2	1	1	0	4	50%
111 mt2015_lfsr👍 (/wiki/mt2015_lfsr)	1	0	1	0	2	50%
112 lfsr32👍 (/wiki/lfsr32)	1	0	0	0	1	100%
113 exams/m2014_q4k👍 (/wiki/exams/m2014_q4k)	1	0	0	0	1	100%
114 exams/2014_q4b👍 (/wiki/exams/2014_q4b)	1	0	4	0	5	20%
115 exams/ece241_2013_q12👍 (/wiki/exams/ece241_2013_q12)	1	0	1	0	2	50%
116 rule90👎 (/wiki/rule90)	0	5	13	0	18	0%
117 fsm1👍 (/wiki/fsm1)	1	0	1	0	2	50%
118 exams/review2015_count1k👍 (/wiki/exams/review2015_count1k)	1	0	0	0	1	100%
119 exams/review2015_shiftcount👍 (/wiki/exams/review2015_shiftcount)	2	4	0	0	6	33%
120 exams/review2015_fsmseq👍 (/wiki/exams/review2015_fsmseq)	1	1	1	0	3	33%
121 exams/review2015_fsmshift👍 (/wiki/exams/review2015_fsmshift)	1	9	0	0	10	10%
122 bugs_mux2👍 (/wiki/bugs_mux2)	1	2	0	0	3	33%
123 bugs_nand3👍 (/wiki/bugs_nand3)	1	0	1	0	2	50%
124 bugs_mux4👍 (/wiki/bugs_mux4)	1	0	1	0	2	50%
125 bugs_addsubz👍 (/wiki/bugs_addsubz)	1	1	0	0	2	50%
126 bugs_case👍 (/wiki/bugs_case)	1	6	0	0	7	14%
127 sim/circuit1👍 (/wiki/sim/circuit1)	1	0	0	0	1	100%
128 sim/circuit2👍 (/wiki/sim/circuit2)	1	1	0	0	2	50%
129 sim/circuit3👍 (/wiki/sim/circuit3)	1	1	0	0	2	50%
130 sim/circuit4👍 (/wiki/sim/circuit4)	1	0	0	0	1	100%
131 sim/circuit5👍 (/wiki/sim/circuit5)	1	0	0	0	1	100%
132 sim/circuit6👍 (/wiki/sim/circuit6)	1	0	2	0	3	33%
133 sim/circuit7👍 (/wiki/sim/circuit7)	1	0	0	0	1	100%
134 sim/circuit8👍 (/wiki/sim/circuit8)	1	2	1	0	4	25%
135 sim/circuit9👍 (/wiki/sim/circuit9)	1	1	0	0	2	50%
136 sim/circuit10👍 (/wiki/sim/circuit10)	1	0	0	0	1	100%
137 tb/clock👍 (/wiki/tb/clock)	1	0	1	0	2	50%
138 tb/tb1👍 (/wiki/tb/tb1)	1	0	0	0	1	100%
139 tb/and👍 (/wiki/tb/and)	1	0	1	2	4	25%
140 tb/tb2👍 (/wiki/tb/tb2)	1	0	1	3	5	20%
141 tb/tff👍 (/wiki/tb/tff)	1	0	0	0	1	100%
142 cs450/timer👍 (/wiki/cs450/timer)	2	6	0	0	8	25%
143 cs450/counter_2bc👍 (/wiki/cs450/counter_2bc)	1	1	2	1	5	20%
Attempts:	157	116	108	9	390	40%
Problems:	142				143	99%

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