SAM E70 / SAM S70

Atmel | SMART ARM-based Flash MCU

ERRATA

Scope

This document contains the known errata found on the following Atmel® | SMART SAM E70 and SAM S70 devices:

ATSAME70Q21A-CN-ES2	ATSAMS70Q21A-CN-ES2
ATSAME70Q21A-AN-ES2	ATSAMS70Q21A-AN-ES2
ATSAME70N21A-CN-ES2	ATSAMS70N21A-CFN-ES2
ATSAME70N21A-AN-ES2	ATSAMS70N21A-CN-ES2
ATSAME70J21A-AN-ES2	ATSAMS70N21A-AN-ES2
	ATSAMS70J21A-AN-ES2

Errata Topics

1. Errata

1.1 ARM® Cortex®-M7

Issue: **All issues related to the ARM r0p1 core are described on the ARM site.**

Workaround: Refer to ARM documentation:

- ARM Processor Cortex-M7 (AT610) and Cortex-M7 with FPU (AT611) Software Developers Errata Notice
- ARM Embedded Trace Macrocell CoreSight ETM–M7 (TM975) Software Developers Errata Notice

1.2 Backup Mode Power Consumption

Issue: **Backup power consumption is higher than expected**

Power consumption on VDDIO in Backup mode is up to 11 µA without backup SRAM and up to 35 µA with backup SRAM.

Resolution: Fixed in parts marked -ES3 and in production silicon.

1.3 Digital-to-Analog Controller (DAC)

Issue: **Expected performances are not achieved on the full power supply range**

Applying VDDIO below 2.5V leads to reduced DAC performances.

DNL, INL, offset, will be ±65mV, ±35mV and ±30mV, respectively, instead of, ±5mV, ±7mV and ±8mV in the [2.5 : 3.6V] range.

Workaround: Apply VDDIO power supply in the range [2.5 : 3.6V].

1.4 Master CAN-FD Controller (MCAN)

Issue: **Flexible data rate is not fully supported**

CAN-FD peripheral does not support the new CRC scheme introduced by the ISO standardization committee.

CAN 2.0 operation is not impacted.

Workaround: None.

1.5 Extended DMA Controller (XDMAC)

Issue: **Issue with byte and half-word accesses to TCM**

If TCM accesses are generated through the AHBS port of the core, only 32-bit accesses are supported. Accesses which are not 32-bit aligned may overwrite bytes at the beginning and at the end of 32-bit words.

Workaround: The user must use 32-bit aligned buffers and buffers with size of a multiple of 4 bytes when transferring data to or from the TCM through the AHBS port of the core.

1.6 AHB Peripheral Port (AHBP)

Issue: **Access with frequency ratio different from 1 and 1/2 may fail**

Peripheral accesses done through the AHBP with a core/bus ratio of 1/3 and 1/4 may lead to unpredictable results.

Workaround: The user must use a core/bus frequency ratio of 1 or 1/2.

1.7 AHB Slave Port (AHBS)

Issue: **Latency on accesses with frequency ratio different from 1**

DMA accesses done through the AHBS to the TCM with a core/bus ratio of 1/2, 1/3 and 1/4 may lead to latency due to one wait state added to the access from the bus to AHBS.

Workaround: The user must use only the core/bus frequency ratio of 1 to guarantee the length of the access.

1.8 Serial Synchronous Controller (SSC)

Issue: **Inverted left/right channels**

In some cases of overflow, a left/right channel inversion may occur.

In this case, the SSC must be re-initialized.

Workaround: None.

1.9 Power Management Controller (PMC)

Issue: **SleepWalking is not working with division by 8**

UART and TWIHS clock can be divided to reduce power consumption. If the divider is 8, SleepWalking is not functional.

Workaround: None.

2. Revision History

Table 2-1. SAM VE70/S70 Errata – Revision History

Doc. Rev. 44027A	Change
17-Mar-15	First issue

Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**