AKD4618-A

AK4618 Evaluation Board Rev.0

GENERAL DESCRIPTION

The AKD4618-A is an evaluation board for AK4618, which is a 24bit CODEC including 6ch ADC and 12ch DAC. The control settings of this board may be controlled via USB port, allowing for easy A/D and D/A evaluation. RCA connectors are used for the input and output of the analog signals. This board also has a digital interface which can be connected to the digital audio system via optical connector.

■ **Ordering guide**

AKD4618-A --- Evaluation board for AK4618
Control software included with package

FUNCTION

- ☐ **Clock generator circuits (AK4118A used)**
- ☐ **Compatible with 2 types of digital audio interface**
  - **Optical input (x1) / Optical output (x1)**
  - **10pin header for external data source**
- ☐ **RCA connector for external clock input**
- ☐ **ADC 6ch input, DAC 12ch output**
- ☐ **USB port for board control**

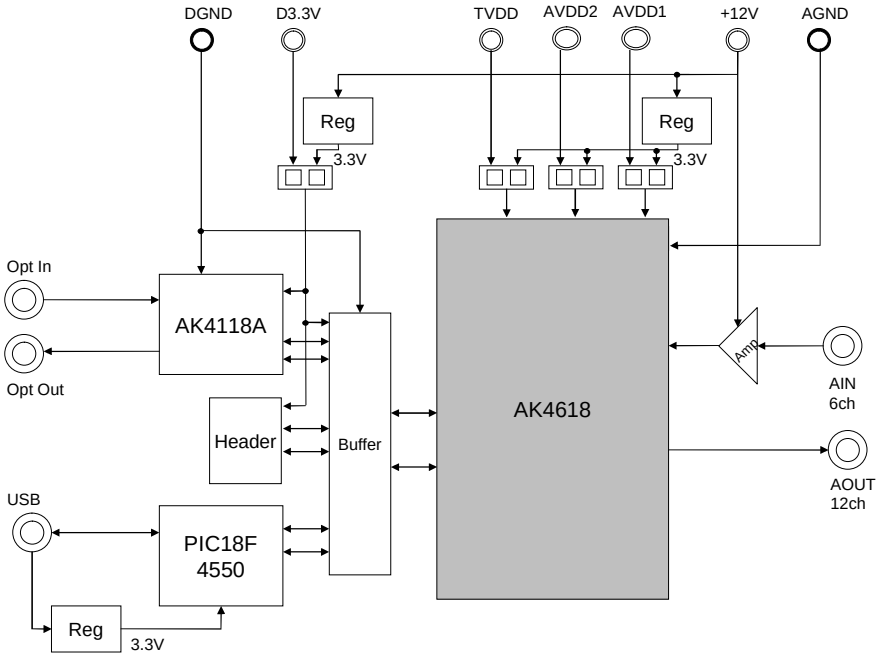

Figure 1. AKD4618-A Block Diagram

Evaluation Board Diagram

■ Board Diagram

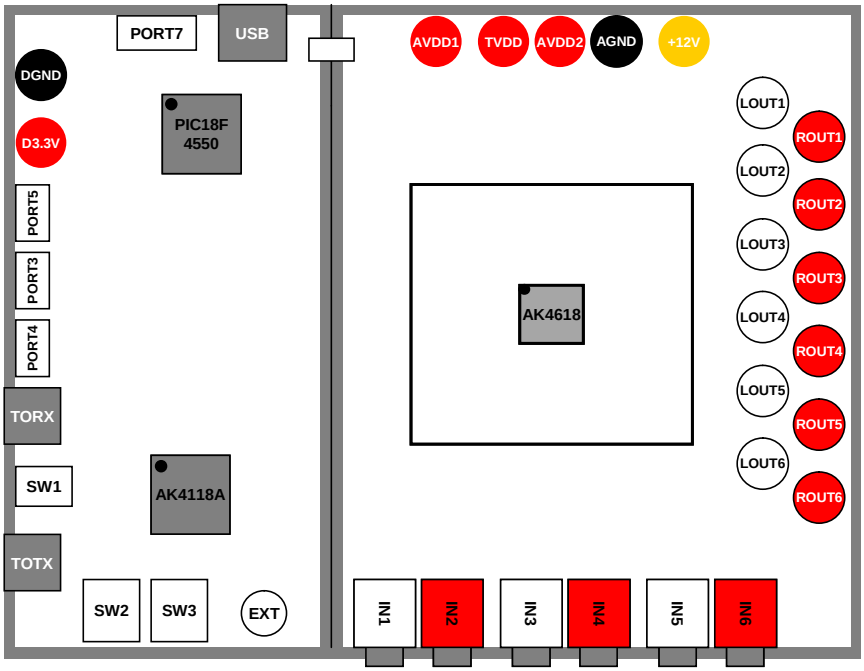

Figure 2. AKD4618-A Board Diagram

■ Description

(1) IN1-IN6; L/ROUT1- L/ROUT6 (RCA Jack)
IN1-6;: Analog input jacks for IN1-6..
L/ROUT1-6: Analog output jacks for L/ROUT1-6.
White jacks are used for left channel and red ones are used for right channel.

(2) AK4118A
AK4118A has DIR, DIT and X'tal oscillator. Transports input data to AK4618 when working in master mode, and output data from AK4618 when working in slave mode.

(3) TORX/TOTX (Optical Connector)
TORX PORT1: Input optical signal to AK4118A
TOTX PORT2: Output optical signal from AK4118A.

(4) +12V/AVDD1/AVDD2/TVDD/D3.3V/AVSS/DGND (Power supply)
+12V: +12V Power Supply
AVDD1-2,TVDD: +3.3V Power Supply
D3.3V: +3V Power Supply
Connect to +12V and GND according to the following operation sequence.

(5) PIC18F4550
USB control chip. Sets up AK4618 registers from PC via USB port.

(6) SW1
DIP type switch. Sets clock and audio format of AK4118A. DIF[2:0] used to set audio interface format and OCKS[1:0] used to master clock frequency. Please refer to Table 3. SW1 Setting, Table 4. Audio format, Table 5. Master Clock Frequency Select for details.

(7) SW2
Toggle type switch. Power-down switch for AK4118A.

(8) SW3
Toggle type switch. Power-down switch for AK4618. Reset board by bringing down SW2 once upon power-up.

(9) PORT3 (6-pin header)
DSP port. Input/output MCLK, BICK, LRCK

(10) PORT4 (12-pin header)
DSP port. Input SDTI1, SDTI2, SDTI3, SDTI4, SDTI5, SDTI6.

(11) PORT5 (6-pin header)
DSP port. Output SDTO1, SDTO2, SDTO3

(12) EXT (RCA jack)
Input external clock source.

Evaluation Board Manual

■ Operation sequence

[1] Power supply line settings

[2] Jumper pins settings

[3] DIP switches settings

[4] Toggle switches settings

[5] LED indication

[6] Register control (Serial control)

[7] Evaluation modes

Refer to the following pages for details.

[1] Power Supply Line Settings

Name	Color	Voltage Range	Typ Voltages	Function	Comments	Default Settings
+12V	Red	+9~+12V	+12V	Regulator power supply OPAmp +terminal power supply	Should always be connected	+12V
AVDD1	Yellow	+3.0~+3.6V	+3.3V	AK4618 AVDD1	3.3V regulator is used (JP30 = REG) by default, when jack is used (JP30=AVDD1).	REG
AVDD2	Yellow	+3.0~+3.6V	+3.3V	AK4618 AVDD2	3.3V regulator is used (JP31 = REG) by default, when jack is used (JP31=AVDD2).	REG
TVDD	Yellow	+3.0~+3.6V	+3.3V	AK4618 TVDD	3.3V regulator is used (JP32 = REG) by default, when jack is used (JP32=TVDD).	REG
D3.3V	Yellow	+3.0~+3.6V	+3.3V	AK4118A 3.3V, Logic IC power supply	3.3V regulator is used (JP33 = REG) by default, when jack is used (JP33=D3V).	REG
AVSS	Black	0V	0V	Analog ground	Should always be connected	0V
DGND	Black	0V	0V	Digital ground	Should always be connected	0V

Table 1. Power supply line setting

Note 1. Each power supply should be powered up while PDN pin = “L”. The PDN pin may be brought to “H” after all power supplies are powered up. Do not turn off AK4618 while surrounding devices are still powered on and I2C bus is in use.

<Operation procedure>

1) Connect power supply as above.

2) Set up jumper pin and evaluation mode (See below for details)

3) Power-up
Reset AK4618 once by bringing SW3 “L” upon power up.

[2] Jumper Pin Settings

No	Names	JP No.	Default	Functions
1	IN1N	JP1	Open	Select Single-ended/Differential input. Lch Analog Negative input to AK4618 (U1) Open: Single-ended input (default) Short: Differential Input
2	IN1/IN1P	JP3	Single	Select Single-ended/Differential input. Lch Analog Positive input to AK4618 (U1) Single: Single-ended input (default) Diff: Differential Input
3	IN2N	JP2	Open	Select Single-ended/Differential input. Rch Analog Negative input to AK4618 (U1) Open: Single-ended input (default) Short: Differential Input
4	IN2/IN2P	JP4	Single	Select Single-ended/Differential input. Rch Analog Positive input to AK4618 (U1) Single: Single-ended input (default) Diff: Differential Input
5	IN3N	JP5	Open	Select Single-ended/Differential input. Lch Analog Negative input to AK4618 (U1) Open: Single-ended input (default) Short: Differential Input
6	IN3/IN3P	JP7	Single	Select Single-ended/Differential input. Lch Analog Positive input to AK4618 (U1) Single: Single-ended input (default) Diff: Differential Input
7	IN4N	JP6	Open	Select Single-ended/Differential input. Rch Analog Negative input to AK4618 (U1) Open: Single-ended input (default) Short: Differential Input
8	IN4/IN4P	JP8	Single	Select Single-ended/Differential input. Rch Analog Positive input to AK4618 (U1) Single: Single-ended input (default) Diff: Differential Input
9	IN5N	JP9	Open	Select Single-ended/Differential input. Lch Analog Negative input to AK4618 (U1) Open: Single-ended input (default) Short: Differential Input
10	IN5/IN5P	JP11	Single	Select Single-ended/Differential input. Lch Analog Positive input to AK4618 (U1) Single: Single-ended input (default) Diff: Differential Input
11	IN6N	JP10	Open	Select Single-ended/Differential input. Rch Analog Negative input to AK4618 (U1) Open: Single-ended input (default) Short: Differential Input
12	IN6/IN6P	JP12	Single	Select Single-ended/Differential input. Rch Analog Positive input to AK4618 (U1) Single: Single-ended input (default) Diff: Differential Input

13	BICK-SEL	JP13	DIR	Select input to AK4618 (U1) BICK Buffer 64fs: 64fs divider 32fs: 32fs divider DIR: DIR-AK4118A-BICK (default) PORT3: PORT3-BICK Open: No signal
14	BICK-PHASE	JP14	THR	Select polarity (non-inverted output / inverted output) of BICK_SEL outputs. THR: Non-inverted output. (default) INV: Inverted output.
15	LRCK-SEL	JP15	DIR	Select input to AK4618 (U1) LRCK Buffer 1fs: 1fs divider DIR: DIR-AK4118A-BICK (default) PORT3: PORT3-BICK Open: No signal
16	MCKI-SEL	JP25	DIR	PORT3: PORT3-MCKI EXT: External MCLK (JACK: J19) input GND: GND DIR: DIR-AK4118A-MCKI (default)
17	SDTI6-SEL	JP16	DIR	Select input to AK4618 (U1) SDTI6 DIR: DIR-AK4118A-SDTO (default) PORT4: PORT4-SDTI6 GND: Digital ground
18	SDTI5-SEL	JP18	DIR	Select input to AK4618 (U1) SDTI5 DIR: DIR-AK4118A-SDTO (default) PORT4: PORT4-SDTI5 GND: Digital ground
19	SDTI4-SEL	JP21	DIR	Select input to AK4618 (U1) SDTI4 DIR: DIR-AK4118A-SDTO (default) PORT4: PORT4-SDTI4 GND: Digital ground
20	SDTI3-SEL	JP22	DIR	Select input to AK4618 (U1) SDTI3 DIR: DIR-AK4118A-SDTO (default) PORT4: PORT4-SDTI3 GND: Digital ground
21	SDTI2-SEL	JP23	DIR	Select input to AK4618 (U1) SDTI3 DIR: DIR-AK4118A-SDTO (default) PORT4: PORT4-SDTI2 GND: Digital ground
22	SDTI1-SEL	JP24	DIR	Select input to AK4618 (U1) SDTI3 DIR: DIR-AK4118A-SDTO (default) PORT4: PORT4-SDTI1 GND: Digital ground
23	EXT	JP27	Open	Open: No input (default) Short: External MCLK(JACK: J19) input
24	DAUX-SEL	JP28	SDTO1	Select input to DIT:AK4118A (U8) DAUX SDTO1: AK4618A-SDTO1 (default) SDTO2: AK4618A-SDTO2 SDTO3: AK4618A-SDTO2
25	PIC	JP29	Open	Connect PIC microchip connector VDD(pin.1),MCLR(pin.2),PGD(pin.3),PGC(pin.4),GND(pin.5)

26	AVDD-SEL	JP30	REG	Select power supply to AVDD1 REG: Regulator T2 (default) (When regulator "T2" is selected, power supply jack "AVDD1" should be open.) JACK: Power supply jack J21 "AVDD1"
27	AVDD2-SEL	JP22	REG	Select power supply to AVDD2 REG: Regulator T2 (default) (When regulator "T2" is selected, power supply jack "AVDD2" should be open.) JACK: Power supply jack J22 "AVDD2"
28	TVDD-SEL	JP23	REG	Select power supply to TVDD REG: Regulator T2 (default) (When regulator "T2" is selected, power supply jack "TVDD" should be open.) JACK: Power supply jack J23 "TVDD"
29	D3.3V-SEL	JP24	REG	Select power supply to D3.3V REG: Regulator T3 (default) (When regulator "T3" is selected, power supply jack "D3.3V" should be open.) JACK: Power supply jack J24 "D3.3V"
30	GND	JP34	Short	Select connection / separation between analog ground and digital ground. Open: Separate analog ground from digital ground Short: Connect analog ground to digital ground (default)

Table 2. Main board Jumper pin setting

[3] DIP switch setting

(1). Setting for SW1 (Sets AK4118A (U8) audio format and master clock setting)

No.	Switch Name	Function	default
1	DIF0	Set-up of DIF0 pin. (in parallel mode)	H
2	DIF1	Set-up of DIF1 pin. (in parallel mode)	L
3	DIF2	Set-up of DIF2 pin. (in parallel mode)	H
4	OCKS1	Set-up of OCKS1 pin. (in parallel mode)	L
5	OCKS0	Set-up of OCKS0 pin. (in parallel mode)	L

Table 3. SW1 Setting

Mode	DIF2 pin (SW1_1)	DIF1 pin (SW1_2)	DIF0 pin (SW1_3)	DAUX	SDTO	LRCK		BICK		
	DIF2 bit	DIF1 bit	DIF0 bit				I/O		I/O	
0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
1	0	0	1	24bit, Left justified	18bit, Right justified	H/L	O	64fs	O	
2	0	1	0	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
3	0	1	1	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
4	1	0	0	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	
5	1	0	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	default
6	1	1	0	24bit, Left justified	24bit, Left justified	H/L	I	64-128fs	I	
7	1	1	1	24bit, I^2S	24bit, I^2S	L/H	I	64-128fs	I	

Table 4. Audio format

OCKS1 pin (SW1_4)	OCKS0 pin (SW1_5)	(X'tal)	MCKO1	MCKO2	fs (max)	
OCKS1 bit	OCKS0 bit					
0	0	256fs	256fs	256fs	96 kHz	default
0	1	256fs	256fs	128fs	96 kHz	
1	0	512fs	512fs	256fs	48 kHz	
1	1	128fs	128fs	64fs	192 kHz	

Table 5. Master Clock Frequency Select

[4] Toggle switch settings

SW2, SW3 Settings

SW2	4118-PDN	Power down switch for DIR/T: AK4118A (U8). Reset AK4118A (U8) once by brining SW2 to "L" once upon power-up. Keep "H" when AK4118A is in use; keep "L" when AK4118A is not in use.
SW3	4618-PDN	Power down switch for AK4618 (U1). Reset AK4618 (U1) once by brining SW3 to "L" once upon power-up. Keep "H" during normal operation.

Table 6. Toggle switch settings

[5] LED

LE1 Indication

LE1	INT0	DIR: AK4118A (U8) INT0 pin output. Turns on when DIR: AK4118A (U8) is unlocked

Table 7. LED Indication

[6] Evaluation modes

(1) ADC (Analog → Digital): Stereo ADC

(2) DAC (Digital → Analog)

(1) ADC (Analog → Digital)

■ **Toggle switch setting:**

SW2	SW3
H	L→H
AK4118A(U8) : Used	AK4618(U1) : Used

Table 8. Toggle switch setting

■ **Power management of ADC**

Set Addr: 00H = "7F" to release Internal timing reset and power on ADC. Other control register settings are default.

RSTN bit: Internal timing reset
0: Reset.
1: Normal operation (default)

PMADC bit: Power management of mono-stereo
0: All ADC's power-down
1: Normal operation (default)

PMADC12/PMADC34/PMADC56 bit: Power management of ADC1-6 (0: Power-down, 1: Normal operation)
PMADC12 bit: Power management control of ADC1 and ADC2
PMADC34 bit: Power management control of ADC3 and ADC4
PMADC56 bit: Power management control of ADC5 and ADC6

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	MS	PMMB	PMADC	PMDAC	PMADC56	PMADC34	PMADC12	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Setting		0	1	1	1	1	1	1	1

Table 9. Addr 00H control register setting

■ **Analog Input Mode Selector for ADC**

DIE6-1 bit: ADC Input Mode Table

DIEx bit	Input Mode Selector
0	INx Single-ended Input.(default) Single-ended input to the INx pin.
1	INx Differential Input. Differential input to the INxP and INxN pins.

Table 10.Input Mode Selector for ADC

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
13H	Input Selector	0	0	DIE6	DIE5	DIE4	DIE3	DIE2	DIE1
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default Setting		0	0	0	0	0	0	0	0

Table 11. Addr 13H control register setting

◆ For Differential Input Select for Amp. (DIE6-1 = "1"):
Change to following jumper setting:

JP1 (IN1N)	= Short ,	JP3 (IN1/IN1P)	= Diff
JP2 (IN2N)	= Short ,	JP4 (IN2/IN2P)	= Diff
JP5 (IN3N)	= Short ,	JP7 (IN3/IN3P)	= Diff
JP6 (IN4N)	= Short ,	JP8 (IN4/IN4P)	= Diff
JP9 (IN5N)	= Short ,	JP11(IN5/IN5P)	= Diff
JP10 (IN6N)	= Short ,	JP12 (IN6/IN6P)	= Diff

(2) DAC (Digital → Analog)

■ **Toggle switch setting:**

SW2	SW3
H	L→H
AK4118A(U8) : Used	AK4618(U1) : Used

Table 12. Toggle switch setting

■ **Power management of DAC**

Set Addr: 00H = "7F" to release Internal timing reset and power on DAC. Other control register settings are default.

RSTN bit: Internal timing reset
0: Reset.
1: Normal operation (default)

PMDAC bit: Power management of DAC1-6
0: All DAC's power-down. PMDA1-6 bits are invalid.
1: Normal operation (default). PMDA1-6 bits are valid.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	MS	PMMB	PMADC	PMDAC	PMADC56	PMADC34	PMADC12	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Setting		0	1	1	1	1	1	1	1

Table 13. Addr 00H control register setting

PMDA6-1 bit: Power management of DAC 1-6 (0: Power-down, 1: Normal operation)
PMDA1 bit: Power management control of DAC1
PMDA2 bit: Power management control of DAC2
PMDA3 bit: Power management control of DAC3
PMDA4 bit: Power management control of DAC4
PMDA5 bit: Power management control of DAC5
PMDA6 bit: Power management control of DAC6

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 2	0	0	PMDA6	PMDA5	PMDA4	PMDA3	PMDA2	PMDA1
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default Setting		0	0	1	1	1	1	1	1

Table 14. Addr 01H control register setting

*Only the DAC bit being used should be powered on for best results.

Control Software Manual

■ Set-up evaluation board and control software

1. Set up AKD4618-A evaluation board according to above instructions.

2. Connect PC with AKD4618-A evaluation board by USB cable (included in package).
   The board is recognized as HID (Human Interface Device) on the PC.
   When it can not be recognized correctly please reconnect Evaluation board to PC with USB cable.
   [Support OS]
   Windows XP / Vista / 7 (32bit) (XP compatible mode is recommended for Vista / 7)
   64bit OS's are not supported.

3. Insert the CD-ROM labeled "AKD4618-A Evaluation Kit" into the CD-ROM drive.

4. Access the CD-ROM drive, double-click on "akd4618-a.exe" and set up the control program.

5. Evaluate according to the following.

■ Operation flow

1. Set up control program as above and open control program.
   The following operation screen will be shown. (Default setting)

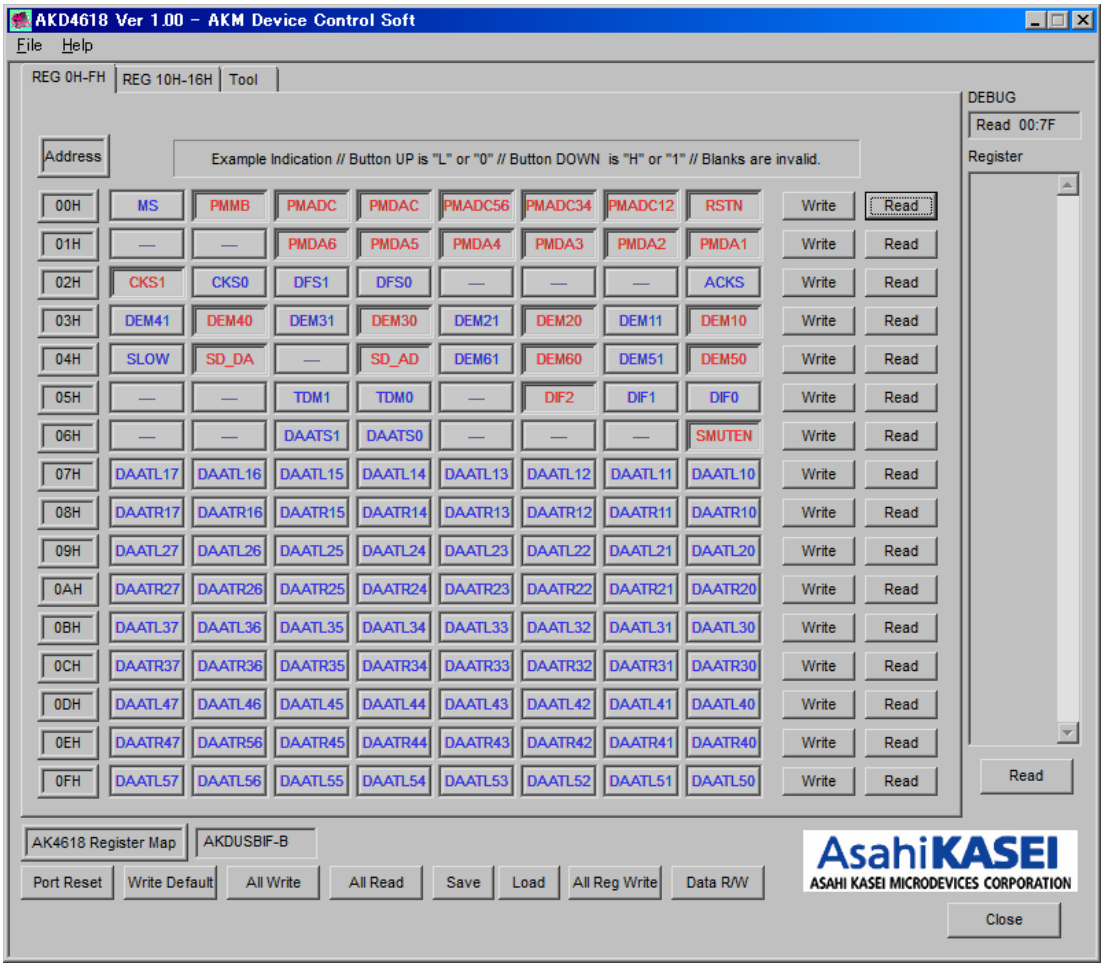

Figure 3. Control software window

2. Click the “Write” button on right side of Addr 00H register.

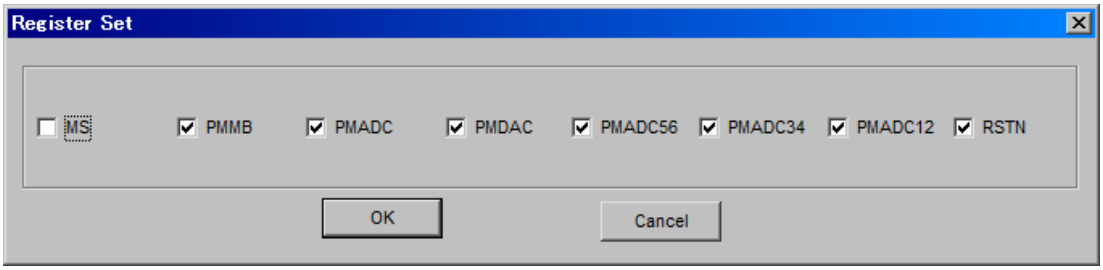

Figure 4. Register set window

3. Input dummy command settings and click “OK” to write dummy command to AK4618.
The following No Ack error message will pop up. Click “OK”.

Figure 5. No ack message window

4. Input registers accordingly into dialog box to evaluate AK4618.

■ Button Functions

1. [Port Reset] : Set up USB interface board (AKDUSBIF-B).
2. [Write Default] : Initialize all register setting.
3. [All Write] : Write all registers currently displayed.
4. [All Read] : Read all register setting.
5. [Save] : Save the current register setting to .akr file.
6. [Load] : Load register setting from saved .akr file.
7. [All Reg Write] : Opens “All Register Write” dialog box. (see Dialog boxes below)
8. [Data R/W] : Opens “Data Read/Write” dialog box . (see Dialog boxes below)
9. [Read] : Read and display current register setting in register window (on right side of main window). Different from [All Read] as it does not reflect to the register map.
10. [Close] : Close Control Software window.

■ Dialog boxes

1. [All Register Write]: Dialog box to write register setting files

Clicking the [All Reg Write] button in the main window opens the dialog box below.
Multiple register setting files created by the [SAVE] button can be set and applied.

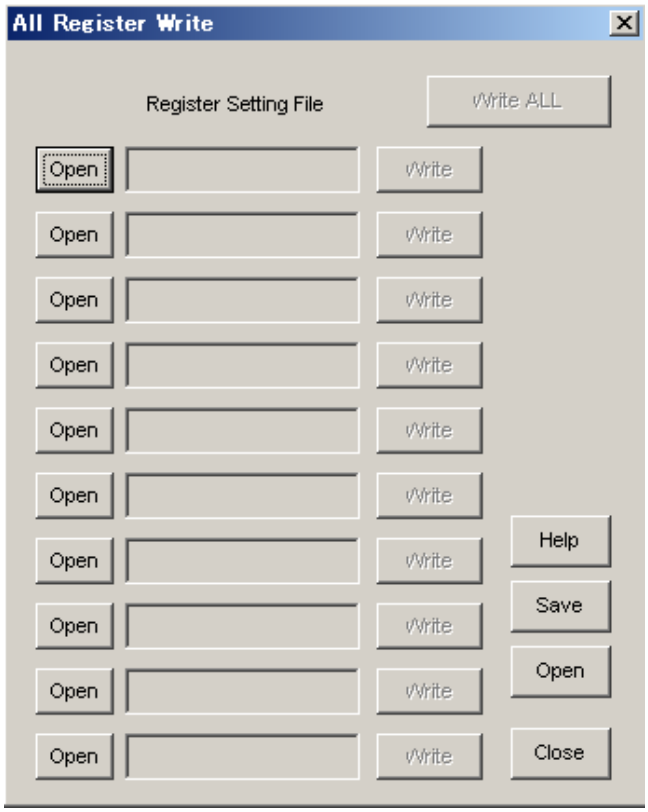

Figure 6. Window of [All Reg Write]

<Operation flow>
(1) Click [Open(left) Button.
(2) Select file (*.akr) and Click [Open] Button. Up to 10 files can be selected.
(3) Click [Write] to write each file. [Write ALL] writes all files selected.

Button Functions:
1. [Open (left)] : Select register setting file (*.akr).
2. [Write] : Write register setting file in textbox.
3. [Write ALL] : Write all register setting files selected. Write is executed in descending order.
4. [Help] : “Help” window pops up.
5. [Save] : Save the current register map setting (*.mar).
6. [Open (right)] : Load register map setting file (*.mar).
7. [Close] : Close dialog box.

2. [Data Read/Write]: Dialog box to manually enter register setting

Click the [Data R/W] button in the main window to open the data read/write dialog box.
Data manually entered into Data box is written to the specified address.

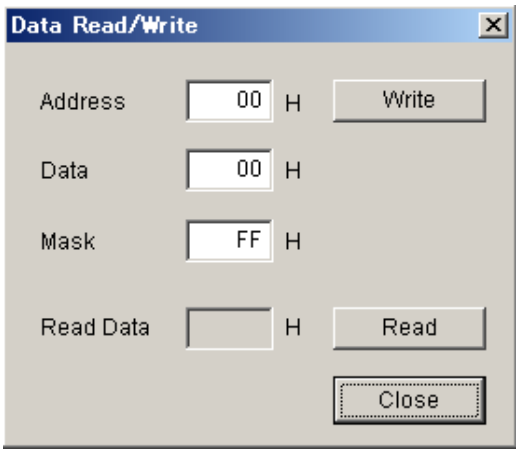

Figure 7. Window of [Data R/W]

Textbox Functions:
[Address] : Input register address in 2 hexadecimal digits.
[Data] : Input register data in 2 hexadecimal digits.
[Mask] : Input mask data in 2 hexadecimal digits. This value is AND-ed with input data.

Button Functions:
[Write] : Writes data generated from [Data] and [Mask] to register specified in [Address]
[Read] : Displays register data specified in [Address] in [Read Data] box in hexadedimal.
[Close] : Closes dialog box. To cancel a process close the dialog box without writing

※ Register map updated after [Write] and [Read] operation.

Tab Functions

1. [REG]: Register Map

Register data is indicated on the register map. Each bit on the register map is a push-button switch. Button DOWN and red lettering indicates “1” and button UP with blue lettering indicates “0”. Buttons with “---“are undefined in the datasheet.

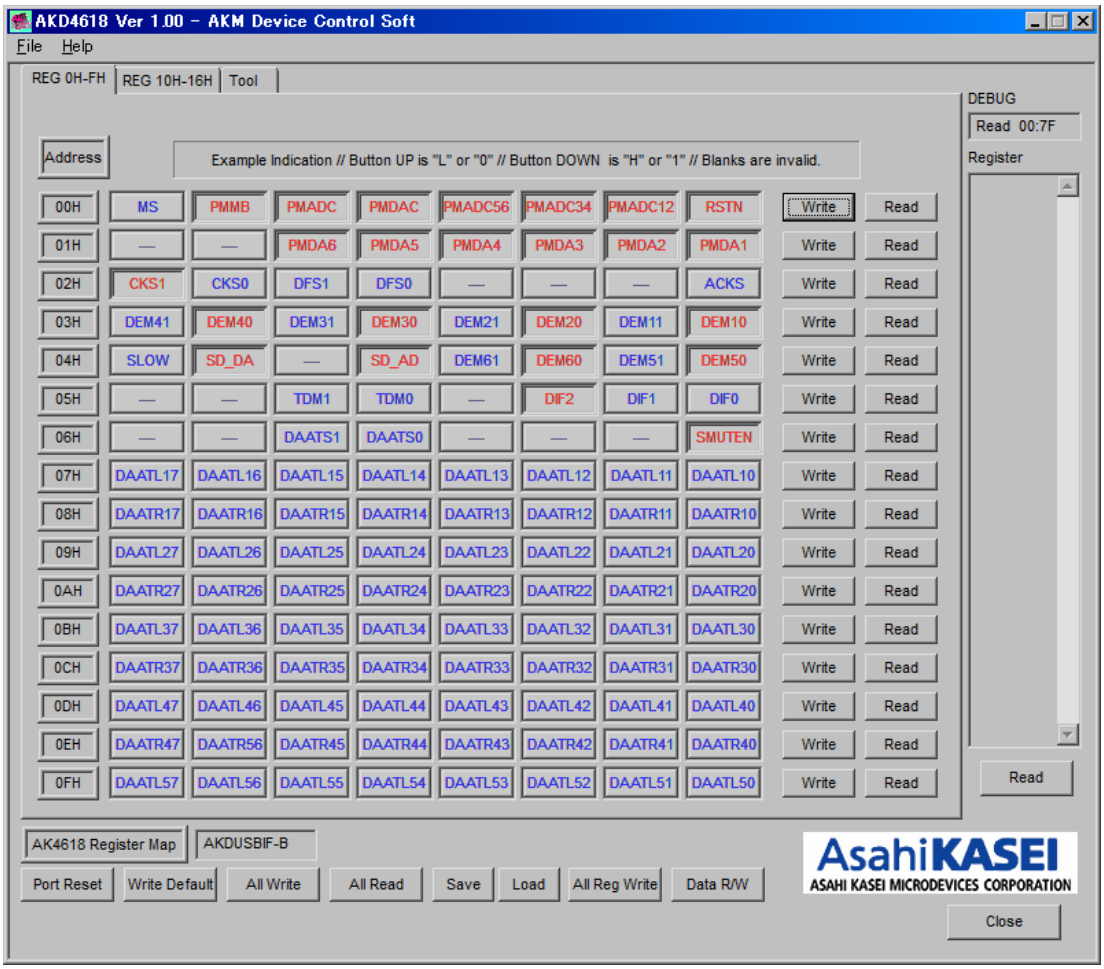

Figure 8. [REG] window (REG 0H-FH)

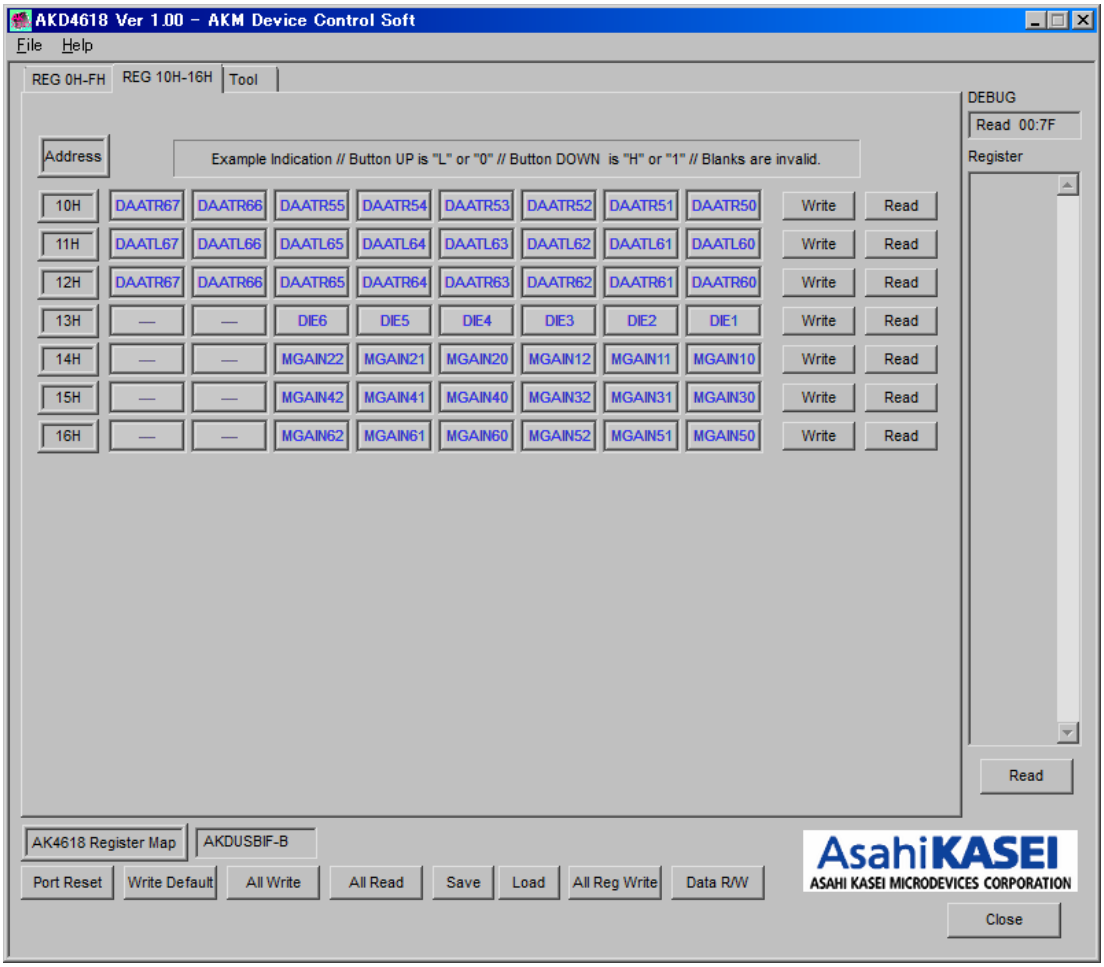

Figure 9. [REG] window (REG 10H-1FH)

2. [Tool]: Testing Tools

This tab screen is for the evaluation testing tool.
Click button for each testing tool.

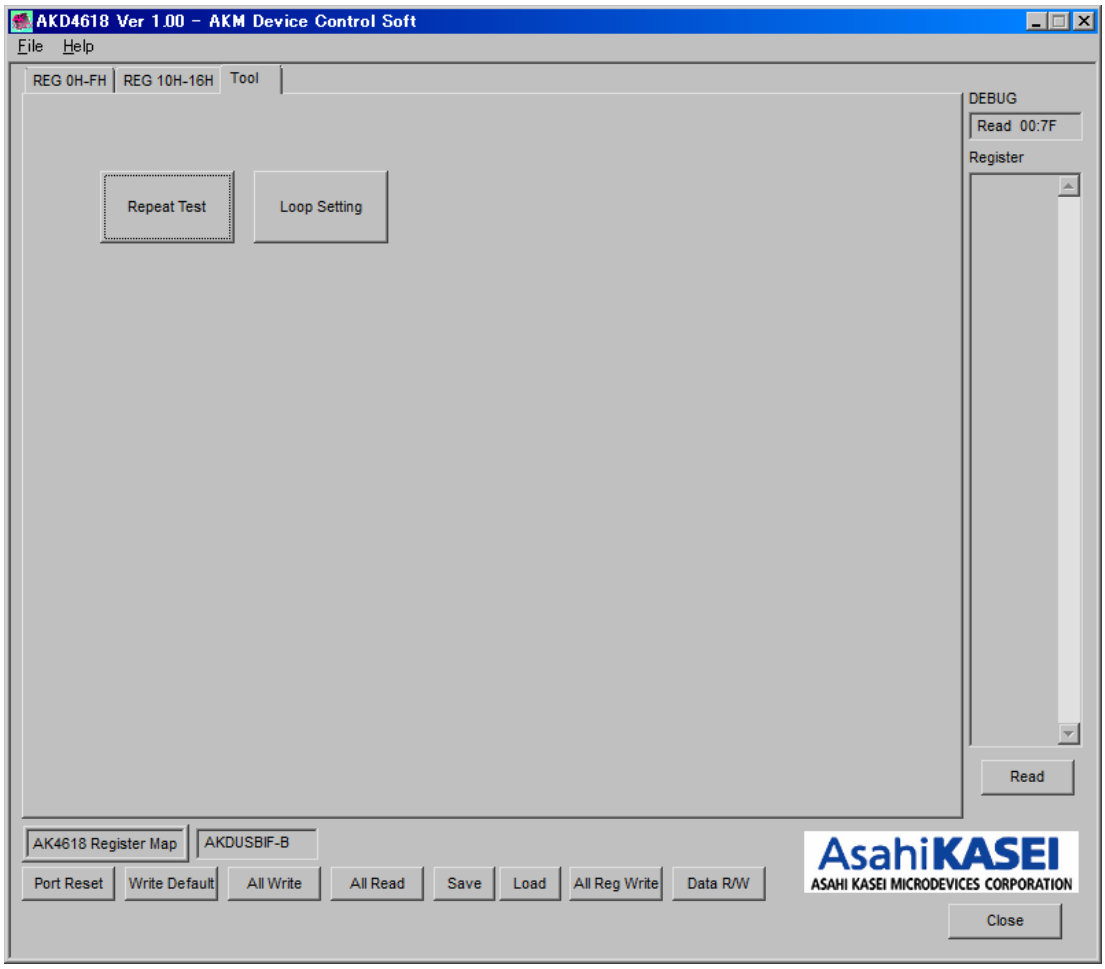

Figure 10. [Tool] window

Measurement Results

[Measurement condition]

- Measurement unit : Audio Precision, SYS-2722 (No.00069)
- MCKI : 256fs (12.288MHz)
- BICK : 64fs
- fs : 48kHz
- Bit : 24bit
- Measurement Mode : ADC @ Slave Mode / DAC @ Slave Mode
- Power Supply : +12V=12V, GND
  AVDD1=AVDD2=3.3V (Regulator), TVDD=3.3V (Regulator)
- Input Frequency : 1kHz
- Measurement Frequency : 20 ~ 20kHz @48kHz
- Temperature : Room

[Measurement Results]

1. ADC（Single-ended Inputs）

		Result		Unit
		Lch	Rch	
Stereo ADC : AIN1L/R => ADC => SDTO1				
S/(N+D)	fs = 48kHz (-1dBFS)	89.0	89.0	dB
DR	fs = 48kHz (-60dBFS, A-Weighted)	98.1	98.0	dB
S/N	fs = 48kHz (A-weighted)	98.2	98.0	dB
Stereo ADC : AIN2L/R => ADC => SDTO2				
S/(N+D)	fs = 48kHz (-1dBFS)	89.3	89.1	dB
DR	fs = 48kHz (-60dBFS, A-Weighted)	98.0	98.0	dB
S/N	fs = 48kHz (A-weighted)	98.1	98.1	dB
Stereo ADC : AIN3L/R => ADC => SDTO3				
S/(N+D)	fs = 48kHz (-1dBFS)	88.9	88.9	dB
DR	fs = 48kHz (-60dBFS, A-Weighted)	98.0	98.0	dB
S/N	fs = 48kHz (A-weighted)	98.1	98.1	dB

2. ADC（Differential Inputs）

		Result		Unit
		Lch	Rch	
Stereo ADC : AIN1L/R => ADC => SDTO1				
S/(N+D)	fs = 48kHz (-1dBFS)	89.1	89.0	dB
DR	fs = 48kHz (-60dBFS, A-Weighted)	97.7	98.6	dB
S/N	fs = 48kHz (A-weighted)	97.7	98.6	dB
Stereo ADC : AIN2L/R => ADC => SDTO2				
S/(N+D)	fs = 48kHz (-1dBFS)	89.4	89.1	dB
DR	fs = 48kHz (-60dBFS, A-Weighted)	98.8	98.6	dB
S/N	fs = 48kHz (A-weighted)	99.1	98.7	dB
Stereo ADC : AIN3L/R => ADC => SDTO3				
S/(N+D)	fs = 48kHz (-1dBFS)	89.1	88.8	dB
DR	fs = 48kHz (-60dBFS, A-Weighted)	98.7	98.1	dB
S/N	fs = 48kHz (A-weighted)	99.1	98.8	dB

3. DAC

		Result		Unit
		Lch	Rch	
DAC1 : SDTI1 => DAC1 => L/ROUT1				
S/(N+D)	fs = 48kHz (0dBFS)	97.5	99.0	dB
DR	fs = 48kHz (-60dBFS, A-Weighted, 20kHz SPCL)	106.9	106.9	dB
S/N	fs = 48kHz (A-weighted, 20kHz SPCL)	107.0	107.0	dB
DAC2 : SDTI2 => DAC2 => L/ROUT2				
S/(N+D)	fs = 48kHz (0dBFS)	98.2	97.5	dB
DR	fs = 48kHz (-60dBFS, A-Weighted, 20kHz SPCL)	106.9	106.9	dB
S/N	fs = 48kHz (A-weighted, 20kHz SPCL)	107.0	107.0	dB
DAC3 : SDTI3 => DAC3 => L/ROUT3				
S/(N+D)	fs = 48kHz (0dBFS)	98.2	97.5	dB
DR	fs = 48kHz (-60dBFS, A-Weighted, 20kHz SPCL)	106.9	106.9	dB
S/N	fs = 48kHz (A-weighted, 20kHz SPCL)	107.0	107.0	dB
DAC4 : SDTI4 => DAC4 => L/ROUT4				
S/(N+D)	fs = 48kHz (0dBFS)	98.8	98.4	dB
DR	fs = 48kHz (-60dBFS, A-Weighted, 20kHz SPCL)	106.9	106.9	dB
S/N	fs = 48kHz (A-weighted, 20kHz SPCL)	107.0	107.0	dB
DAC5 : SDTI5 => DAC5 => L/ROUT5				
S/(N+D)	fs = 48kHz (0dBFS)	97.5	97.6	dB
DR	fs = 48kHz (-60dBFS, A-Weighted, 20kHz SPCL)	106.9	106.9	dB
S/N	fs = 48kHz (A-weighted, 20kHz SPCL)	107.0	107.0	dB
DAC6 : SDTI6 => DAC6 => L/ROUT6				
S/(N+D)	fs = 48kHz (0dBFS)	98.3	98.6	dB
DR	fs = 48kHz (-60dBFS, A-Weighted, 20kHz SPCL)	106.9	106.9	dB
S/N	fs = 48kHz (A-weighted, 20kHz SPCL)	107.0	107.0	dB

[Plot Data]

1. ADC (Single-ended Inputs)
   ADC (fs = 48kHz); IN1/IN2(Single-ended) => ADC => SDTO

AK4618 FFT Stereo ADC (IN1/IN2:L/R)
[fs=48kHz, fin=1kHz, -1dBFS]

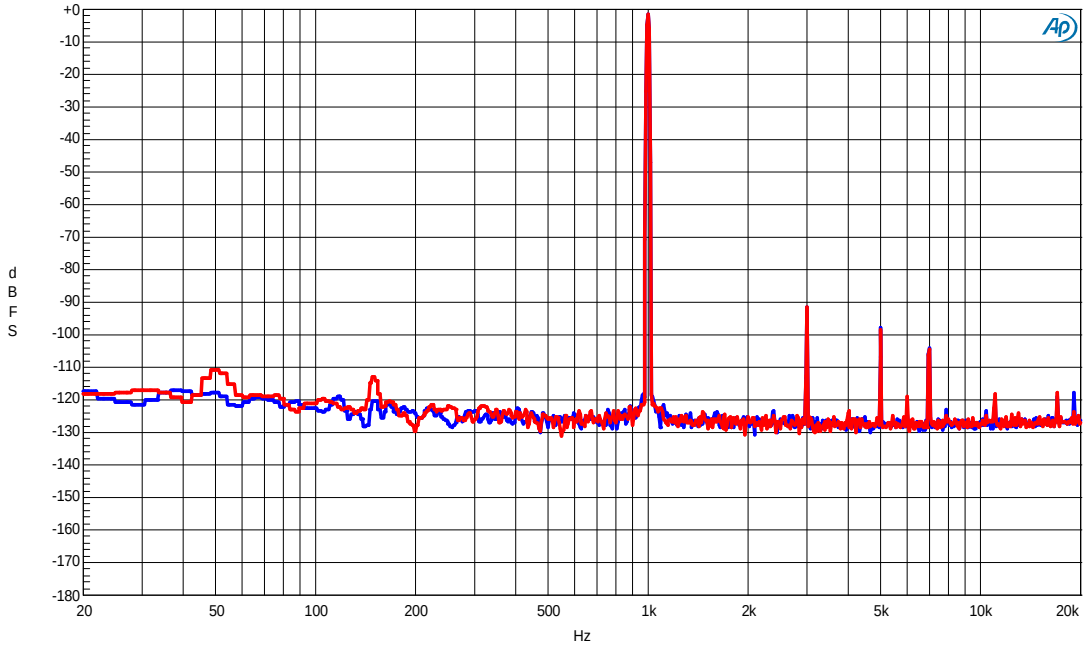

Figure 11. ADC (Single-ended) – FFT (-1dBFS) [fs = 48kHz]

AK4618 FFT Stereo ADC (IN1/IN2:L/R)
[fs=48kHz, fin=1kHz, -60dBFS]

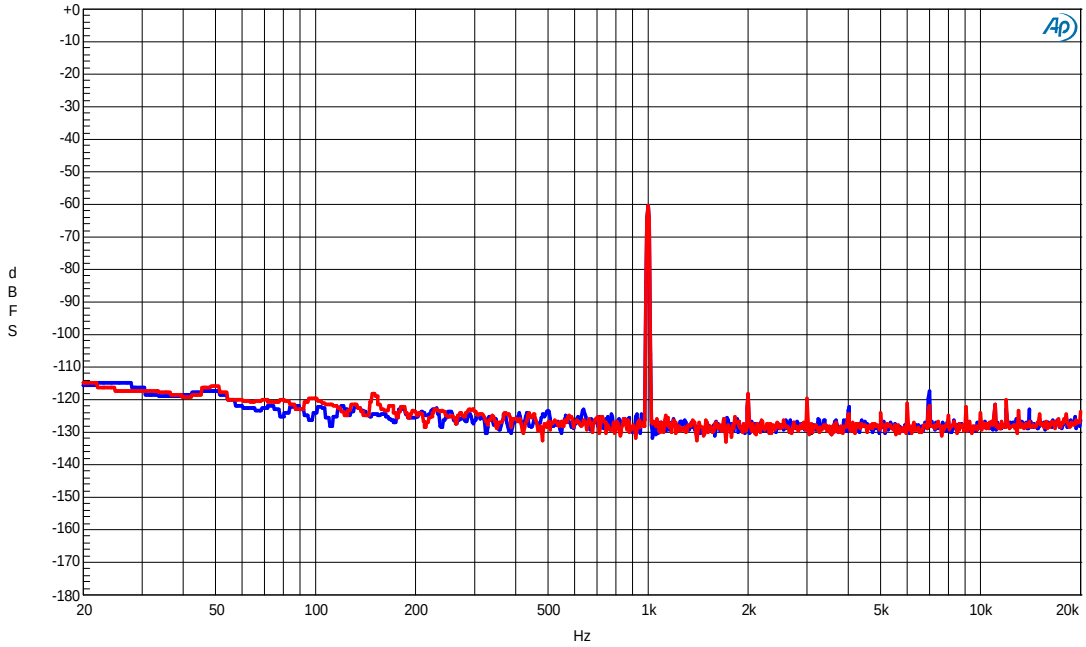

Figure 12. ADC (Single-ended) – FFT (-60dBFS) [fs = 48kHz]

AK4618 FFT Stereo ADC (IN1/IN2:L/R)
[fs=48kHz, fin=1kHz, no signal]

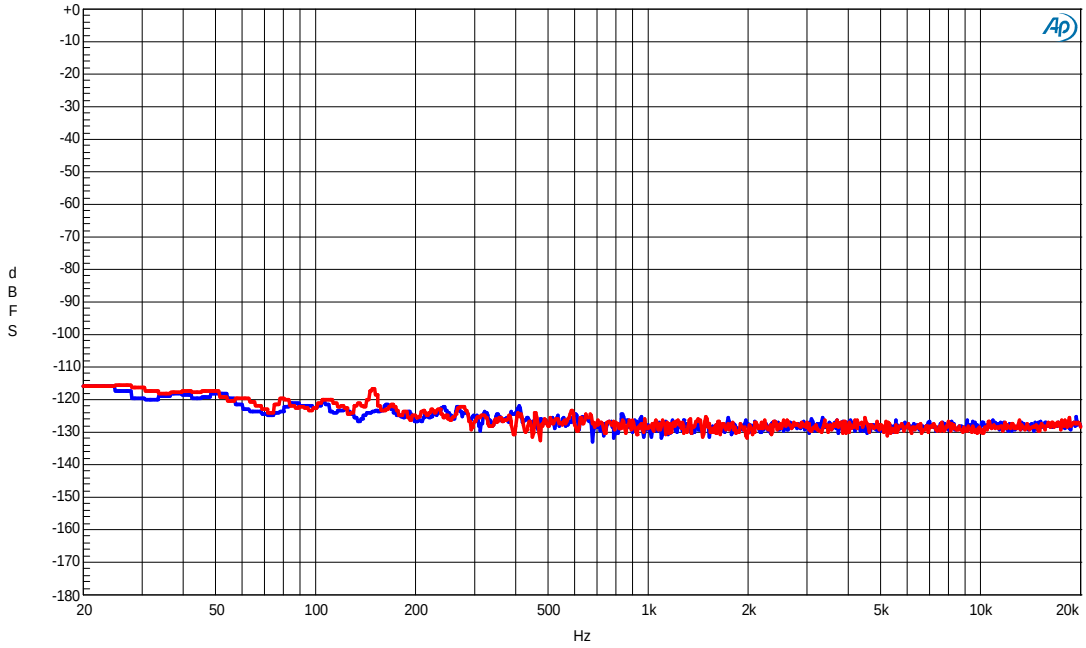

Figure 11. ADC (Single-ended) – FFT (No Signal) [fs = 48kHz]

AK4618 THD+N vs Amplitude Stereo ADC (IN1/IN2:L/R)
[fs=48kHz, fin=1kHz]

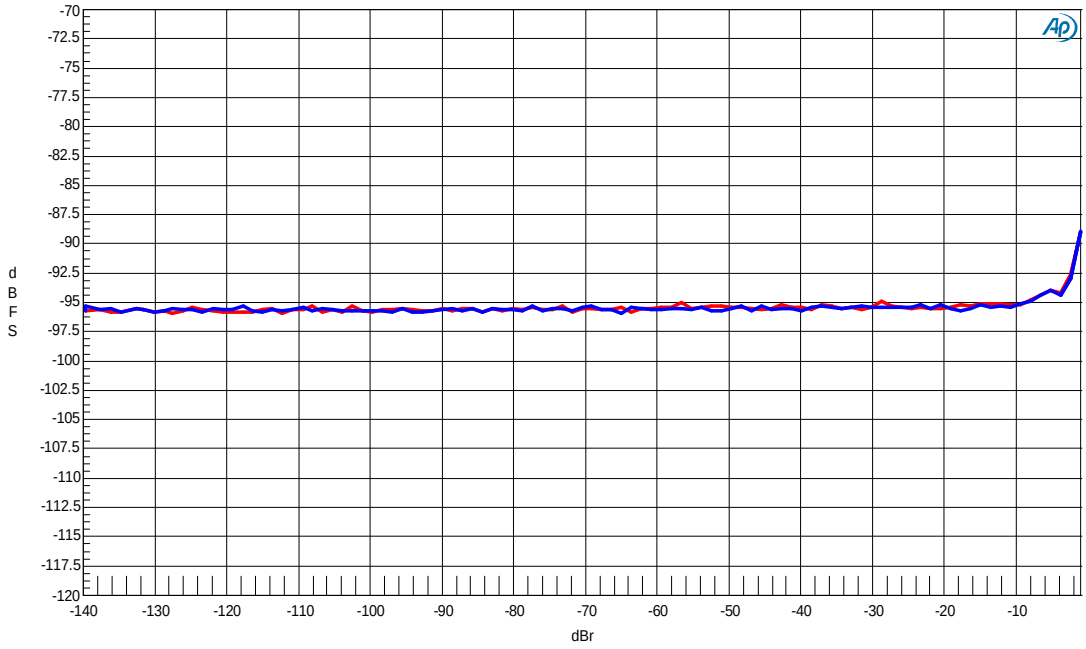

Figure 12. ADC (Single-ended) – THD+N vs. Amplitude (Input Level) [fs = 48kHz]

AK4618 THD+N vs Input Frequency Stereo ADC (IN1/IN2:L/R)
[fs=48kHz, -1dBFS]

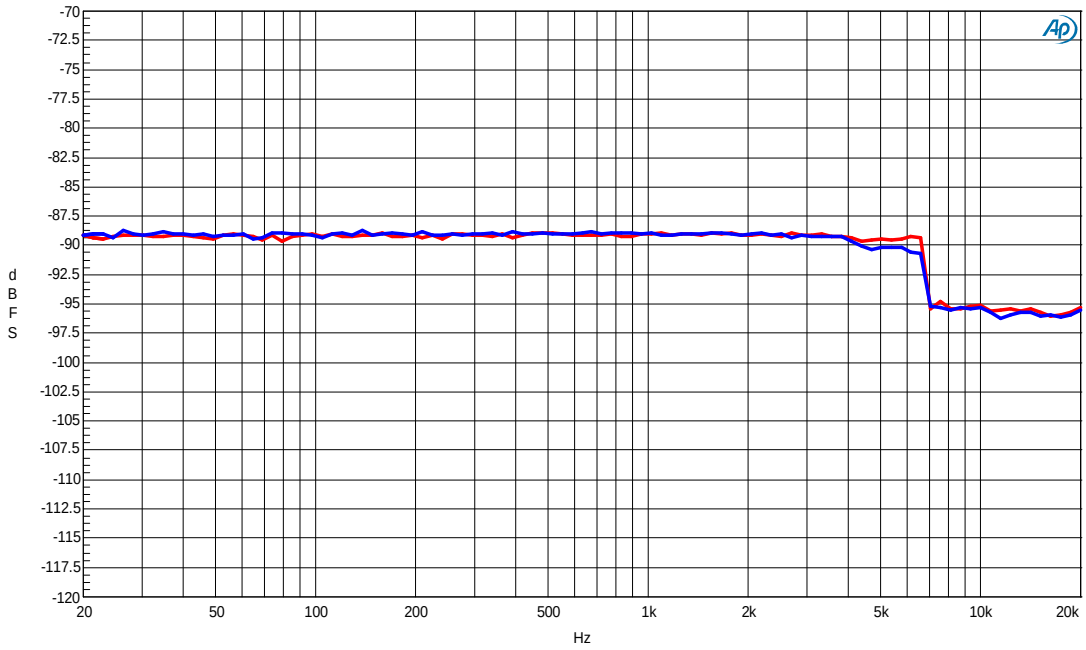

Figure 13. ADC (Single-ended) – THD+N vs. Input Frequency [fs = 48kHz]

AK4618 Linearity Stereo ADC (IN1/IN2:L/R)
[fs=48kHz, fin=1kHz]

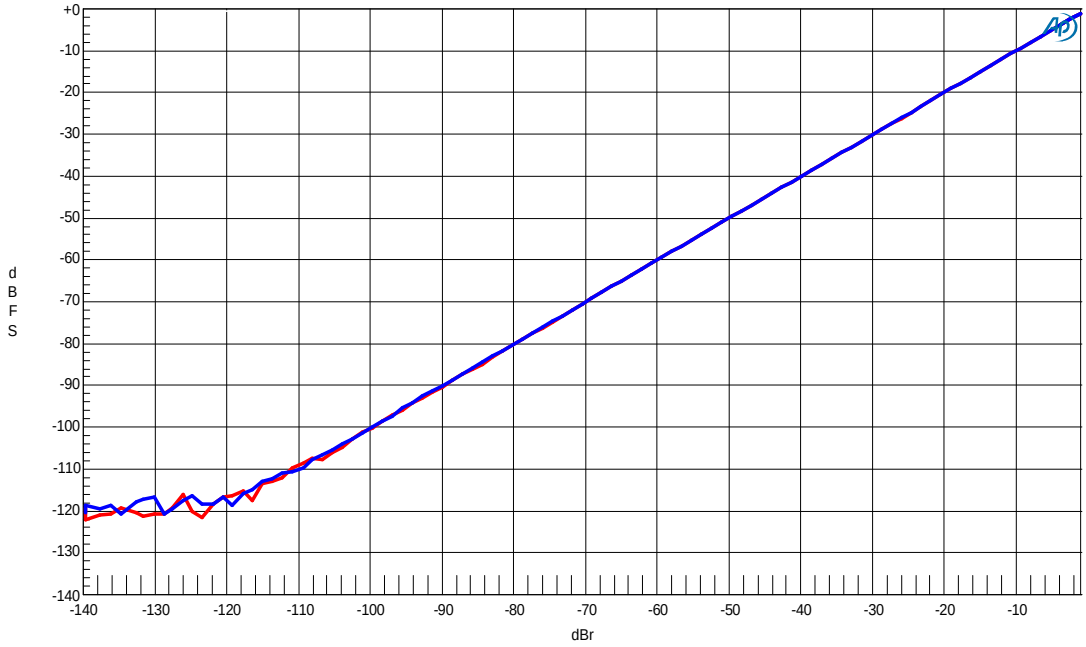

Figure 14. ADC (Single-ended) – Linearity [fs = 48kHz]

AK4618 Frequency Response Stereo ADC (IN1/IN2:L/R)
[fs=48kHz, -1dBFS]

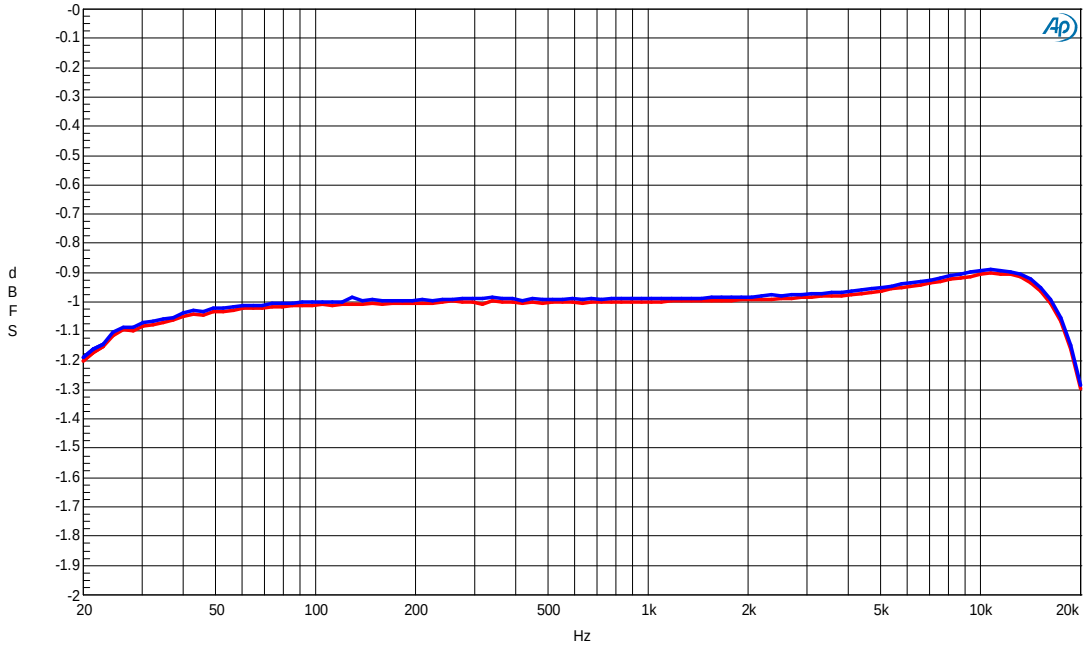

Figure 15. ADC (Single-ended) – Frequency Response [fs = 48kHz]

AK4618 Crosstalk Stereo ADC (IN1/IN2:L/R)
[fs=48kHz, -1dBFS]

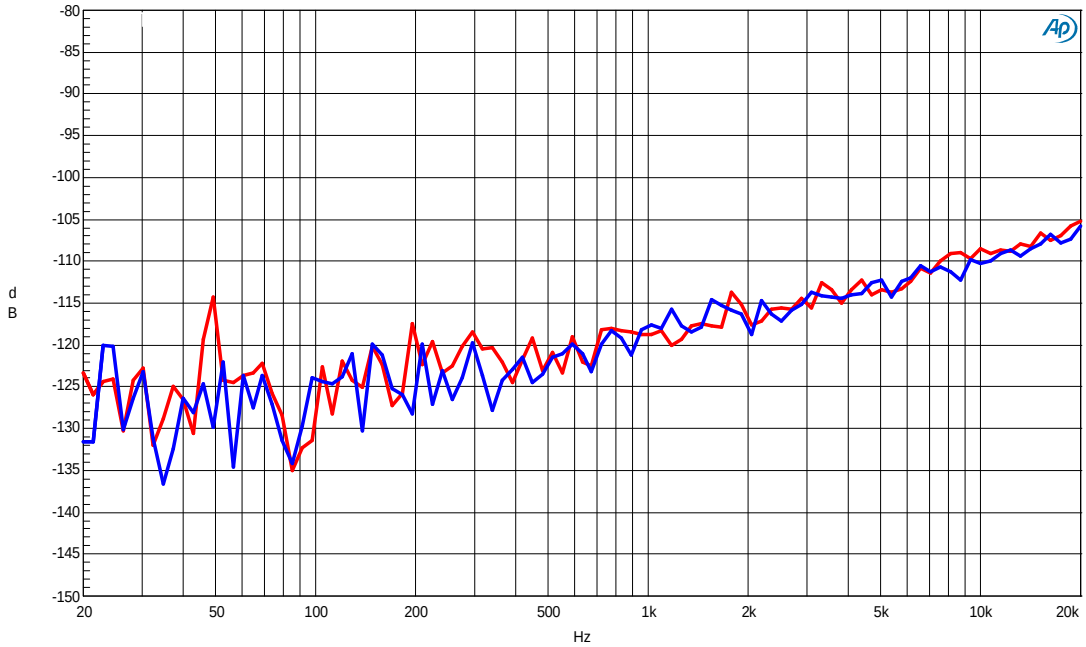

Figure 16. ADC (Single-ended) – Crosstalk [fs = 48kHz]

2. ADC (Differential Inputs)
ADC (fs = 48kHz); IN1P/IN2P,IN1N/IN2N(Differential) => ADC => SDTO

AK4618 FFT Stereo ADC (IN1/IN2:L/R)
[fs=48kHz, fin=1kHz, -1dBFS]

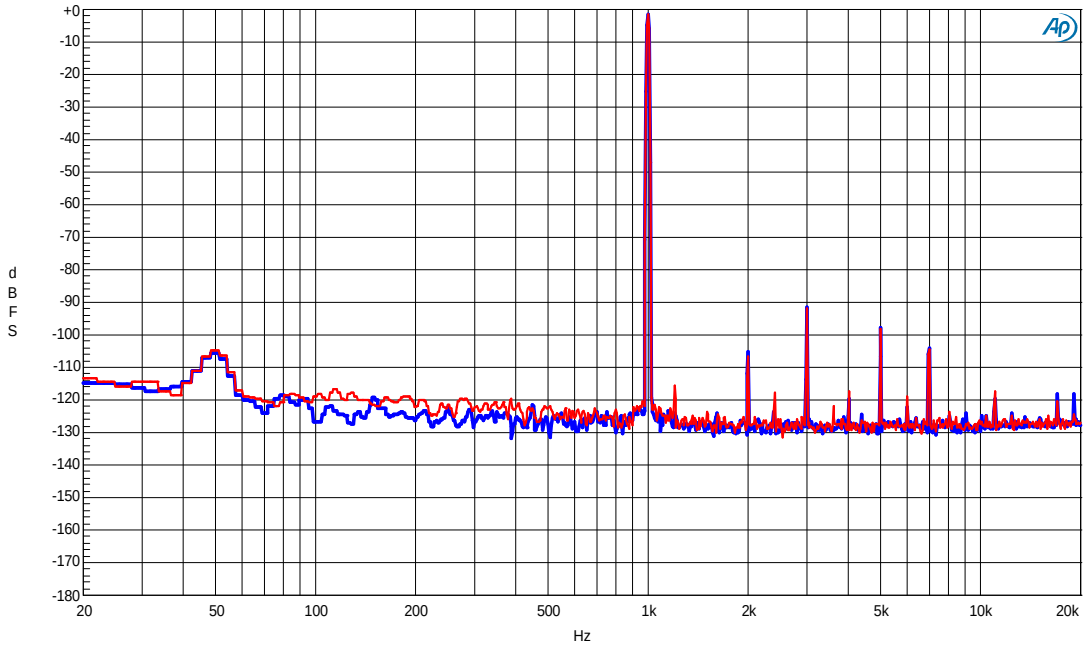

Figure Figure 17. ADC (Differential) – FFT (-1dBFS) [fs = 48kHz]

AK4618 FFT Stereo ADC (IN1/IN2:L/R)
[fs=48kHz, fin=1kHz, -60dBFS]

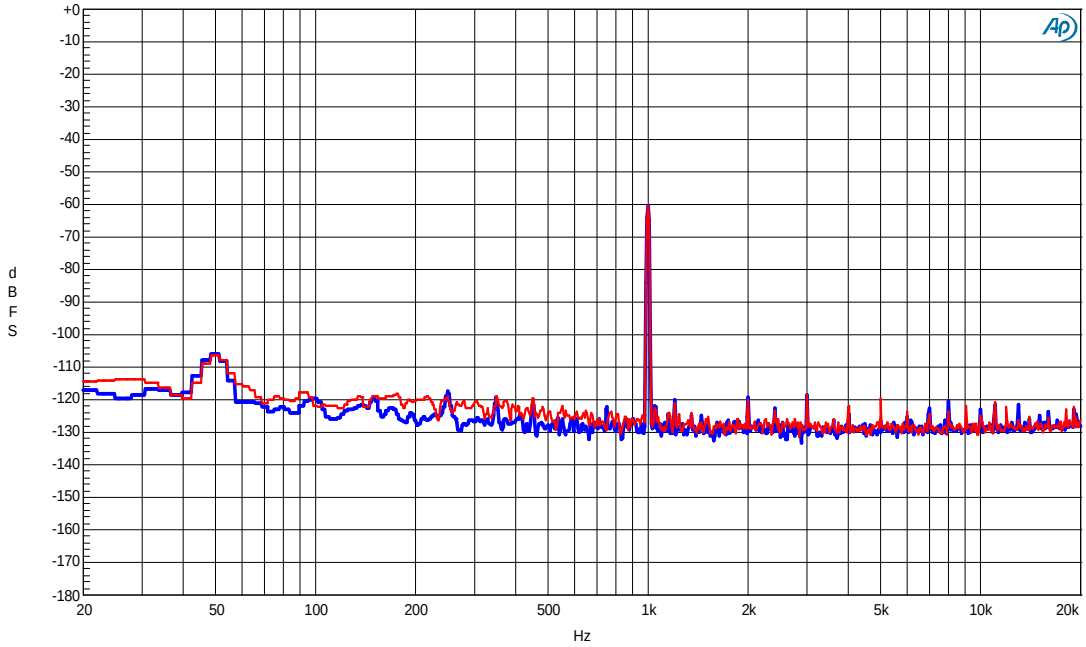

Figure 18. ADC (Differential) – FFT (-60dBFS) [fs = 48kHz]

AK4618 FFT Stereo ADC (IN1/IN2:L/R)
[fs=48kHz, fin=1kHz, no signal]

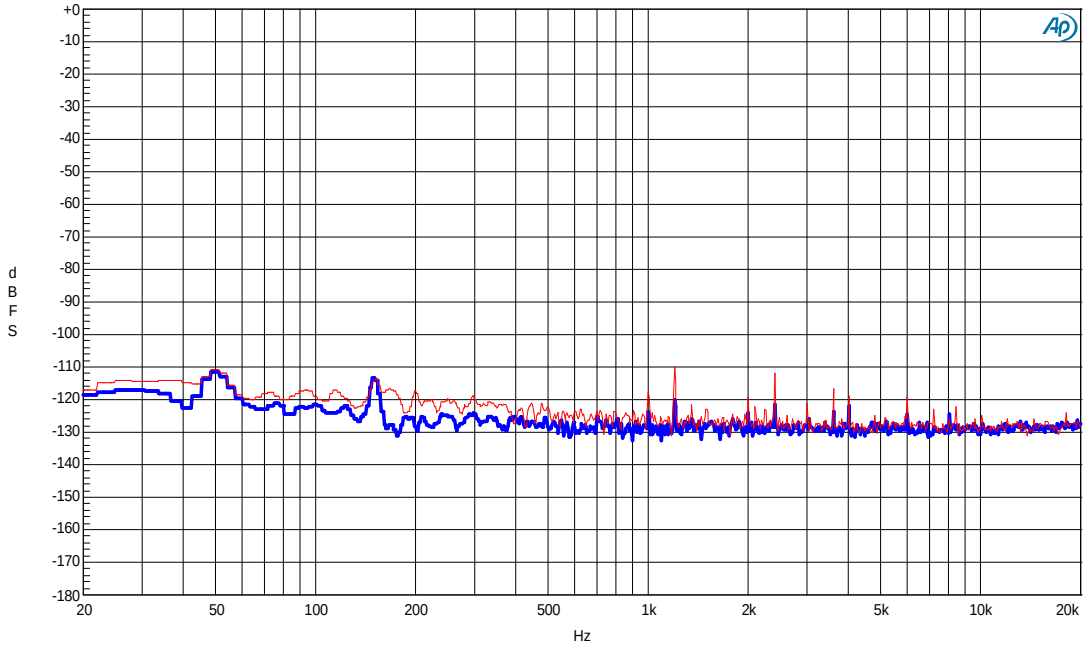

Figure 19. ADC (Differential) – FFT (No Signal) [fs = 48kHz]

AK4618 THD+N vs Amplitude Stereo ADC (IN1/IN2:L/R)
[fs=48kHz, fin=1kHz]

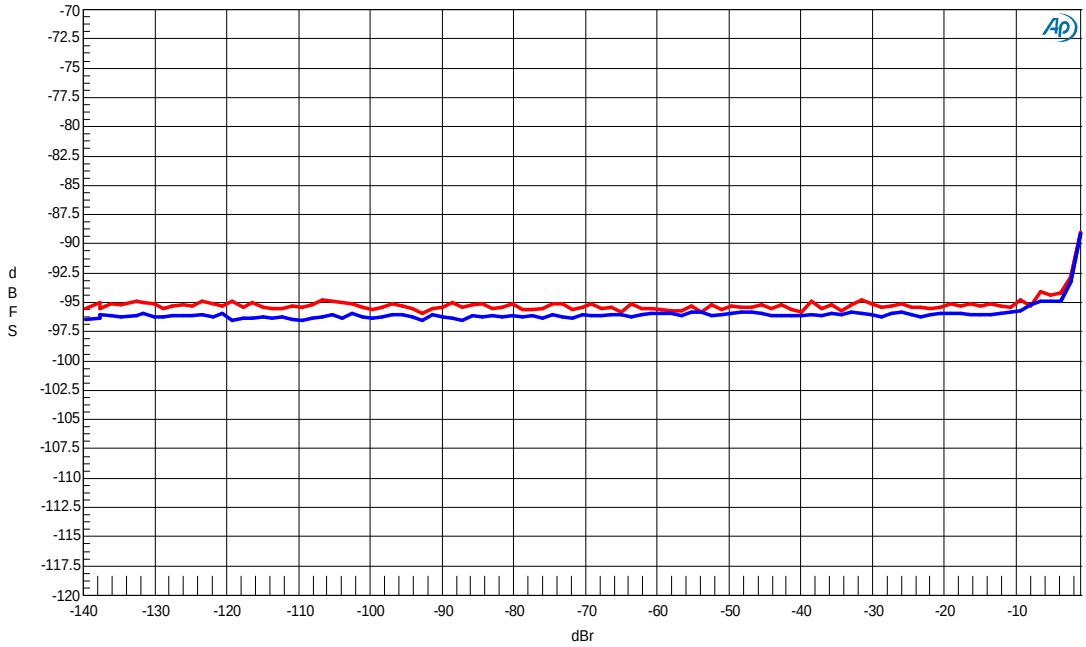

Figure 20. ADC (Differential) – THD+N vs. Amplitude (Input Level) [fs = 48kHz]

AK4618 THD+N vs Input Frequency Stereo ADC (IN1/IN2:L/R)
[fs=48kHz, -1dBFS]

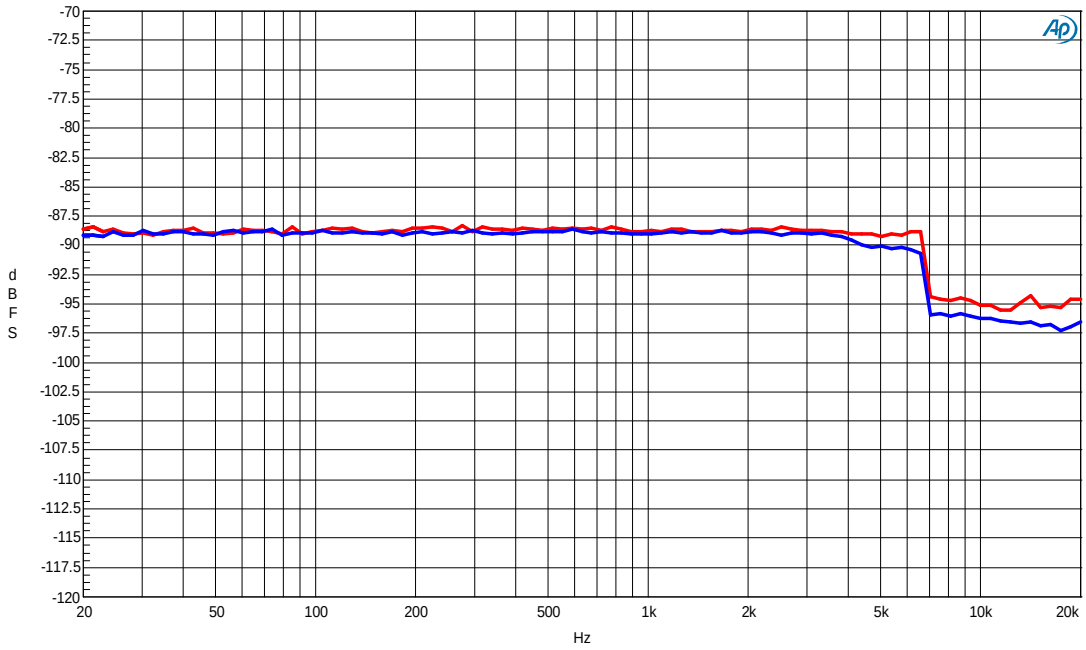

Figure 21. ADC (Differential) – THD+N vs. Input Frequency [fs = 48kHz]

AK4618 Linearity Stereo ADC (IN1/IN2:L/R)
[fs=48kHz, fin=1kHz]

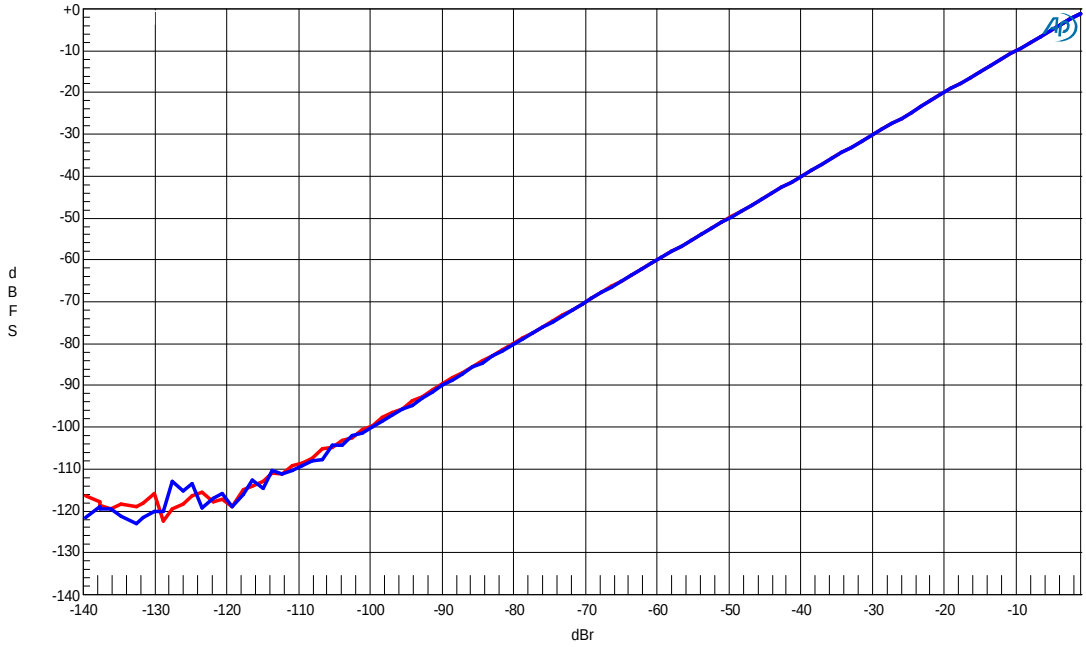

Figure 22. ADC (Differential) – Linearity [fs = 48kHz]

AK4618 Frequency Response Stereo ADC (IN1/IN2:L/R)
[fs=48kHz, -1dBFS]

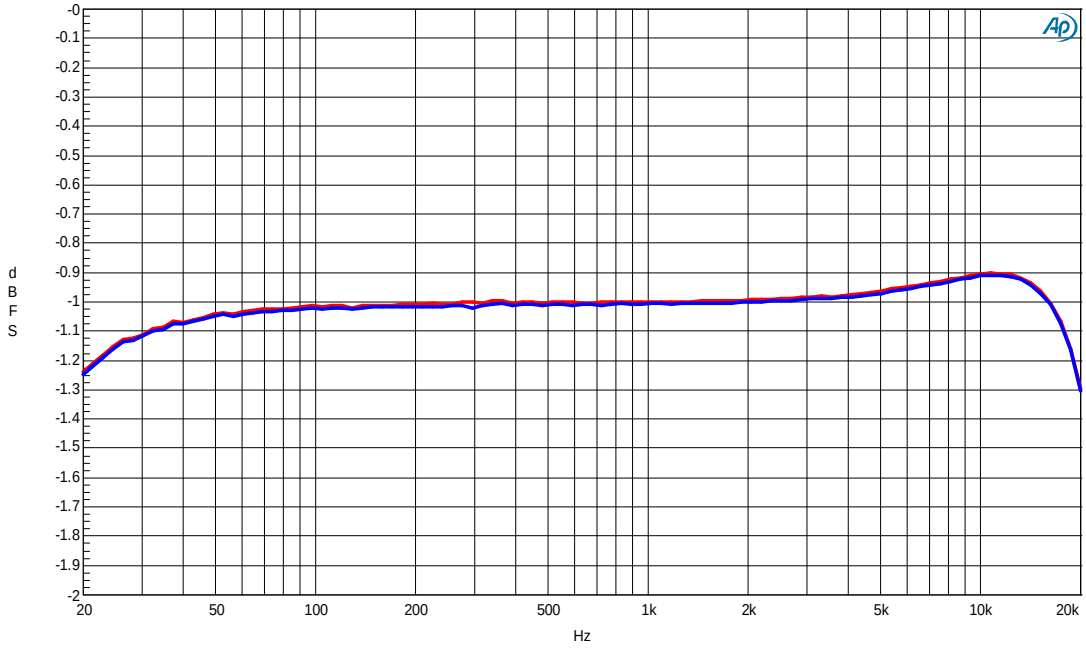

Figure 23. ADC (Differential) – Frequency Response [fs = 48kHz]

AK4618 Crosstalk Stereo ADC (IN1/IN2:L/R)
[fs=48kHz, -1dBFS]

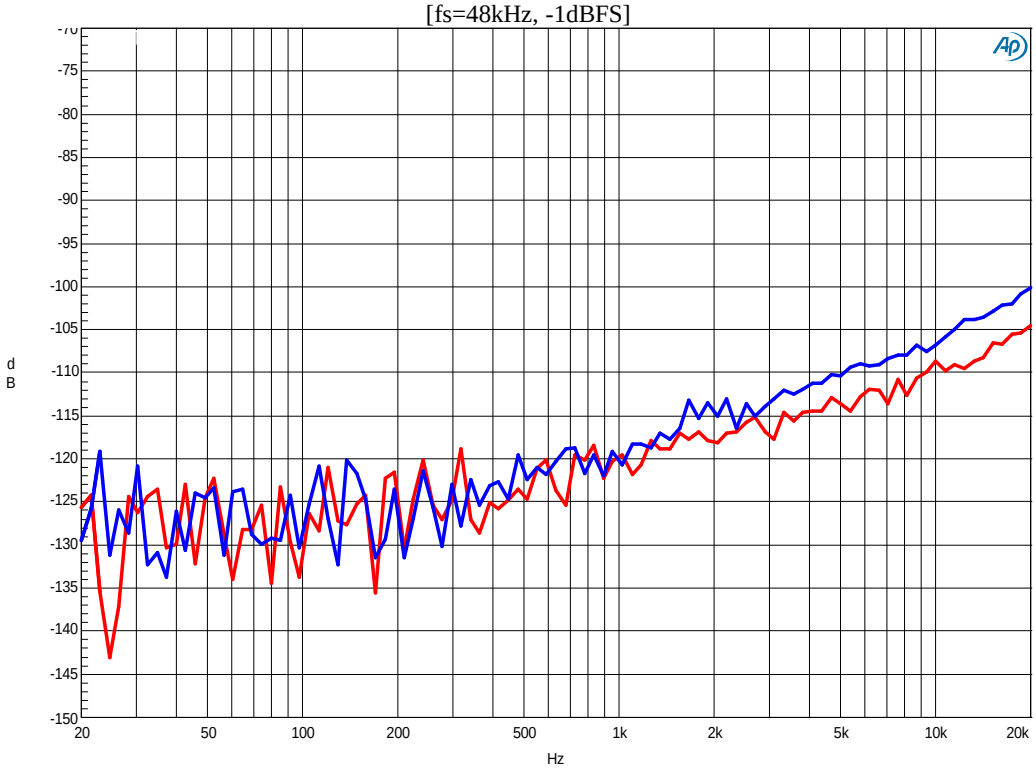

Figure 24. ADC (Differential) – Crosstalk [fs = 48kHz]

3. DAC (SDTI1 => L/ROUT1)
DAC1 (fs = 48kHz); SDTI1 => DAC1 => L/ROUT1

AK4618 FFT Single-end DAC (L/ROUT1)
[fs=48kHz, fin=1kHz, 0dBFS]

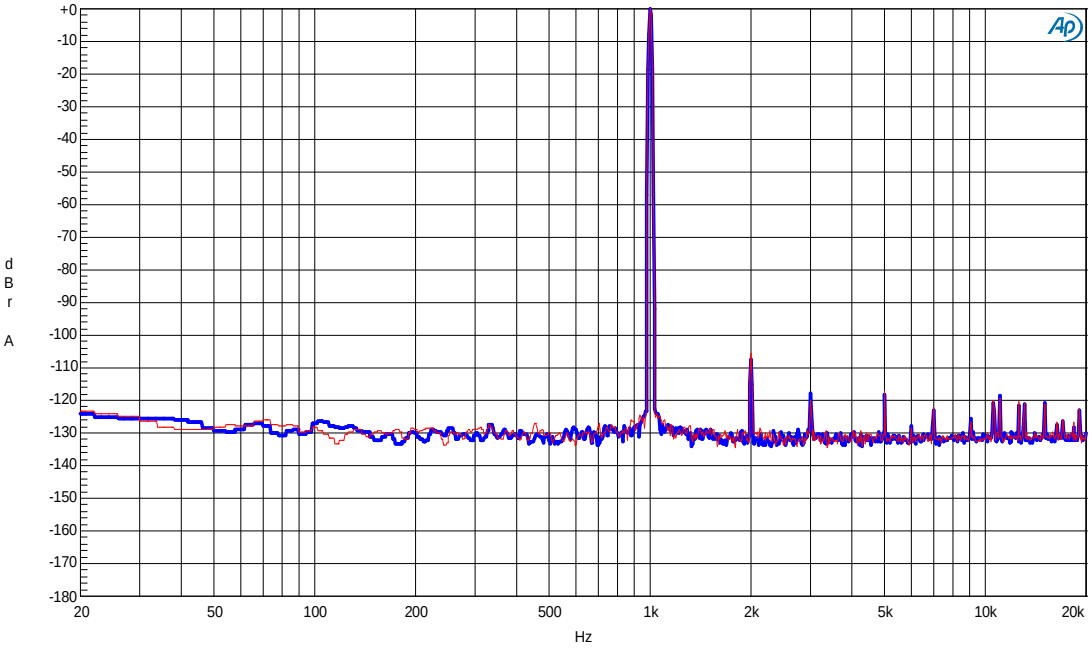

Figure 25. DAC1 – FFT (0BFS) [fs = 48kHz]

AK4618 FFT Single-end DAC (L/ROUT1)
[fs=48kHz, fin=1kHz, -60dBFS]

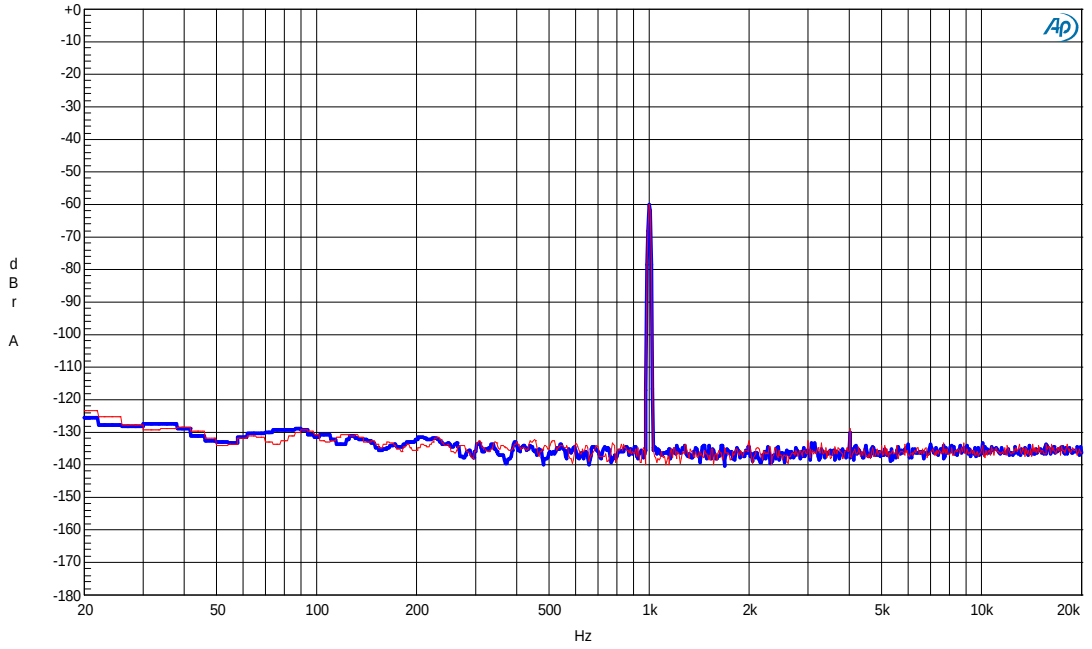

Figure 26. DAC1 – FFT (-60dBFS) [fs = 48kHz]

AK4618 FFT Single-end DAC (L/ROUT1)
[fs=48kHz, fin=1kHz, no signal]

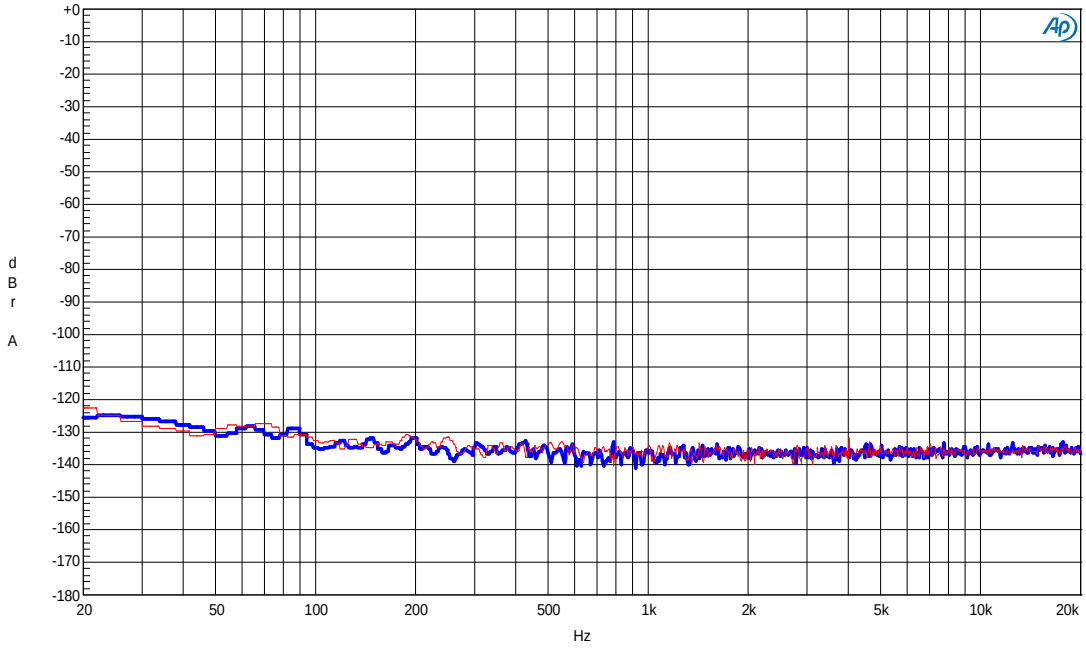

Figure 27. DAC1 – FFT (No Signal) [fs = 48kHz]

AK4618 THD+N vs Amplitude Single-end DAC (L/ROUT1)
[fs=48kHz, fin=1kHz] 20kHz SPCL

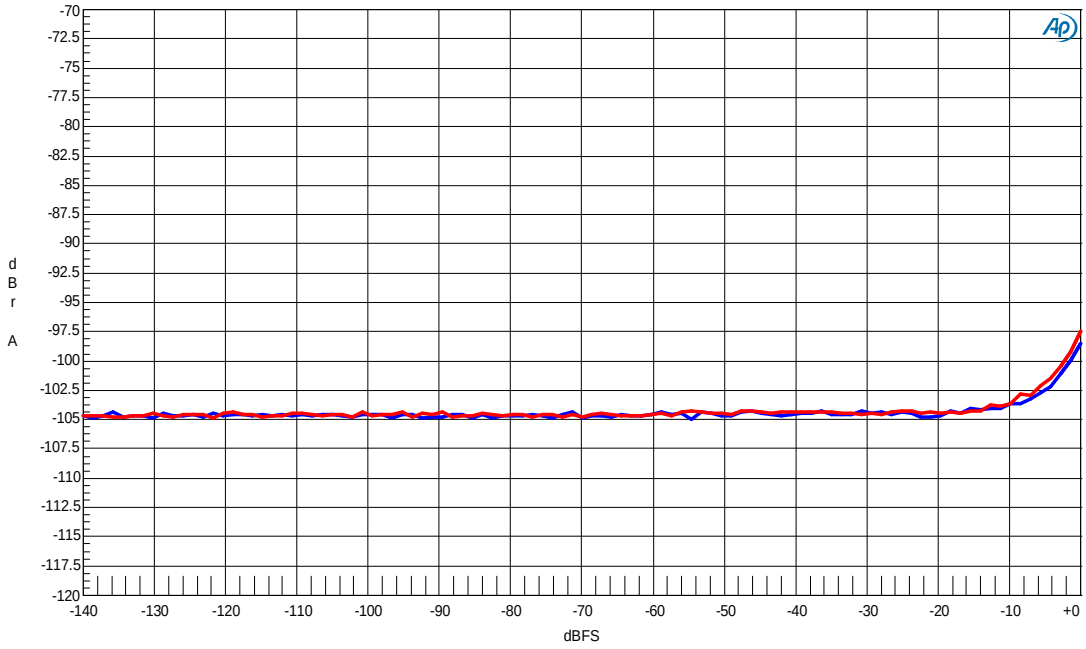

Figure 28.DAC1 – THD+N vs. Amplitude (Input Level) [fs = 48kHz]

AK4618 THD+N vs Input Frequency Single-end DAC (L/ROUT1)
[fs=48kHz, 0dBFS] 20kHz SPCL

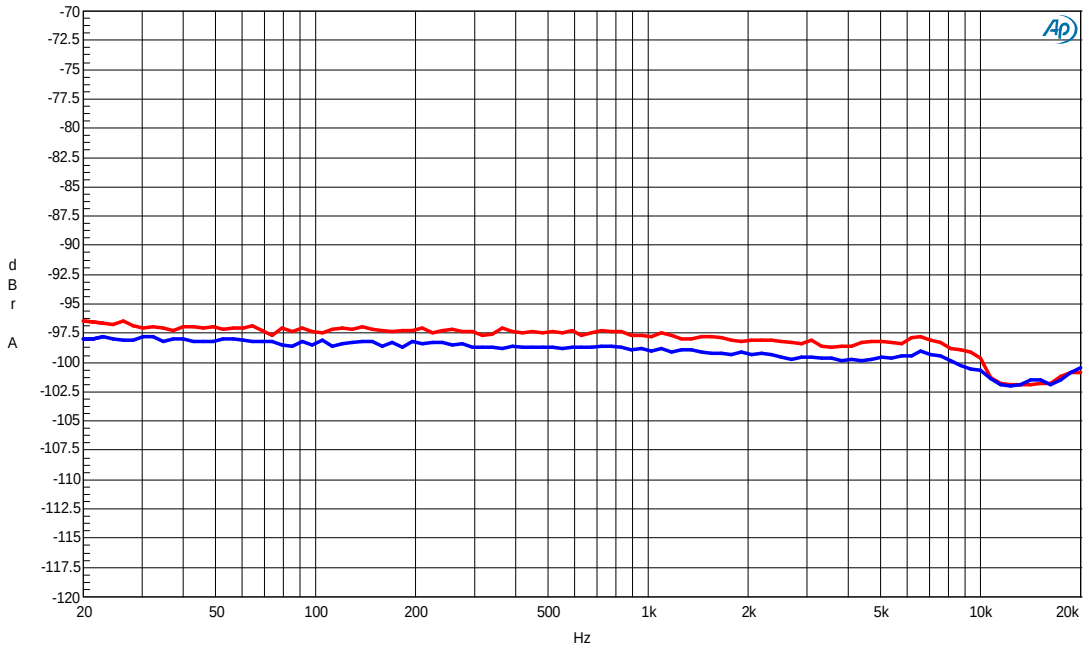

Figure 29. DAC1 – THD+N vs. Input Frequency [fs = 48kHz]

AK4618 Linearity Single-end DAC (L/ROUT1)
[fs=48kHz,fin=1kHz]

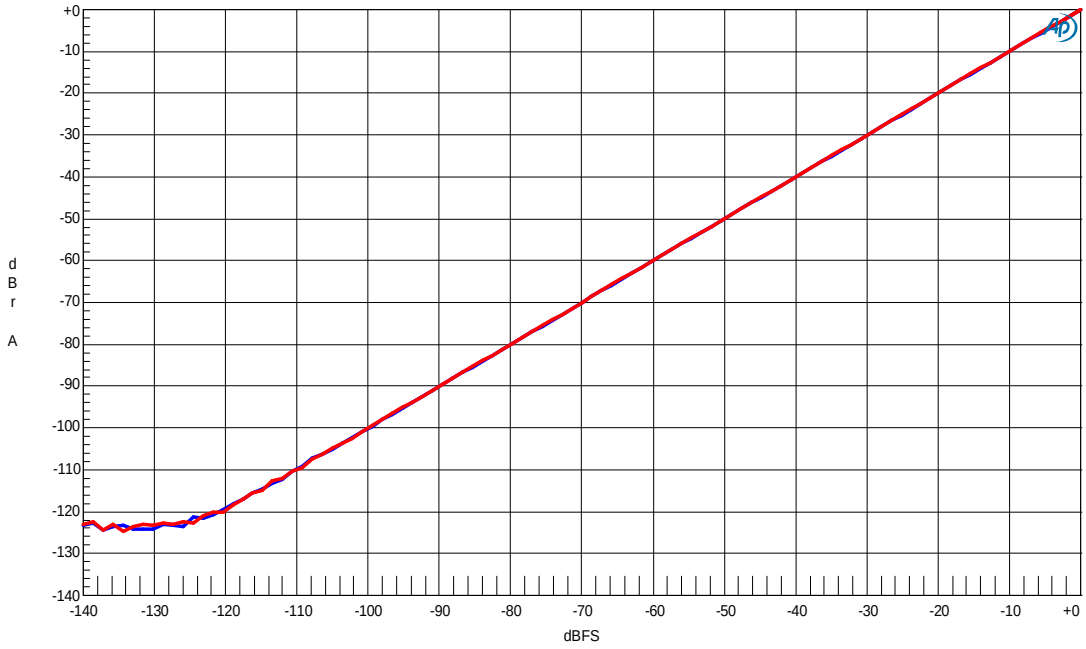

Figure 30. DAC1 – Linearity [fs = 48kHz]

AK4618 Frequency Response Single-end DAC (L/ROUT1)
[fs=48kHz, 0dBFS]

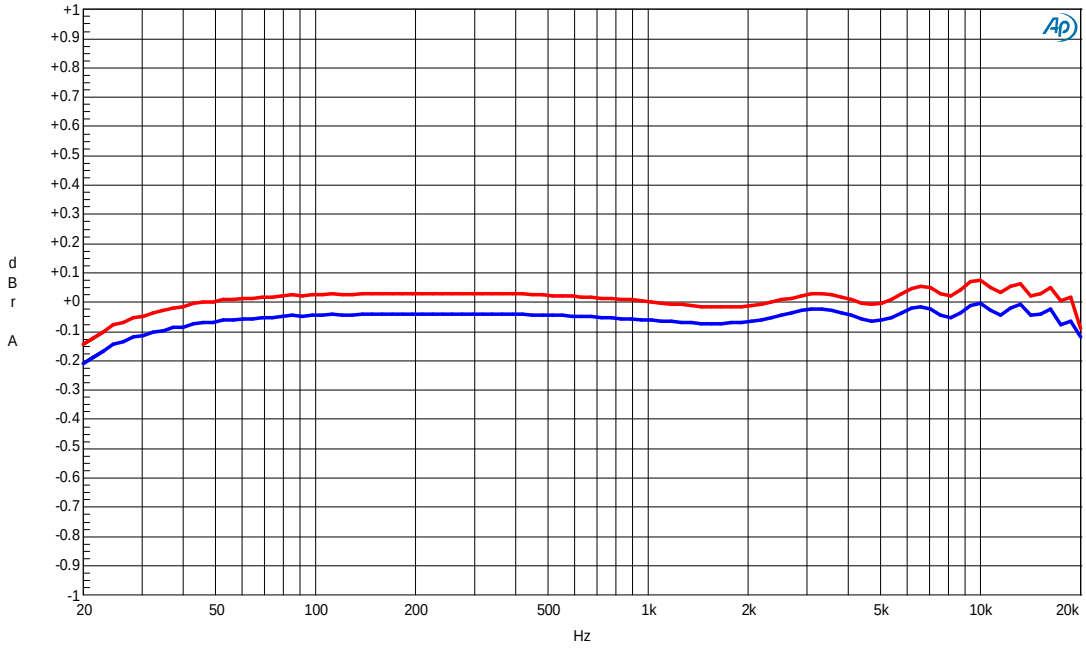

Figure 31. DAC1 – Frequency Response [fs = 48kHz]

AK4618 Crosstalk Single-end DAC (L/ROUT1)
[fs=48kHz, 0dBFS]

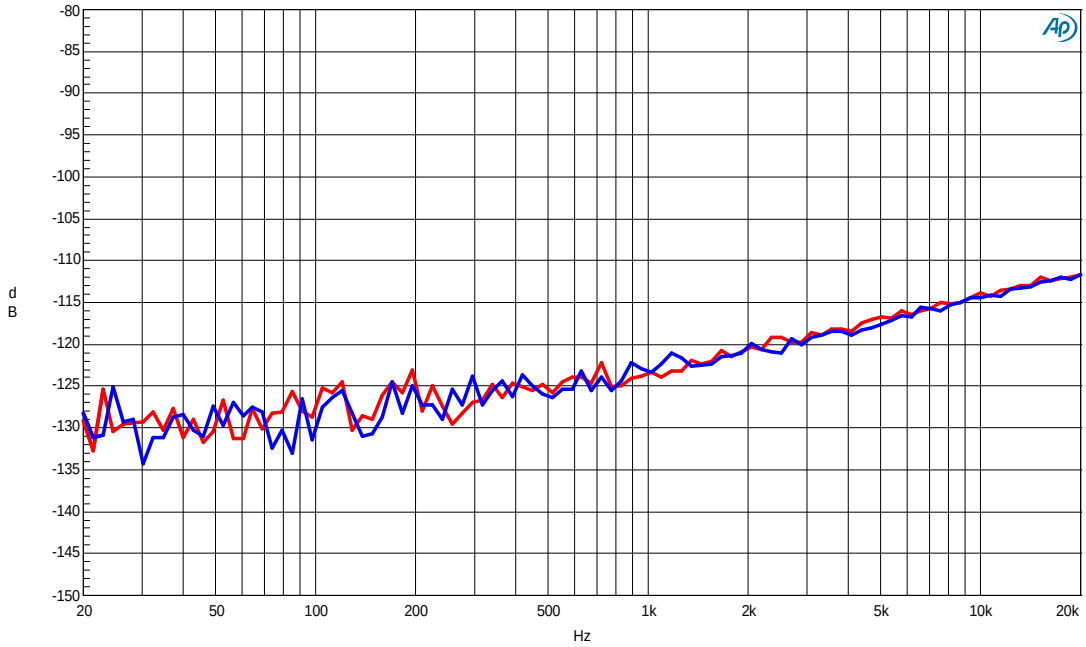

Figure 32. DAC1 – Crosstalk [fs = 48kHz]

REVISION HISTORY

Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
13/09/04	KM113500	0	First edition		

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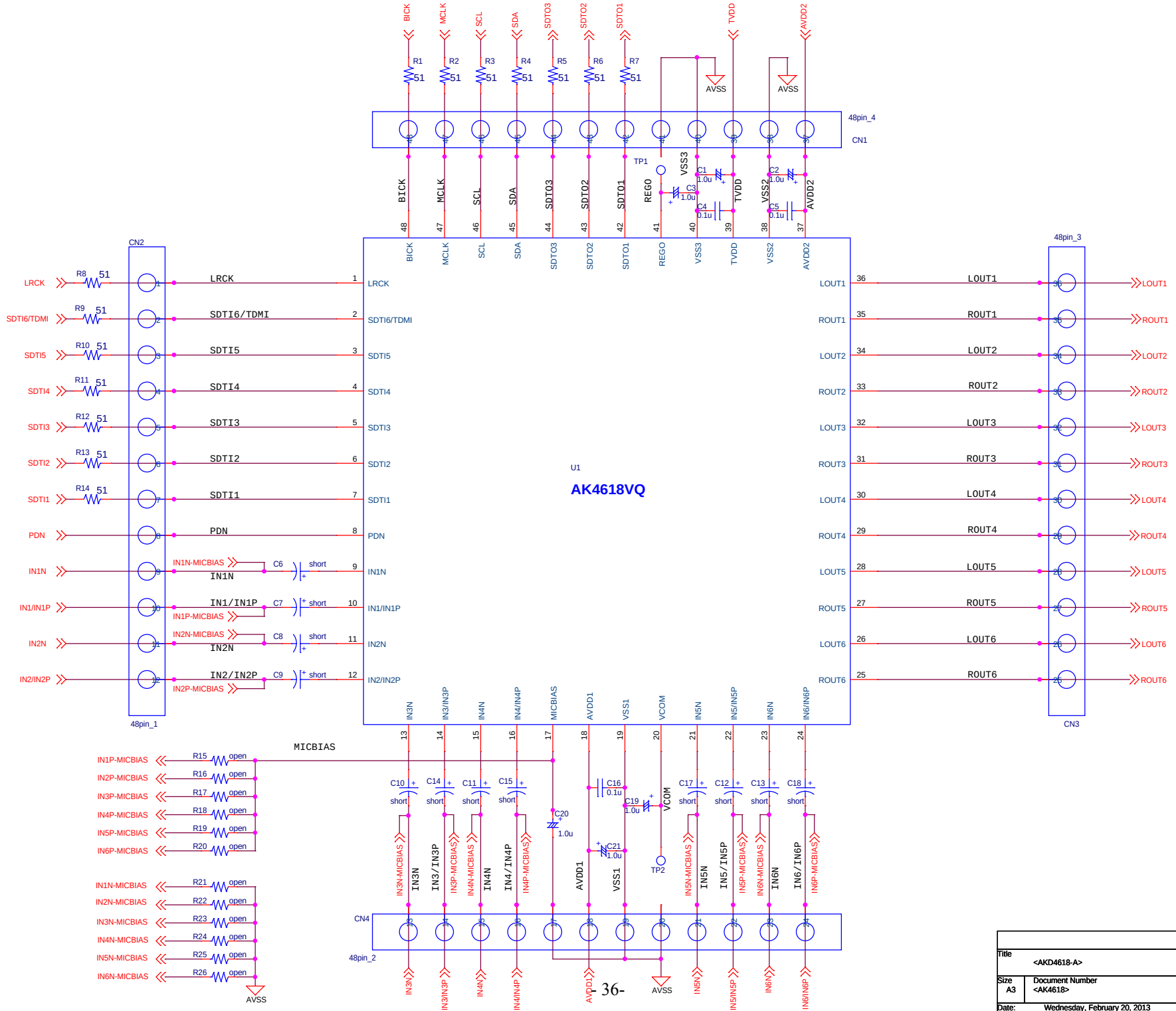

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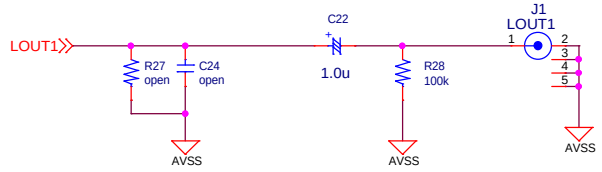
Size A3	Document Number <AK4618>	Rev <0>
Date: Wednesday, February 20, 2013	Sheet 1 of 7	

LOUT1



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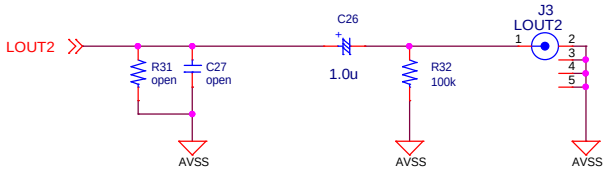

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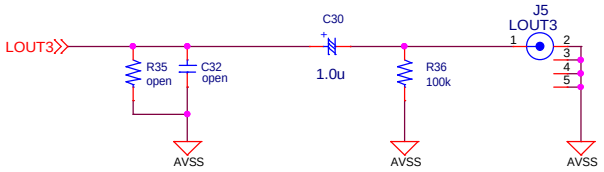
LOUT3



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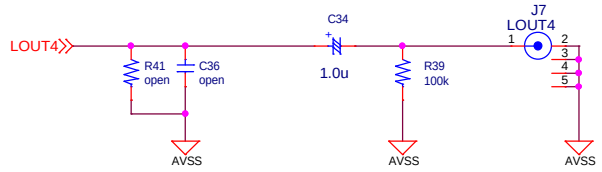

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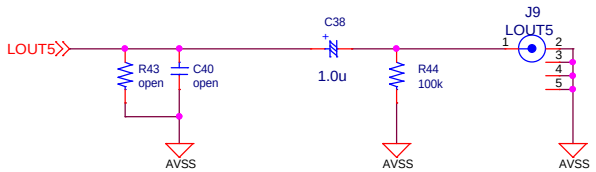
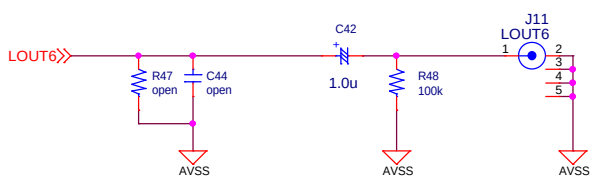


LOUT5

LOUT6



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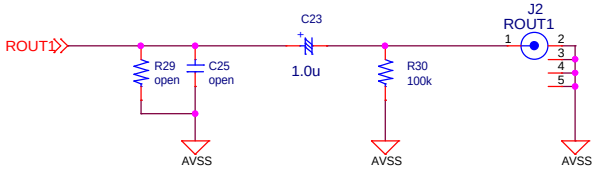
ROUT1



ROUT1

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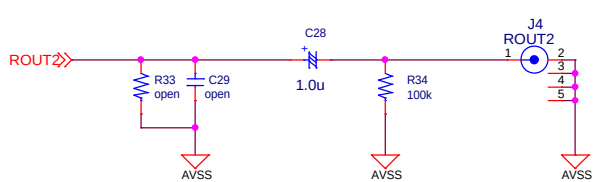
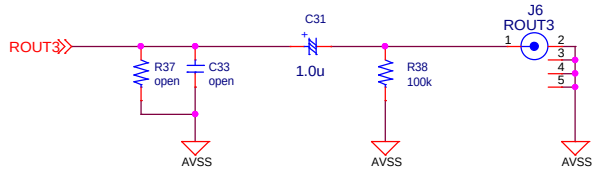


ROUT2

ROUT3



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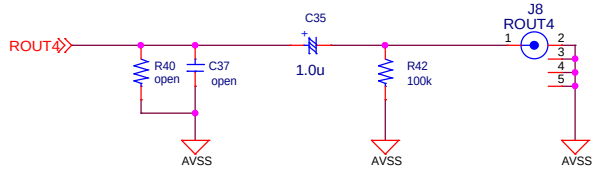

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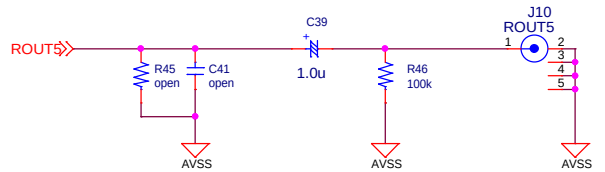

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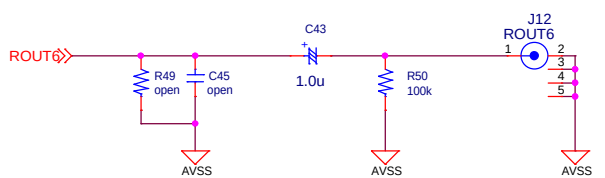
ROUT6



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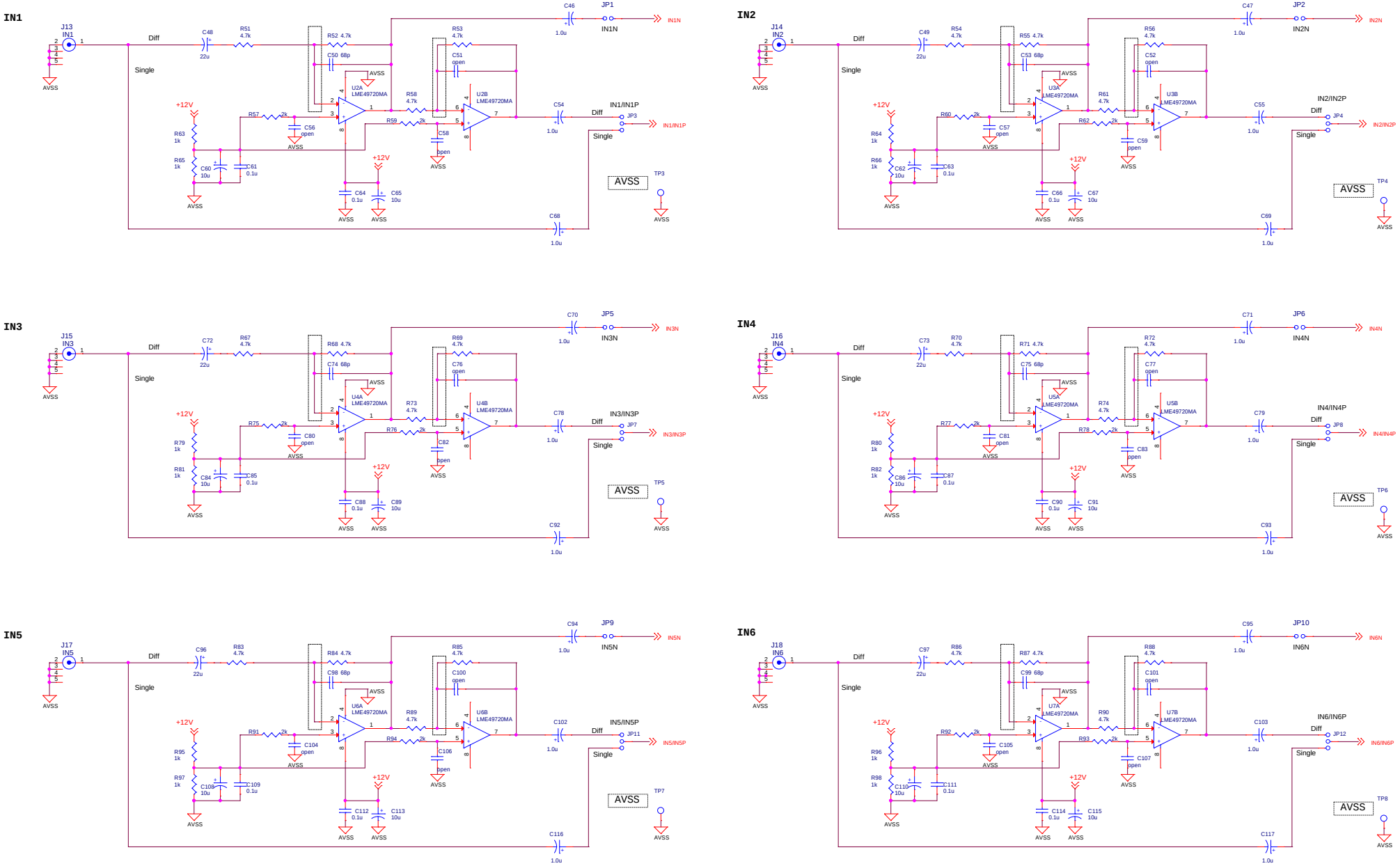
AREA: SHORTEST WIRING



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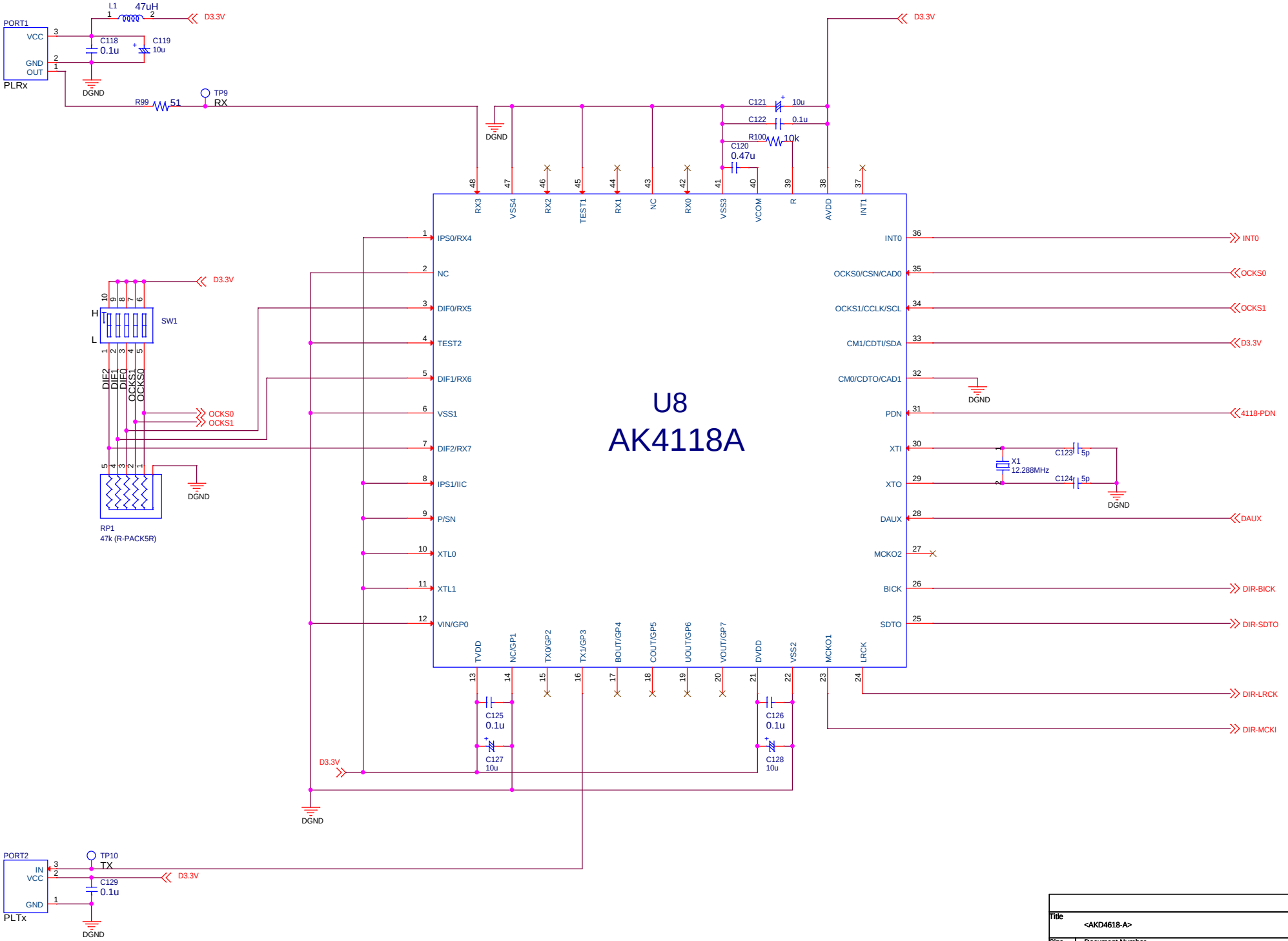

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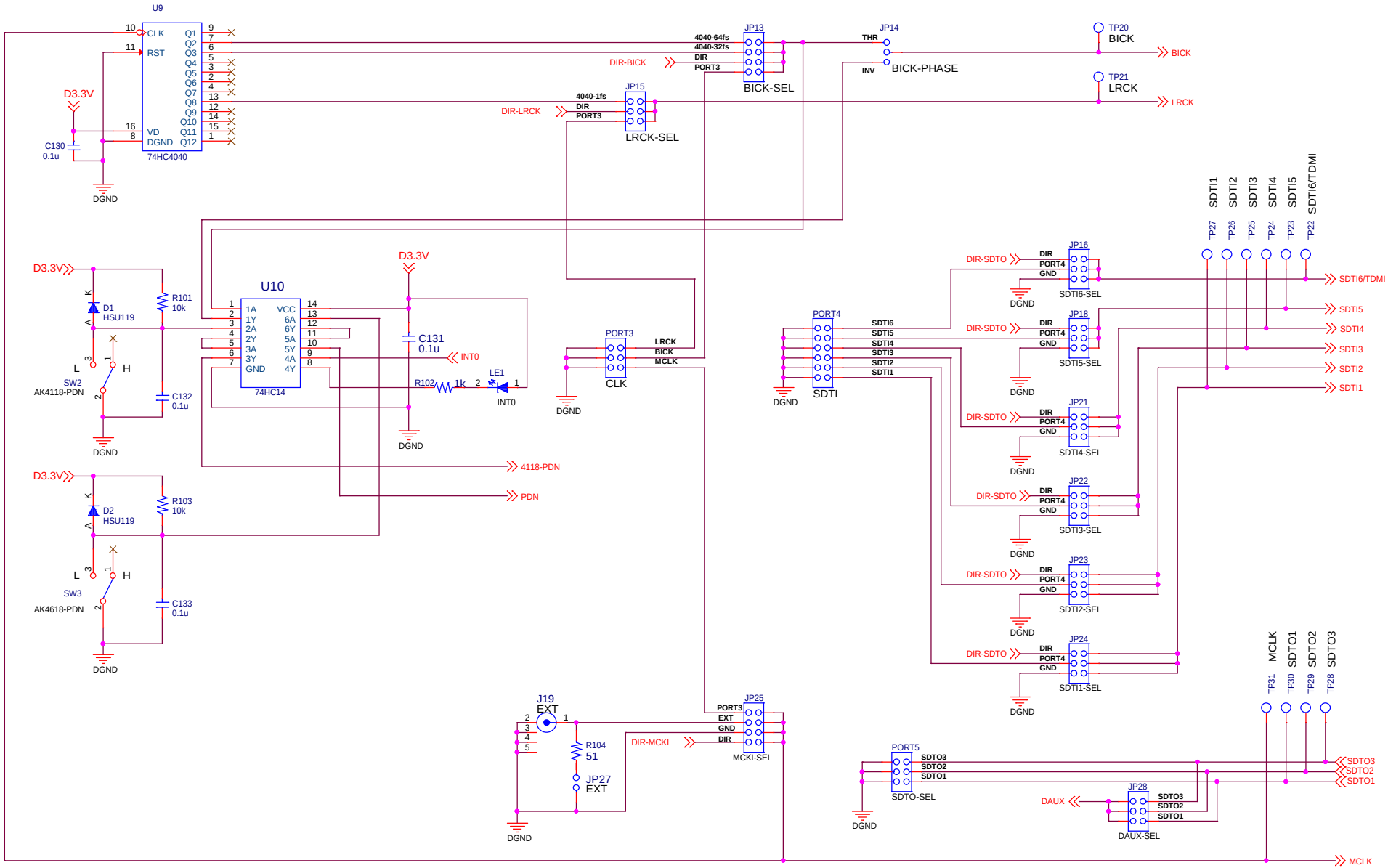

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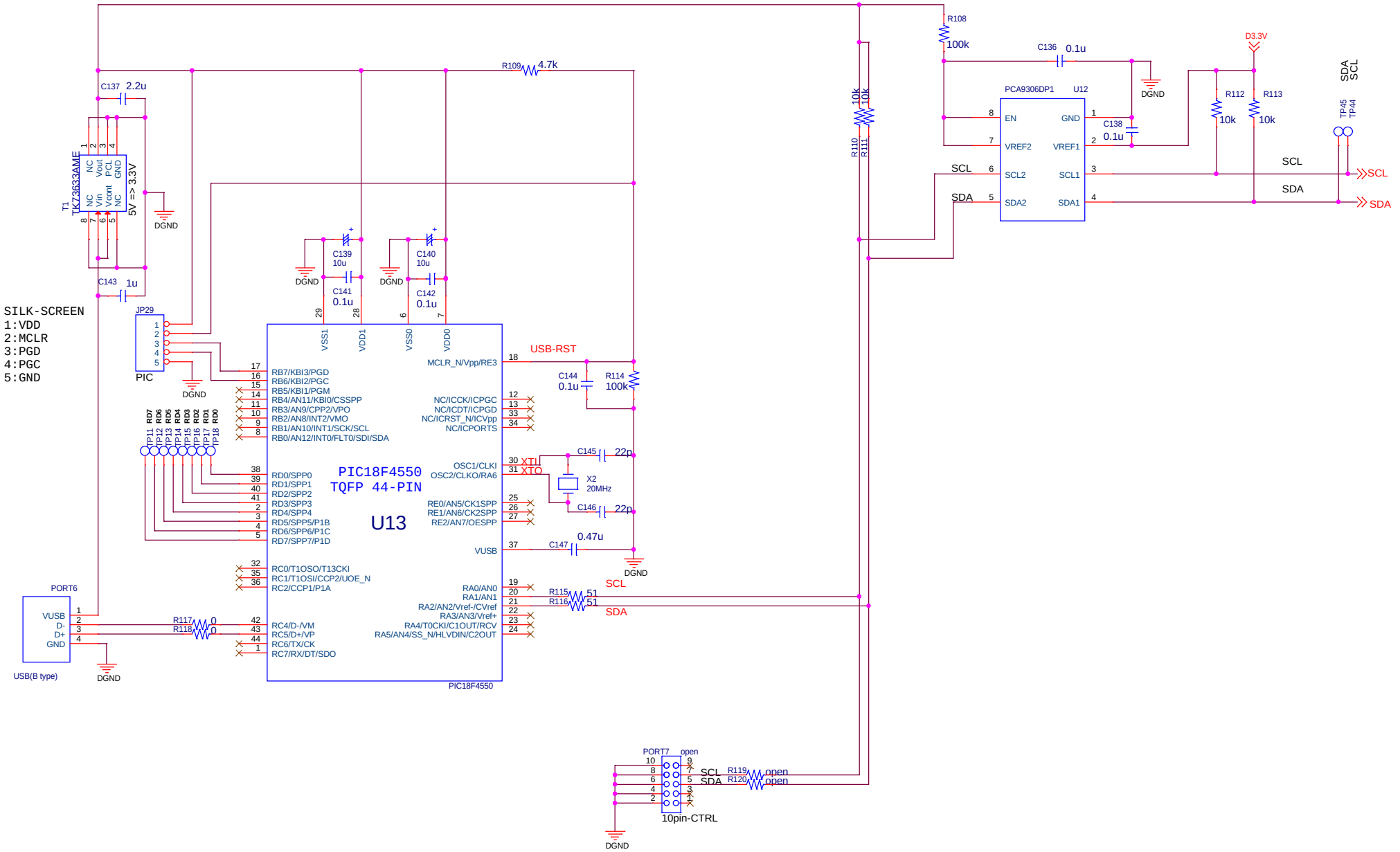

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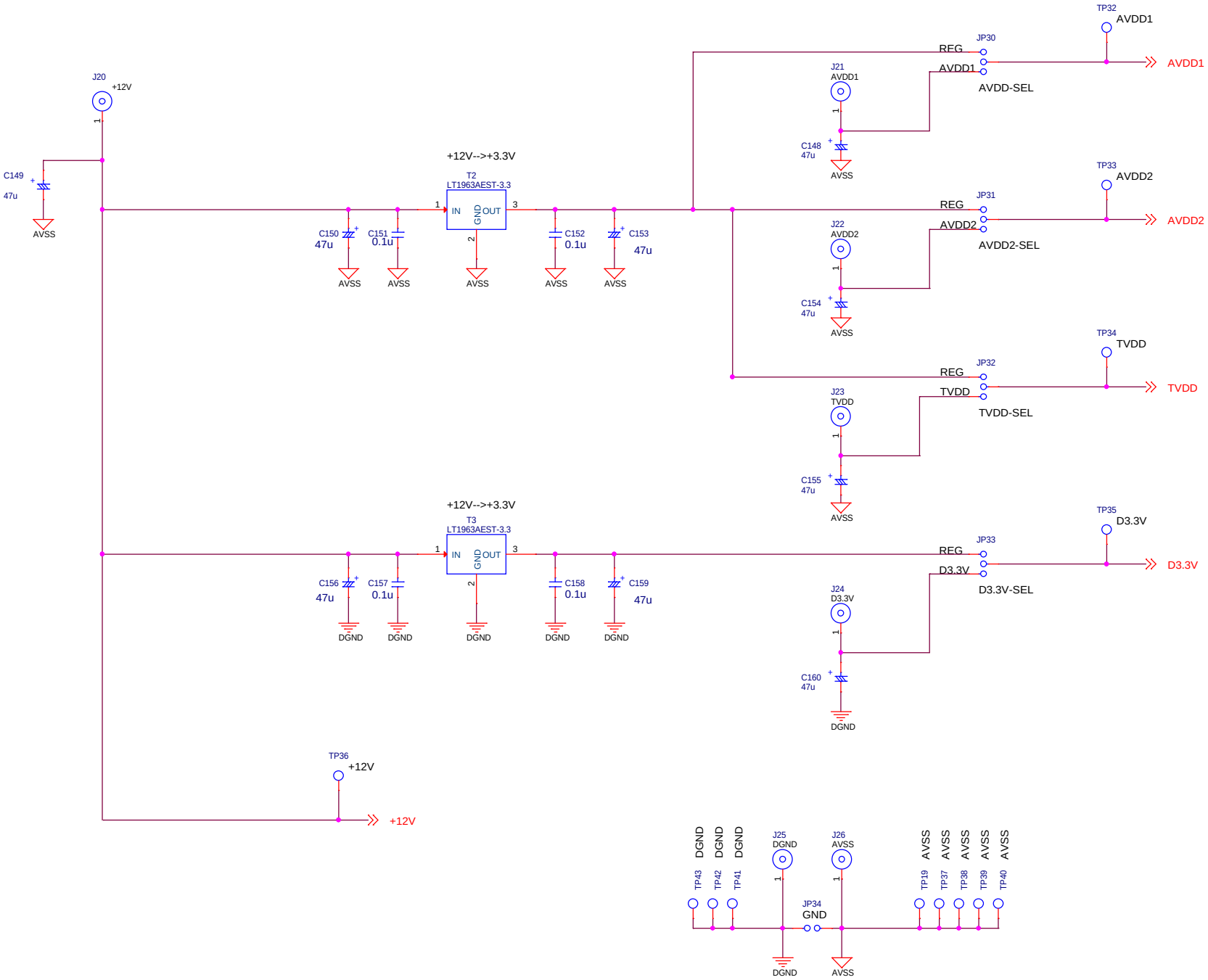
Date: Wednesday, February 20, 2013	Sheet 6 of 7	



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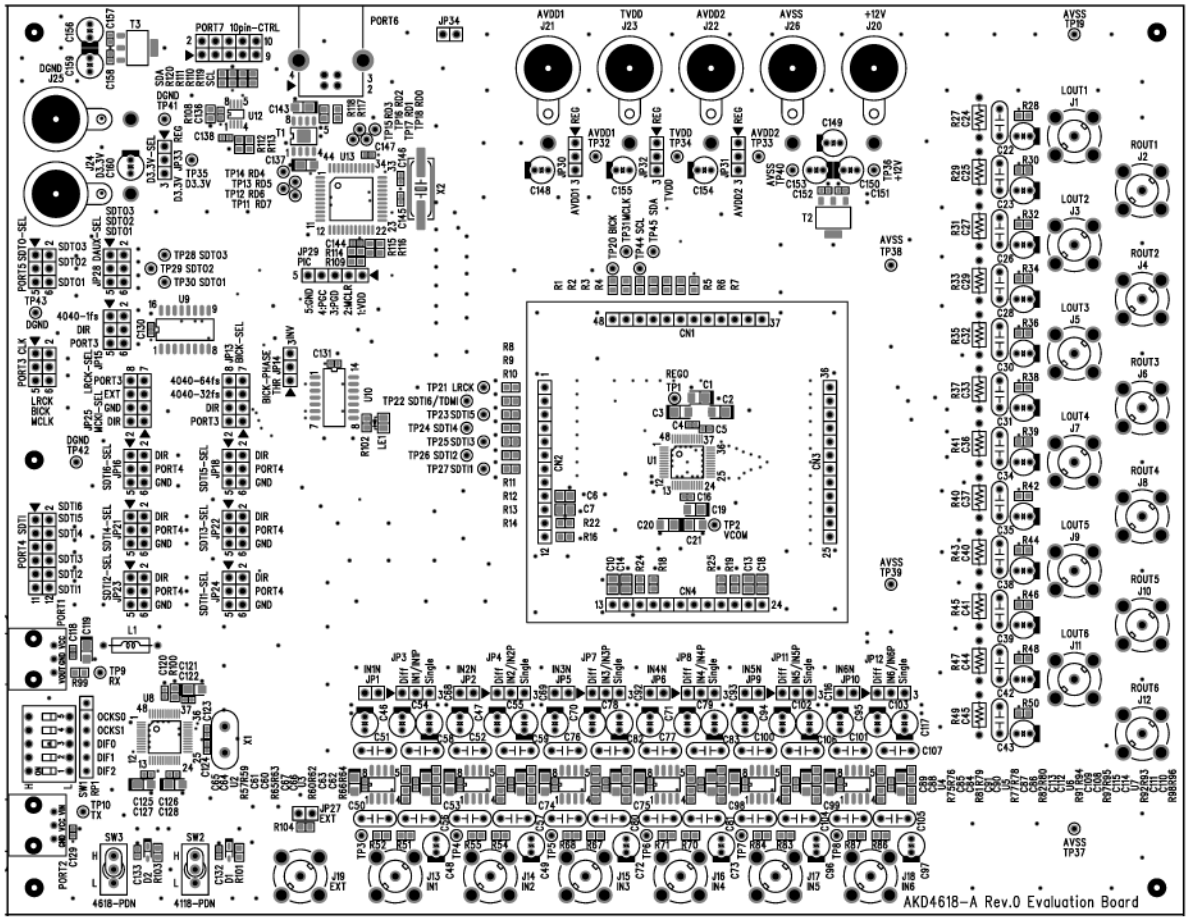
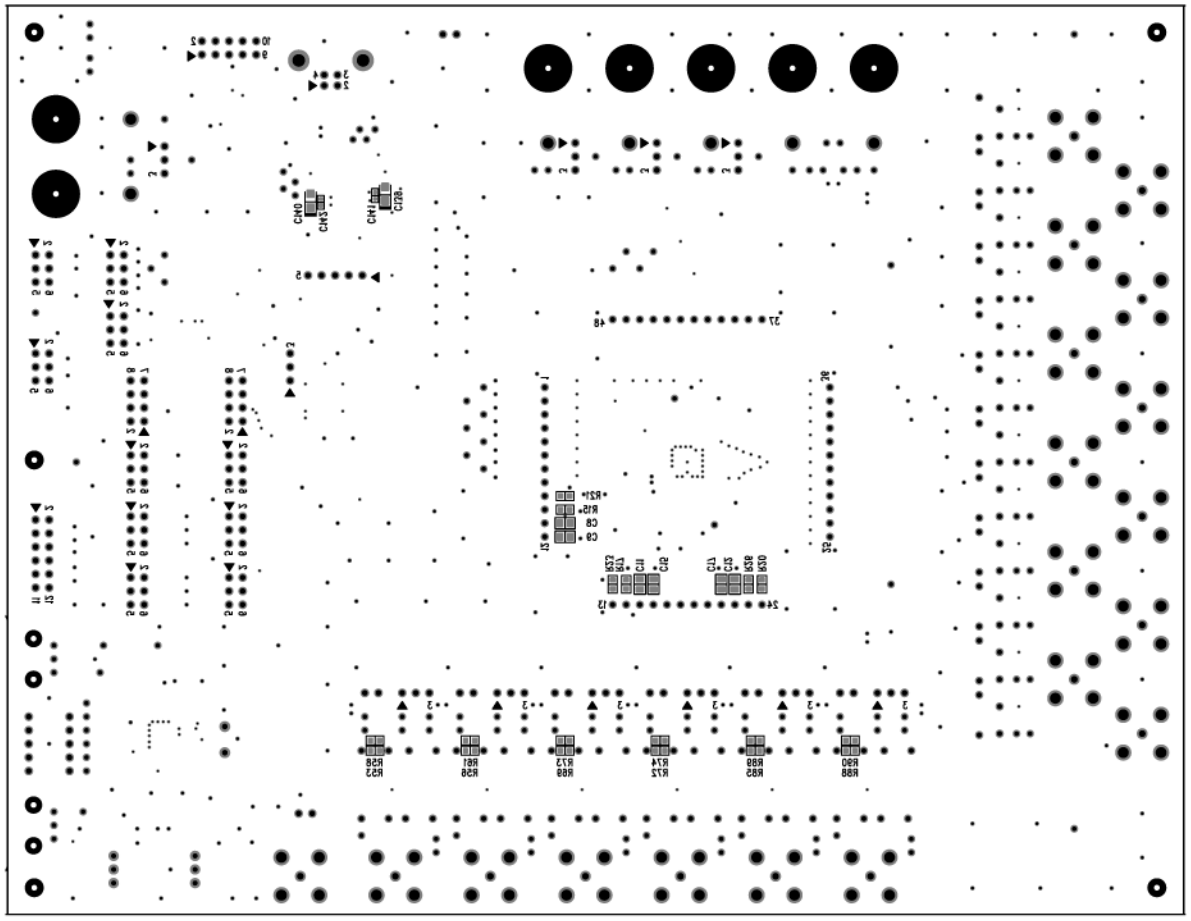
部品面シルク図　　部品面透視図



半田面シルク図　　部品面透視図



部品面パターン図　　部品面透視図