EE314 Term Project - Spring 2022

FPGA Implementation of Simple Quality of Service (QoS) based Queuing

Evaluation Rubric

Your project demonstrations are going to be evaluated according to the following rubric.

Part	Explanation	Points
VGA - Buffers	4 buffers with different colors (*)	/10
	Packet insertion to/deletion from buffers	/10
VGA - Text	Number of transmitted/received/dropped packets (**)	/10
VGA - Quality	No undesirable effects (weird colors, lines etc)	/5
Operation – Packet Input	A new packet is input using Start/0/1 buttons	/10
Operation – Packet Read	Every 3 seconds a packet is read	/10
	Packets are read in first in first out manner	/5
Operation – Latency Requirement	Lowest latency for buffer 1	/10
Operation – Reliability Requirement	Lowest drop rate for buffer 4	/10
Operation - Text	Correct numbers of transmitted/received/dropped packets are written	/10
Integration	The system works as a whole	/10
	Total	/100

(*) A still image is accepted for this part

(**) To get full credit from this part, numbers must be variable. A still image will only get partial credit.

Full points announced above corresponds to **12 pts** of 20 pts total project grade.

You are going to present your project as a group. Each of group member will be asked to talk about the project. Furthermore, some questions related to the project will be asked to members individually. **4 pts** of 20 pts will be given from this individual performance.

You are expected to submit one final report by 07/07/2022, 10.00. Late submission will not be accepted even with a point reduction.

The final report should be in IEEE Journal format, which you can find from the IEEE website either in Word or in LaTeX format. The report should include abstract, introduction and conclusion parts. You should report your approach to the problem, solution ideas, state diagrams, simulation results, and some demonstration photos of your project. The report will constitute remaining **4 pts** of 20 pts.