



# **EE446 PROJECT REPORT**

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## Introduction

The effective execution of instructions is essential for improving the performance of contemporary processors in the constantly developing field of computer architecture. To increase instruction throughput, pipelining, a method that facilitates the simultaneous execution of several instructions, has gained popularity. The smooth flow of instructions across the pipeline, however, may be hampered by risks, which are a new problem brought on by pipelining.

By adding a **hazard unit** and a **branch predictor**, this experiment seeks to improve the functionality of a 32-bit pipelined processor created in a prior Laboratory Work. Two categories of hazards will be detected and handled by the hazard unit, ensuring that pipeline instructions are carried out correctly. On the other side, the branch predictor will boost processor speed by correctly anticipating the results of branch instructions.

The hazard unit and branch predictor must be implemented on a working pipelined processor. This project makes use of the earlier work that was completed in the fourth lab to increase the processor's capabilities. By including the hazard unit and branch predictor into the current **Datapath** and **Control Unit**, we hope to create a processor design that is more dependable and efficient.

Three mechanisms—**flush**, **stall**, and **forward**—will be the main ones used by the hazard unit. A hazard is recognized, and the flush mechanism clears the stage register linked to it, deleting its output. The pipeline is filled with a bubble to eliminate the risk, and the stall mechanism holds the value of a stage register. Finally, the forward mechanism enables the transmission of calculated values to earlier stages, facilitating the elimination of hazards and uninterrupted instruction execution.

The branch target buffer (BTB), global branch history register (GHR), and pattern table make up the branch predictor, an essential aspect of contemporary CPUs. To predict the target of upcoming branches, the branch target buffer holds the program counters (PCs) and associated branch target addresses of recent branch instructions. The global branch history record keeps track of previous branch outcomes, which helps with forecast accuracy. Based on past trends, the pattern table serves as a lookup table to help determine the most likely branch outcome.

By bringing these improvements into practice, we want to increase the pipelined processor's effectiveness at handling risks and forecasting branch outcomes. This project provides an excellent chance to delve further into the intricate details of computer architecture while investigating workable solutions to problems posed by current processor architectures.

## ISA to be Implemented

*Figure 1* illustrates how the processor design for this project will be concentrated on a limited set of ARM instructions. Not all ARM instructions will be supported by this processor. However, it will provide support for conditional logic, specifically the EQ (equal), NE (not equal), and AL (always) conditions, with the Z flag being the only significant condition. If the condition is EQ, the processor will assess the zero flag to decide whether to carry out the instruction or not.

Mnemonic	Name		Operation
ADD	Addition	add Rd,Rn,Rm	$Rd \leftarrow Rn + (Rm \text{ sh } shamt5)$
SUB	Subtraction	sub Rd,Rn,Rm	$Rd \leftarrow Rn - (Rm \text{ sh } shamt5)$
AND	Bitwise And	and Rd,Rn,Rm	$Rd \leftarrow Rn \& (Rm \text{ sh } shamt5)$
ORR	Bitwise Or	orr Rd,Rn,Rm	$Rd \leftarrow Rn   (Rm \text{ sh } shamt5)$
MOV	Move to Register	mov Rd,Rm	$Rd \leftarrow (Rm \text{ sh } shamt5)$
MOV	Move to Register	mov Rd,rot-imm8	$Rd \leftarrow (imm8 \text{ rr } rot < 1)$
STR	Store	str Rd,[Rn,imm12]	$Mem[Rn + imm12] \leftarrow Rd$
LDR	Load	ldr Rd,[Rn,imm12]	$Rd \leftarrow Mem[Rn + imm12]$
CMP	Compare	cmp Rd,Rn,Rm	set the flag if $(Rn - Rm = 0)$
B	Branch	b imm24	$PC \leftarrow (PC + 8) + (imm24 < 2)$
BEQ	Branch if Equal	beq imm24	$PC \leftarrow (PC + 8) + (imm24 < 2)$ if flag = 1
BL	Branch with Link	bl imm24	$PC \leftarrow (PC + 8) + (imm24 < 2), R14 \leftarrow PC + 4$
BX	Branch and Exchange	bx Rm	$PC \leftarrow Rm$

Data Processing Instruction - Memory Instruction - Branch Instruction

Figure 1. ISA to be Implemented.

The new MOV instruction with an immediate operand is a major addition to the instruction set. The rotate field, a 4-bit unsigned integer describing a shift operation on an 8-bit immediate value, is part of the immediate operand. The immediate value is rotated right by twice the value in the rotate field after being zero-extended to 32 bits. This method makes it possible to generate common constants quickly and effectively, increasing the processor's adaptability. It is essential to note that this processor will carry out instructions involving the transfer of another register to the PC, such as BX. These instructions will not be handled by the branch predictor, nevertheless.

## Datapath Changes

As it can be seen from Figure 2, additional MUXs (4x1 MUX) are added to utilize the forwarding signals generated at the Hazard Unit. However, the Datapath design in Figure 2 **does not** contain all the changes, for the overall project. It is only added to visualize the 5-stage Pipelined Computer Architecture with the Hazard Unit.





[illegible]

Figure 6. COCOTB results from the Memory and Write Back stages of the altered MOV instruction.

## Hazard Unit

The implemented hazard unit for this project will deal with two different types of dangers to handle the difficulties brought on by risks in the pipeline.

**Forwarding** method will be used to mitigate data hazards and assure effective execution without adding extra cycles. Forwarding will be used to deliver the necessary data immediately from the executing instruction to the dependent instruction, removing the requirement for pausing, when a data risk occurs as a result of activities involving registers.

On the other hand, control hazards arise when the decision regarding the next instruction to fetch has not yet been determined at the time of the fetch operation. A **branch predictor** will be used by branch procedures that use immediate values, such as B, BL, and their conditional variations. To enhance overall performance, the branch predictor seeks to accurately predict how these branches will turn out. The predictor could, however, make a mistake in its forecasts. In these circumstances, it is necessary to **flush** the pipeline with the goal of discarding the incorrectly obtained instructions and resume execution using the results of the correct branch.

### Matching and Forwarding of Operand AE:

- **Match\_1E\_M** checks if the register being read in the first execute stage (RA1E) matches the register being written to in the third memory stage (WA3M).
- **Match\_1E\_W** checks if RA1E matches WA3W, the register being written to in the third writeback stage (WA3W).
- If **Match\_1E\_M** is true and there is a register write in the memory stage (RegWriteM), the value from ALUOutM is forwarded to the first execute stage as the source operand AE (ForwardAE = 10).
- If **Match\_1E\_W** is true and there is a register write in the writeback stage (RegWriteW), the value from ResultW is forwarded to the first execute stage as the source operand AE (ForwardAE = 01).
- If neither **Match\_1E\_M** nor **Match\_1E\_W** is true, the source operand AE is obtained from the register file (ForwardAE = 00).

### Matching and Forwarding of Operand BE:

- **Match\_2E\_M** checks if the register being read in the second execute stage (RA2E) matches the register being written to in the third memory stage (WA3M).
- **Match\_2E\_W** checks if RA2E matches WA3W, the register being written to in the third writeback stage (WA3W).
- If **Match\_2E\_M** is true and there is a register write in the memory stage (RegWriteM), the value from ALUOutM is forwarded to the second execute stage as the source operand BE (ForwardBE = 10).
- If **Match\_2E\_W** is true and there is a register write in the writeback stage (RegWriteW), the value from ResultW is forwarded to the second execute stage as the source operand BE (ForwardBE = 01).
- If neither **Match\_2E\_M** nor **Match\_2E\_W** is true, the source operand BE is obtained either from ExtImmE or the register file (depending on another multiplexer).

### Hazard Unit Operations:

- **Match\_12D\_E** checks if either RA1D or RA2D matches WA3E, the register being written to in the third execute stage. It determines if there is a hazard in the decode stage due to instructions reading the same register that is being written in the execute stage.
- **LDRstall** is asserted if there is a match in **Match\_12D\_E** and MemtoRegE is true, indicating a data hazard caused by a memory operation. It causes a minimal amount of stalling to resolve the hazard.
- **BranchTakenE** is determined by BranchE and CondEx, indicating if a branch instruction is taken in the execute stage.
- **PCWrPendingF** is the combination of PCSrcD, PCSrcE, and PCSrcM, determining if there is a pending PC write in the fetch stage. This is used to stall the fetch stage and flush the decode stage.
- **StallF** is asserted when there is **LDRstall** or **PCWrPendingF** to stall the fetch stage. However, it is not asserted during PCSrcW to allow the write. It remains asserted continuously for three cycles once PCS=1 is decoded.
- **StallD** is asserted if there is **LDRstall**, causing stalling in the decode stage.
- **FlushD** is asserted when there is **PCWrPendingF**, PCSrcW, or **BranchTakenE**, indicating that the decode stage needs to be flushed.



- **FlushE** is asserted when there is **LDRstall** or **BranchTakenE**, signifying the need to flush the execute stage.

```
# ADD R7, R2, R1 (6 + 1 = 7)
# 0xE0827001
dut._log.info(f"ADD R7, R2, R1")
await clkedge
assert dut.OUT.value == 6
print_all(dut)

# ADD R8, R7, R1 (7 + 1 = 8)
# 0xE0878001
await clkedge
assert dut.OUT.value == 1
print_all(dut)
```

Figure 7. Testing forwarding (ForwardAE) with 2 ADD instructions run consecutively.

[illegible]

Figure 8. Testing forwarding (ForwardAE = 10) with COCOTB.

```
# ADD R8, R7, R1 (7 + 1 = 8)
# 0x00878001
await clkedge
assert dut.OUT.value == 1
print_all(dut)

print("\n R1 = 1\n R2 = 6\n R3 = 9\n")

# NOP
await clkedge
print_all(dut)

# ADD R9, R1, R8 (1 + 8 = 7)
# 0x00819008
dut._log.info(f"ADD R7, R2, R1")
await clkedge
print_all(dut)
```

Figure 9. Testing forwarding (ForwardBE) with 2 ADD instructions run consecutively.



```

R1 = 1
R2 = 6
R3 = 9
R7 = 7

115000.00ns INFO cocotb.Main INSTR: H: f0000000
115000.00ns INFO cocotb.Main PCPrime: D: 44 H: 2c B: 0000000000000000000000000101100
115000.00ns INFO cocotb.Main PCF: D: 40 H: 28 B: 0000000000000000000000000101000
115000.00ns INFO cocotb.Main RegWriteE: D: 1 H: 1 B: 1
115000.00ns INFO cocotb.Main RegWriteW: D: 1 H: 1 B: 1
115000.00ns INFO cocotb.Main ALUControlE: D: 4 H: 4 B: 0100
115000.00ns INFO cocotb.Main CondE: D: 14 H: e B: 1110
115000.00ns INFO cocotb.Main RA1E: D: 1 H: 1 B: 0001
115000.00ns INFO cocotb.Main RA2E: D: 8 H: 8 B: 1000
115000.00ns INFO cocotb.Main ForwardBE: D: 1 H: 1 B: 01
115000.00ns INFO cocotb.Main WA3E: D: 9 H: 9 B: 1001
115000.00ns INFO cocotb.Main WA3W: D: 8 H: 8 B: 1000
115000.00ns INFO cocotb.Main SrcAE: D: 1 H: 1 B: 00000000000000000000000000000001
115000.00ns INFO cocotb.Main SrcBE: D: 8 H: 8 B: 000000000000000000000000000001000
115000.00ns INFO cocotb.Main ReadDataM: D: 6 H: 6 B: 00000000000000000000000000000110
115000.00ns INFO cocotb.Main ReadDataW: D: 1 H: 1 B: 00000000000000000000000000000001
115000.00ns INFO cocotb.Main ALUResultE: D: 9 H: 9 B: 000000000000000000000000000001001
115000.00ns INFO cocotb.Main ALUOutW: D: 8 H: 8 B: 000000000000000000000000000001000
115000.00ns INFO cocotb.Main OUT: D: 8 H: 8 B: 000000000000000000000000000001000

-----
R1 = 1
R2 = 6
R3 = 9
R7 = 7
R8 = 8

```

Figure 10. Testing forwarding (ForwardBE = 01) with COCOTB.

```

# LDR R2, [R0] => 2
# 0xE410200C
dut._log.info(f"LDR R2, [R0] => 12")
await clkedge
print_all(dut)

# SUB R3, R3, R2 => (9 - 2) = 7
# 0xE0433002
dut._log.info(f"SUB R3, R3, R2 => (9 - 2) = 7")
await clkedge
print_all(dut)

```

Figure 11. Testing LDRstall.

```

-----
165000.00ns INFO cocotb.Main InstructionF: H: f0000000
165000.00ns INFO cocotb.Main INSTR: H: e0433002
165000.00ns INFO cocotb.Main PCPrime: D: 64 H: 40 B: 00000000000000000000000001000000
165000.00ns INFO cocotb.Main PCF: D: 60 H: 3c B: 0000000000000000000000000111100
165000.00ns INFO cocotb.Main RegWriteD: D: 1 H: 1 B: 1
165000.00ns INFO cocotb.Main RegWriteE: D: 1 H: 1 B: 1
165000.00ns INFO cocotb.Main ALUControlE: D: 4 H: 4 B: 0100
165000.00ns INFO cocotb.Main ALUSrcE: D: 1 H: 1 B: 1
165000.00ns INFO cocotb.Main CondE: D: 14 H: e B: 1110
165000.00ns INFO cocotb.Main RA1D: D: 3 H: 3 B: 0011
165000.00ns INFO cocotb.Main RA2D: D: 2 H: 2 B: 0010
165000.00ns INFO cocotb.Main RD1: D: 9 H: 9 B: 00000000000000000000000001001
165000.00ns INFO cocotb.Main RD2: D: 6 H: 6 B: 00000000000000000000000000000110
165000.00ns INFO cocotb.Main RA2E: D: 12 H: c B: 1100
165000.00ns INFO cocotb.Main StallF: D: 1 H: 1 B: 1
165000.00ns INFO cocotb.Main StallD: D: 1 H: 1 B: 1
165000.00ns INFO cocotb.Main FlushE: D: 1 H: 1 B: 1
165000.00ns INFO cocotb.Main LDRstall: D: 1 H: 1 B: 1
165000.00ns INFO cocotb.Main WA3E: D: 2 H: 2 B: 0010
165000.00ns INFO cocotb.Main SrcBE: D: 12 H: c B: 000000000000000000000000000001100
165000.00ns INFO cocotb.Main ReadDataM: D: 6 H: 6 B: 00000000000000000000000000000110
165000.00ns INFO cocotb.Main ReadDataW: D: 6 H: 6 B: 00000000000000000000000000000110
165000.00ns INFO cocotb.Main ALUResultE: D: 12 H: c B: 000000000000000000000000000001100
165000.00ns INFO cocotb.Main MemtoRegE: D: 1 H: 1 B: 1
165000.00ns INFO cocotb.Main OUT: D: 0 H: 0 B: 000000000000000000000000000000000

```

Figure 12. Testing LDRstall COCOTB results.

## Branch Prediction

### Branch Target Buffer (BTB):

- The BTB is a cache-like structure that stores the Program Counter (PC) values and their corresponding branch target addresses (BTAs).
- During the Fetch cycle, the PC value of the current instruction is used as an index to access the BTB.
- If a match is found in the BTB, the predicted target address is obtained from the corresponding entry.
- The predicted target address is used to fetch the next instruction in the Fetch cycle, assuming the branch is taken.

### Global Branch Register (GBR):

- The GBR is a register that maintains the historical outcomes of previous branch instructions.
- It is updated during the Execute cycle when the actual outcome of a branch instruction is determined.
- The GBR stores the branch history as a pattern of 1s and 0s, representing taken and not taken outcomes, respectively.
- The GBR is used in conjunction with the BTB to improve the accuracy of branch predictions.

### Fetch and Execute Cycle:

- In the Fetch cycle, the PC value is used to fetch the next instruction.
- If the predicted target address is available from the BTB, the next instruction is fetched from that address.
- In the Execute cycle, the branch instruction is evaluated, and the actual outcome is determined.
- If the prediction is accurate (branch taken), the subsequent instructions are fetched from the predicted target address.
- However, if the prediction is incorrect (branch not taken), measures need to be taken to retrieve the correct BTA or PC + 4.

### Measures for Incorrect Predictions:

- If the prediction is incorrect, the pipeline needs to be corrected to ensure the correct execution flow.
- One measure is to flush the incorrect instructions fetched based on the wrong prediction.
- The pipeline stages that follow the branch instruction, including the Fetch, Decode, and Execute stages, are flushed, discarding the incorrectly fetched instructions.
- The correct BTA or the PC + 4 (PC value incremented by 4) is then used to fetch the correct instructions.
- The pipeline continues execution from the correct target address, maintaining the correct program flow.

PC	Instruction
---	-----
0	LDR R1, #1;
4	LDR R2, #2;
8	LDR R3, #3;
12	SUB R3, R3, R1;
16	CMP R3, R2;
20	BEQ #12;
24	ADD R3, R3, R1;

*Figure 13. Sample subroutine for testing branch predictor.*

The sample subroutine in *Figure 13*, demonstrates the case when the branch predictor predicts that the branch will be taken, and the prediction is incorrect. Based on this prediction, the pipeline proceeds to fetch and decode instructions assuming the branch is taken, i.e., it will fetch the instruction at PC 12 next.

However, during the Execute stage, it is determined that the branch condition is not met, and the branch instruction is actually "not taken." The execution will continue with the subsequent instruction after the branch, which is ADD R3, R3, R1 at **PC 24**.

Since the branch prediction was incorrect, the pipeline needs to be corrected. The instructions fetched based on the wrong prediction need to be flushed. The correct program counter (PC) value, in this case, PC + 4 (PC 24 + 4 = 28), is used to fetch the correct instruction.

By flushing the pipeline and fetching from the correct PC value, the pipeline will resume execution with the correct instruction (ADD R3, R3, R1). This ensures that the program execution continues correctly based on the actual outcome of the branch instruction.

Sample Branch Predictor subroutine can be found in Figures 14-18. You can examine the Branch Target Buffer Output, BTB PC addresses that saved for Branch Predictor, BTB BTA addresses, GHR Outputs and Prediction signal generated from PTH. Note that: Only non-zero values are printed in this test environment.

Figure 14. COCOTB Test procedure for the Branch Predictor No.1.

Figure 15. COCOTB Test procedure for the Branch Predictor No.2.

Figure 16. COCOTB Test procedure for the Branch Predictor No.3.

Figure 17. COCOTB Test procedure for the Branch Predictor No.4.

