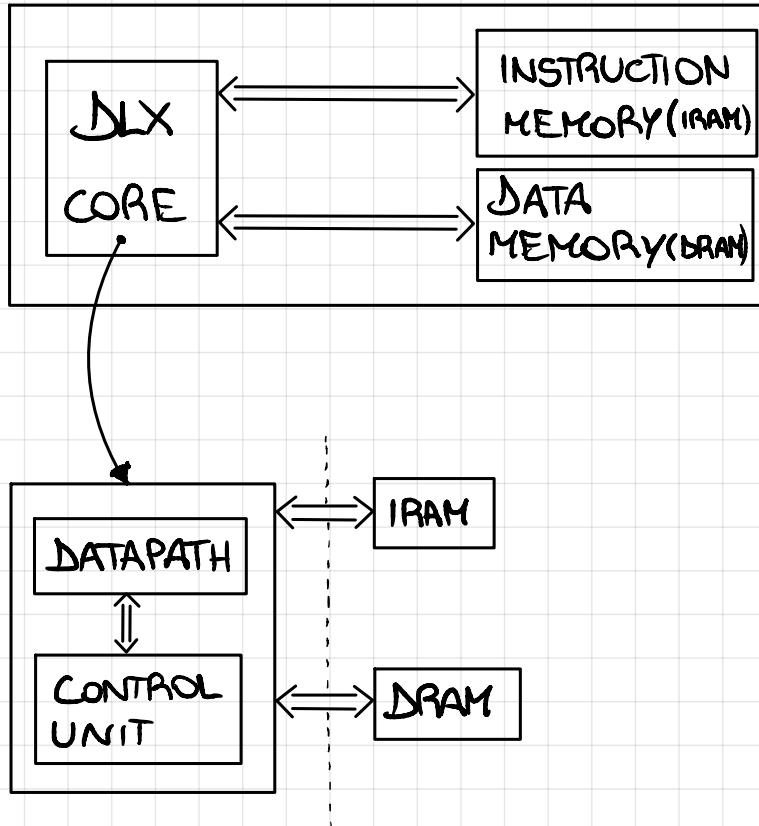
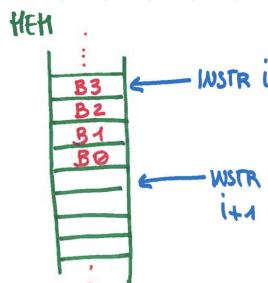


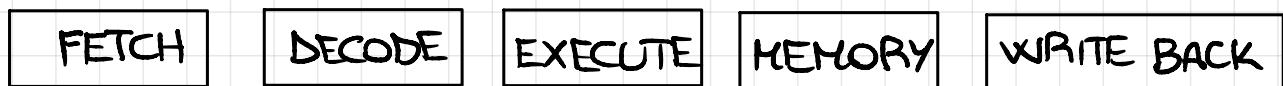
DLX TOP



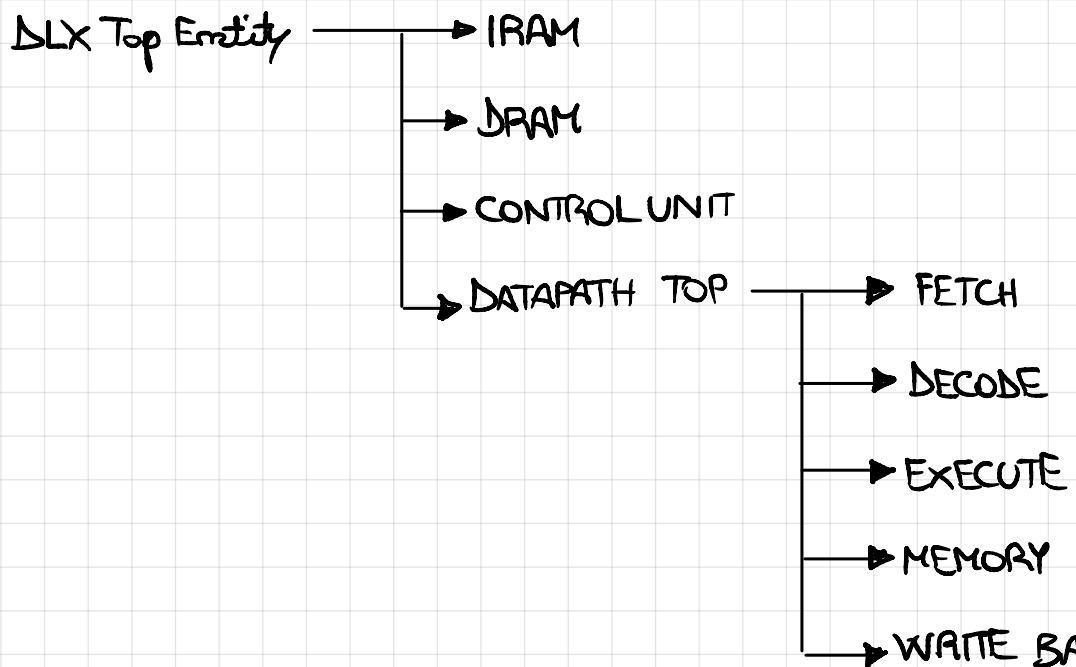
DLX memory is a byte addressable memory in BIG ENDIAN

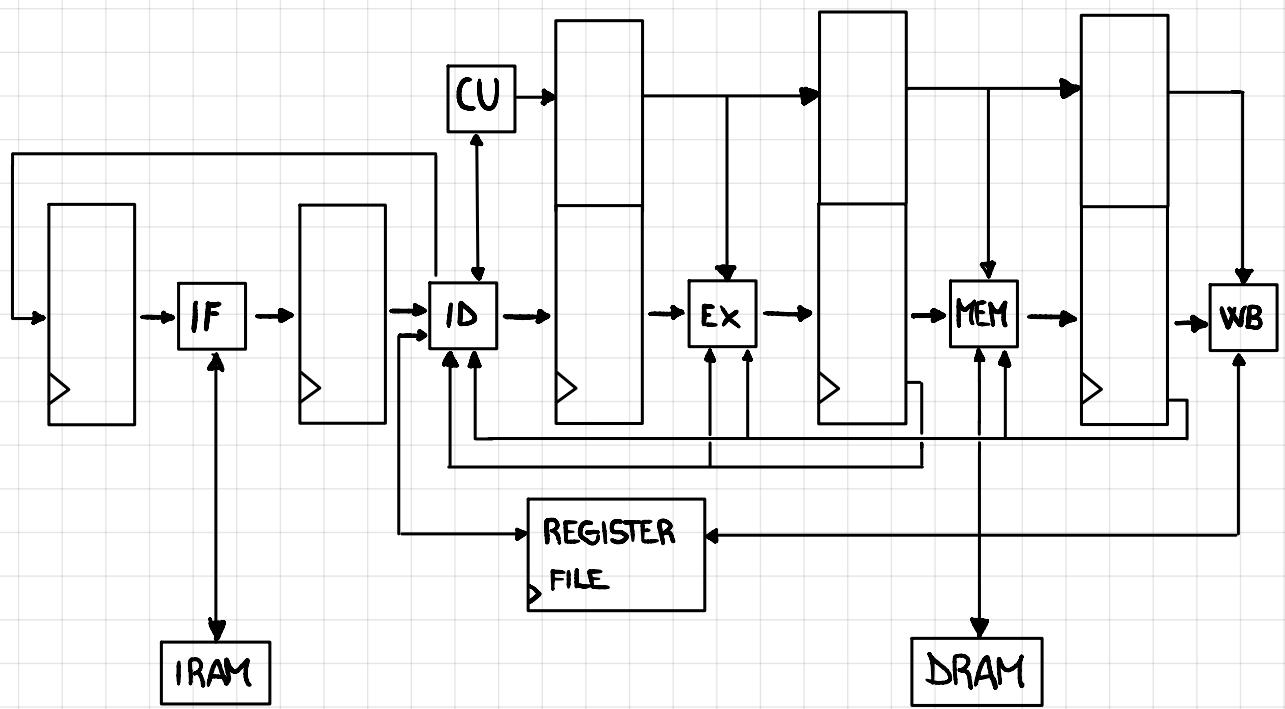


DATAPATH

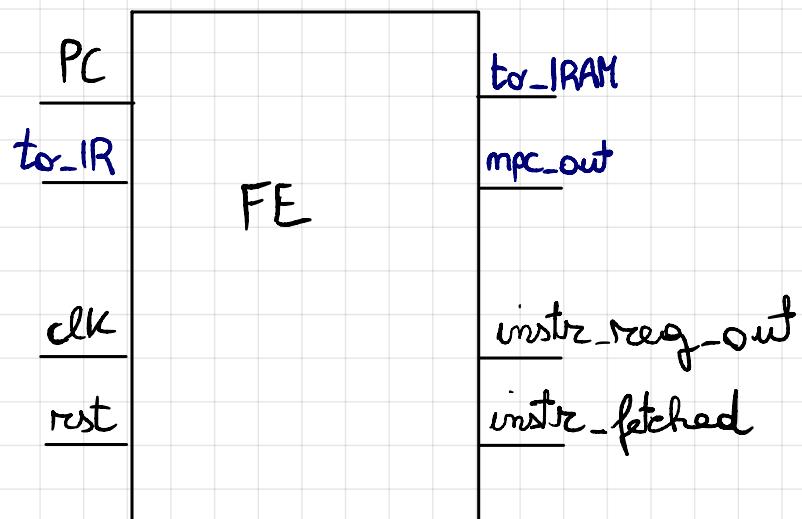


FILES

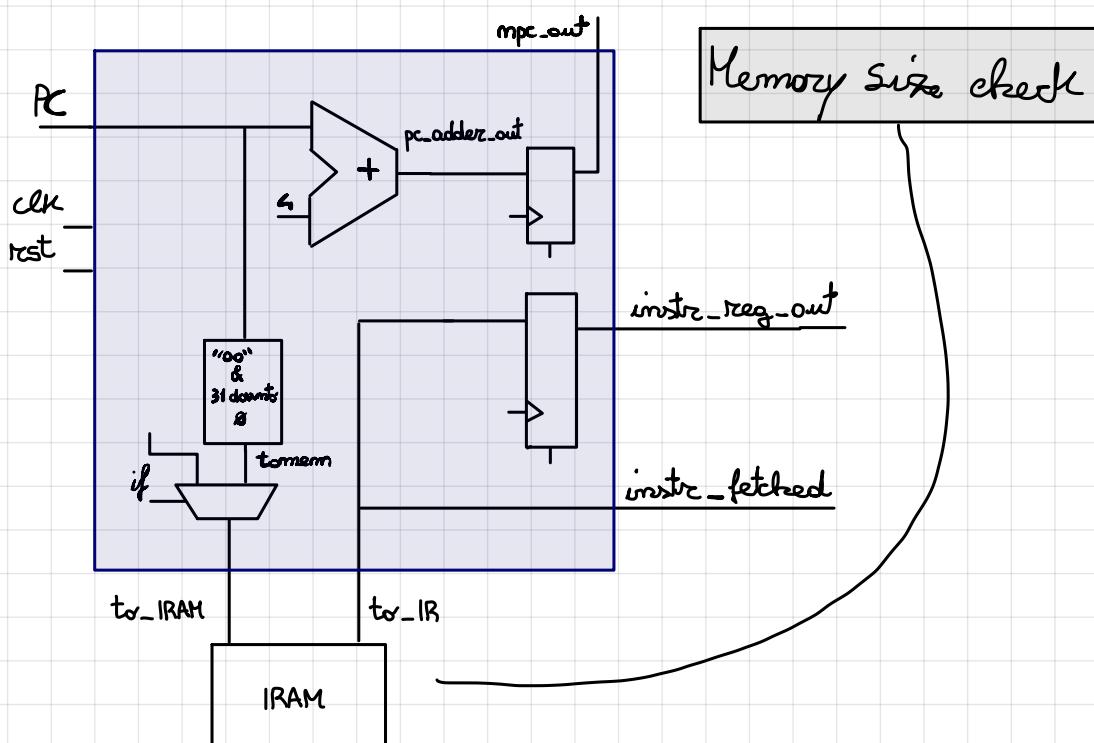
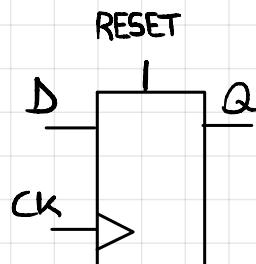




Fetch unit

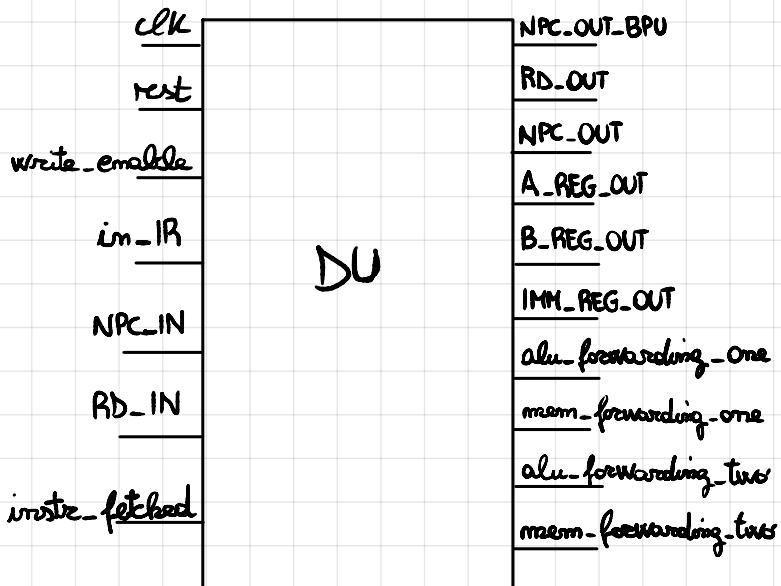


The register of the fetch unit is made of D-FF

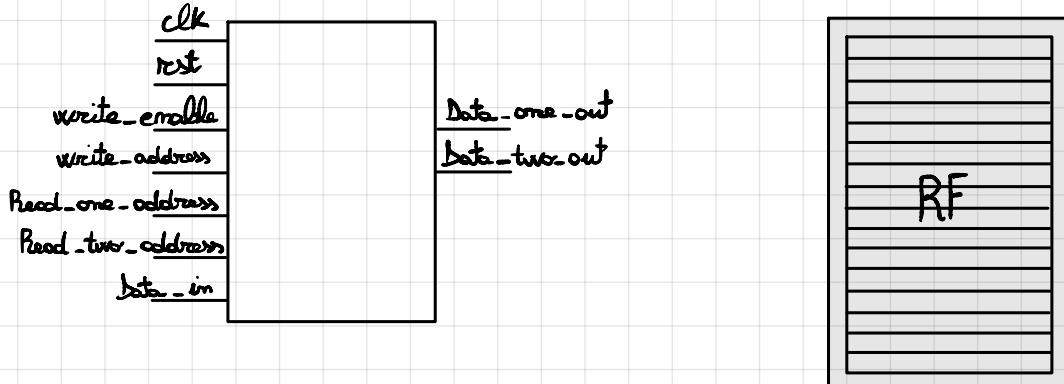


Decode unit

Block diagram



Register file (2R 1W implementation)



type Reg_array is array of vector

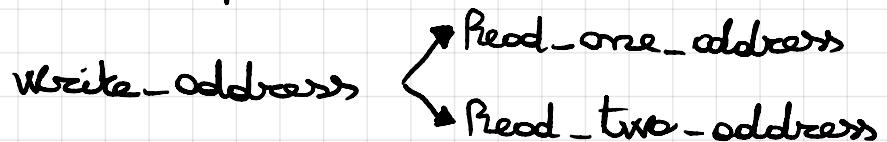
Signal Registers: Reg_array = Ø

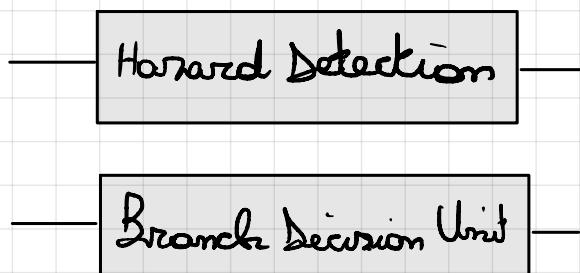
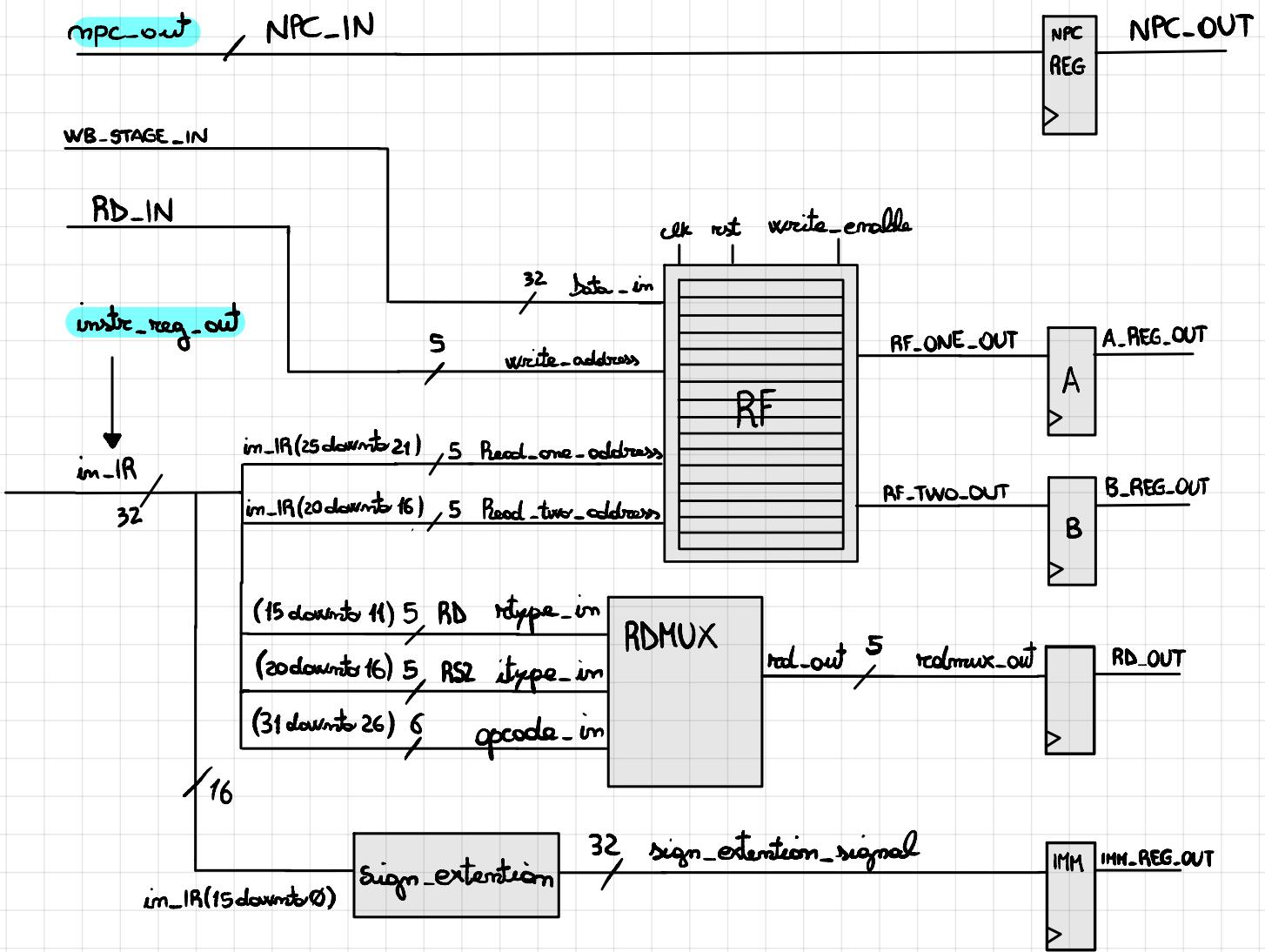
Write : (address different from Ø) and (write_enable = 1)

Read :

if (Write_enable=1) and (Read-one_address = Write_address) and (Read-two_address = Write_address)

Now we write all the possible combinations of addresses

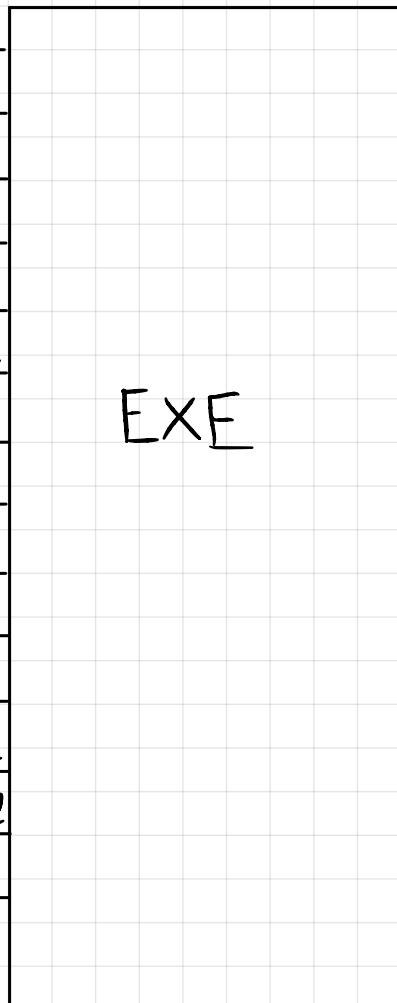




OPCODE	RS1	RS2	RDST	FUNC	
31	26 25	21 20	16 15	11 10	0

Execute write

alu_forwarding_one
mem_forwarding_one
alu_forwarding_two
mem_forwarding_two
alu_forwarding_value
mem_forwarding_value
mpc_im
a_req_im
b_req_im
imm_req_im
rd_req_im
mux_one_control
mux_two_control
alu_control



execution_stage_out

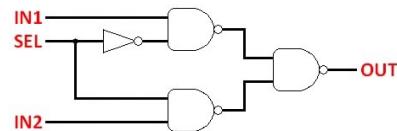
b_req_out

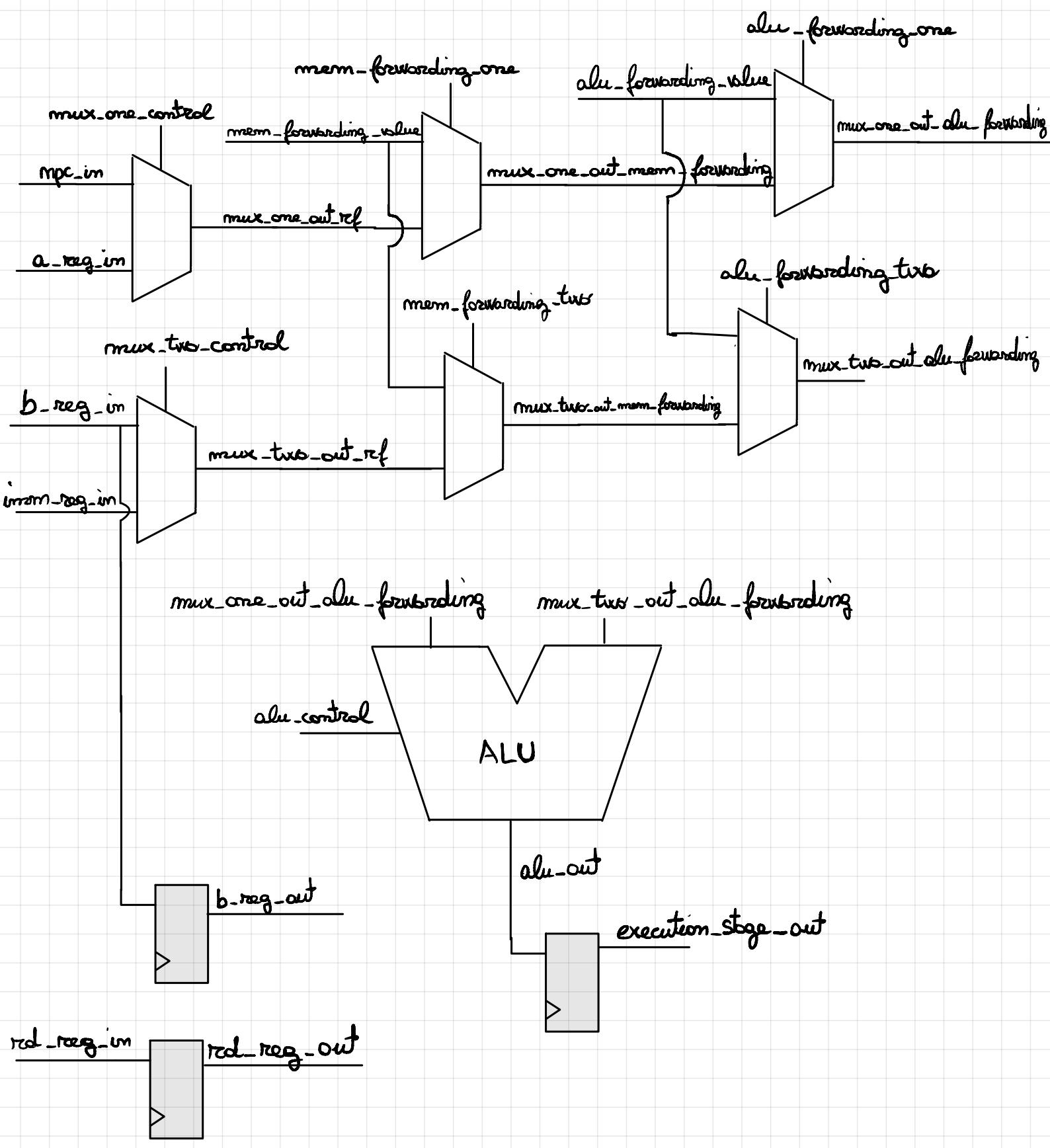
rd_req_out

Merk 21

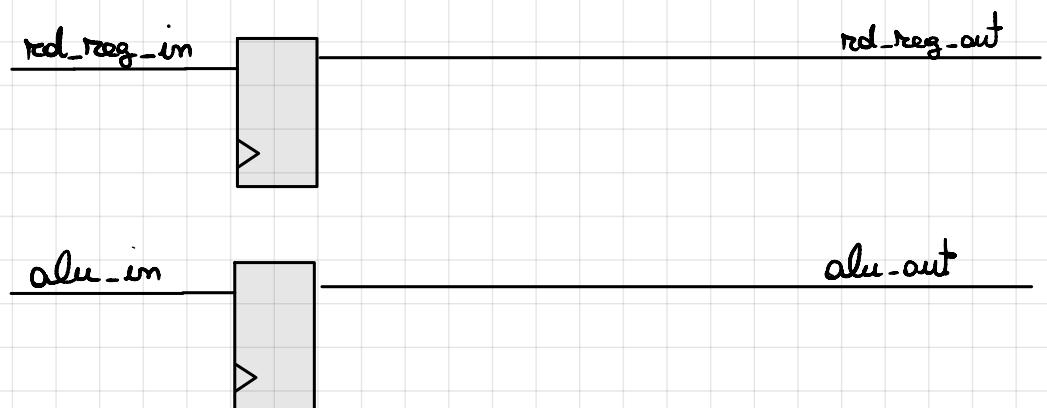
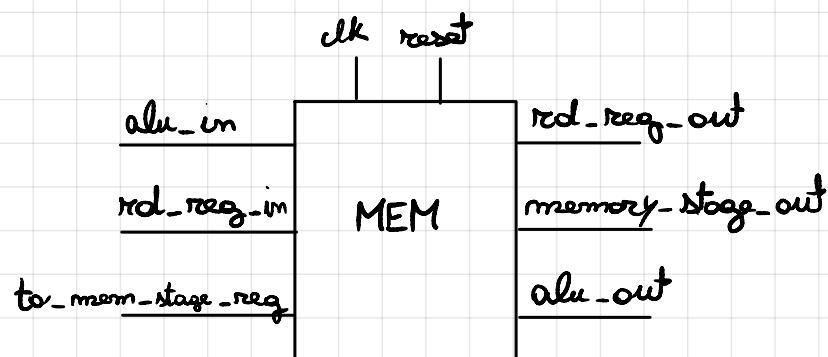
Register - generie

ALU





Memory unit

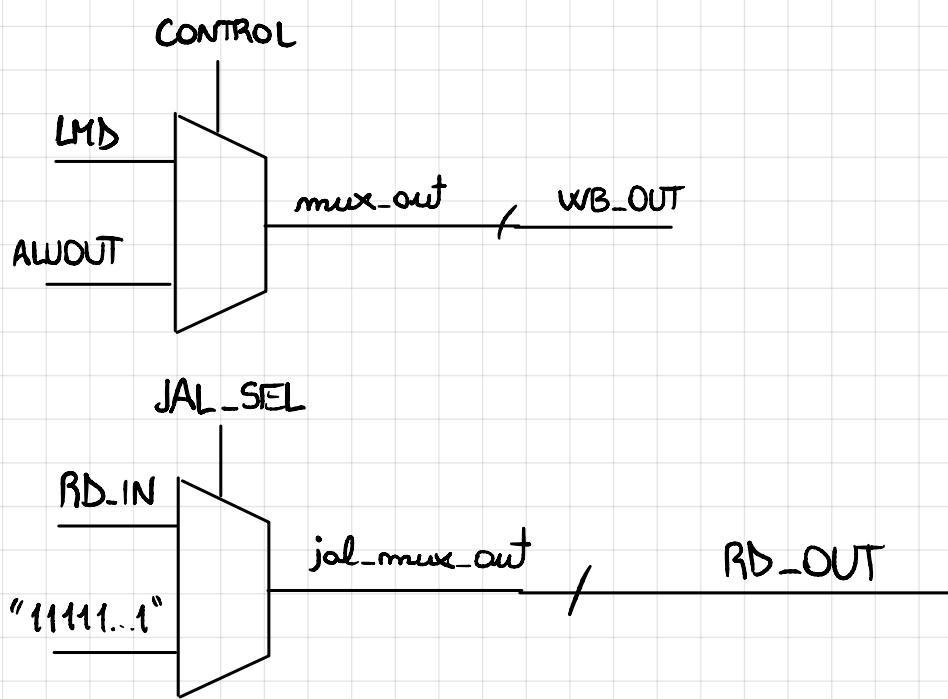
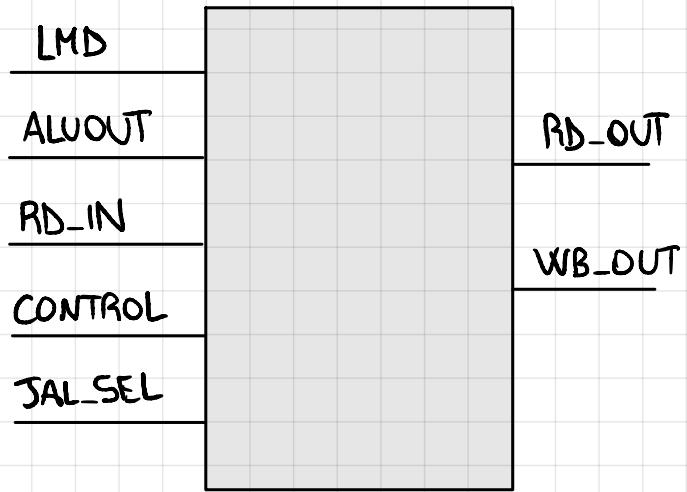


to_mem_stage_req

memory_stage_out

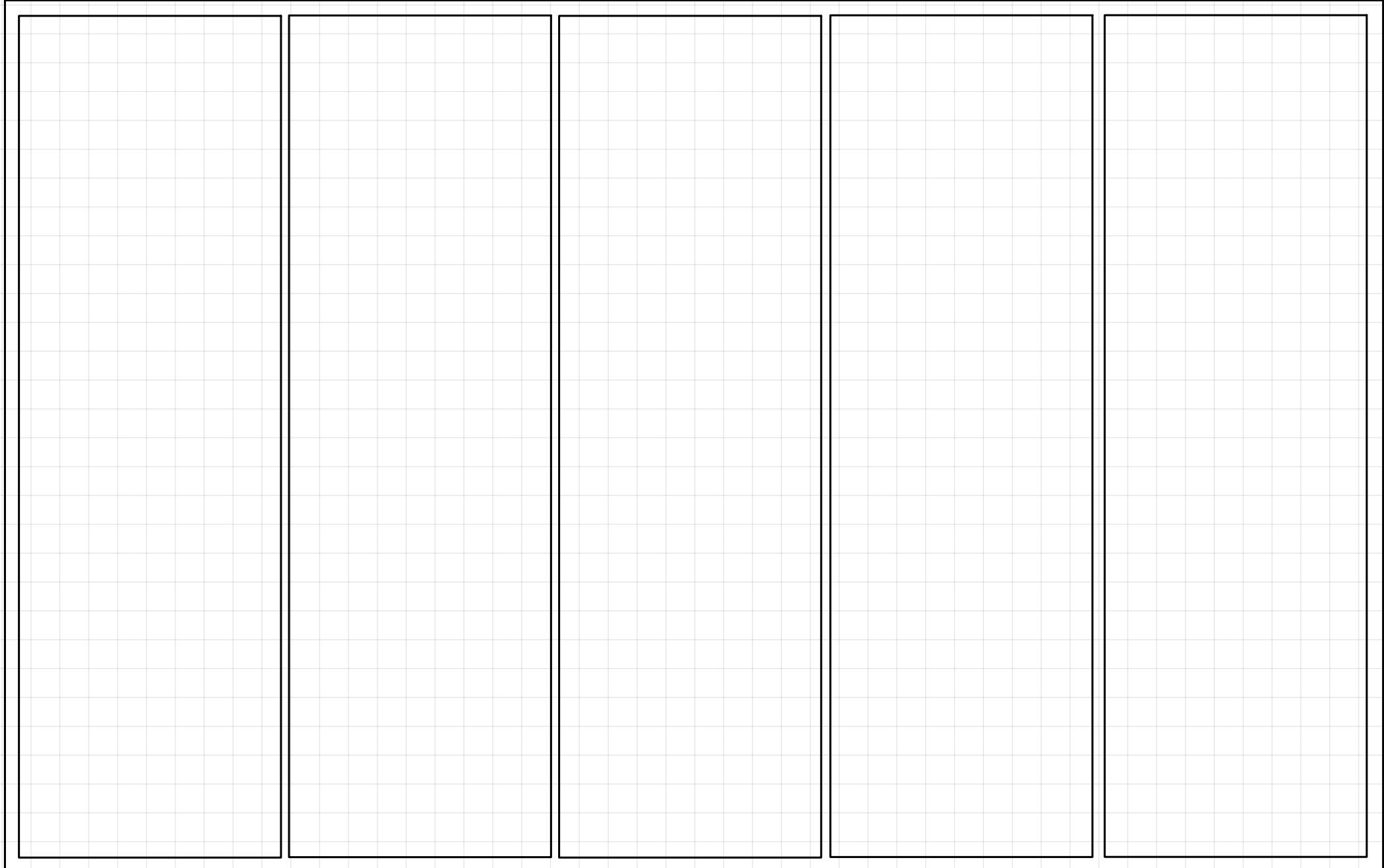


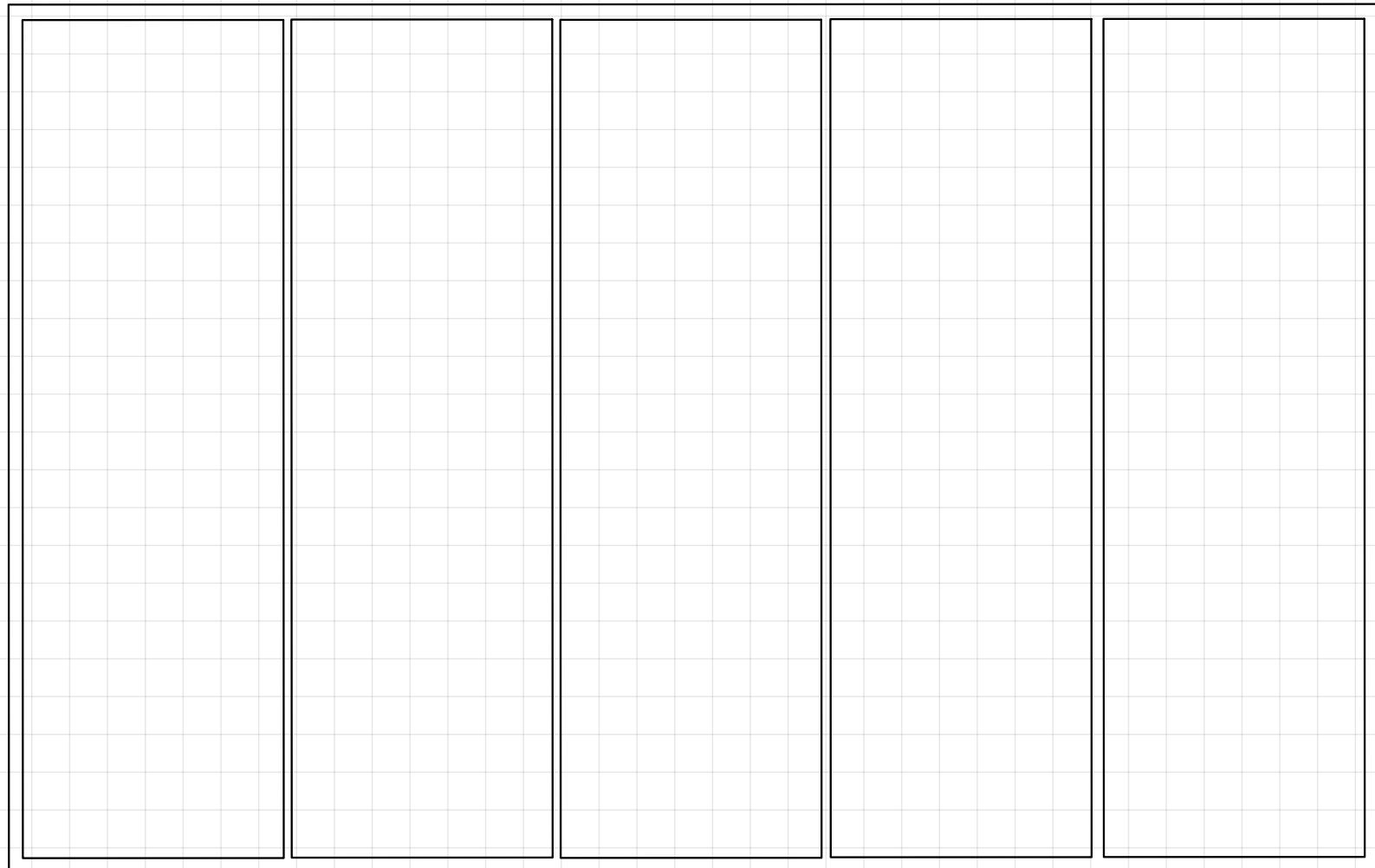
Write Back unit



Datapath

C.U.

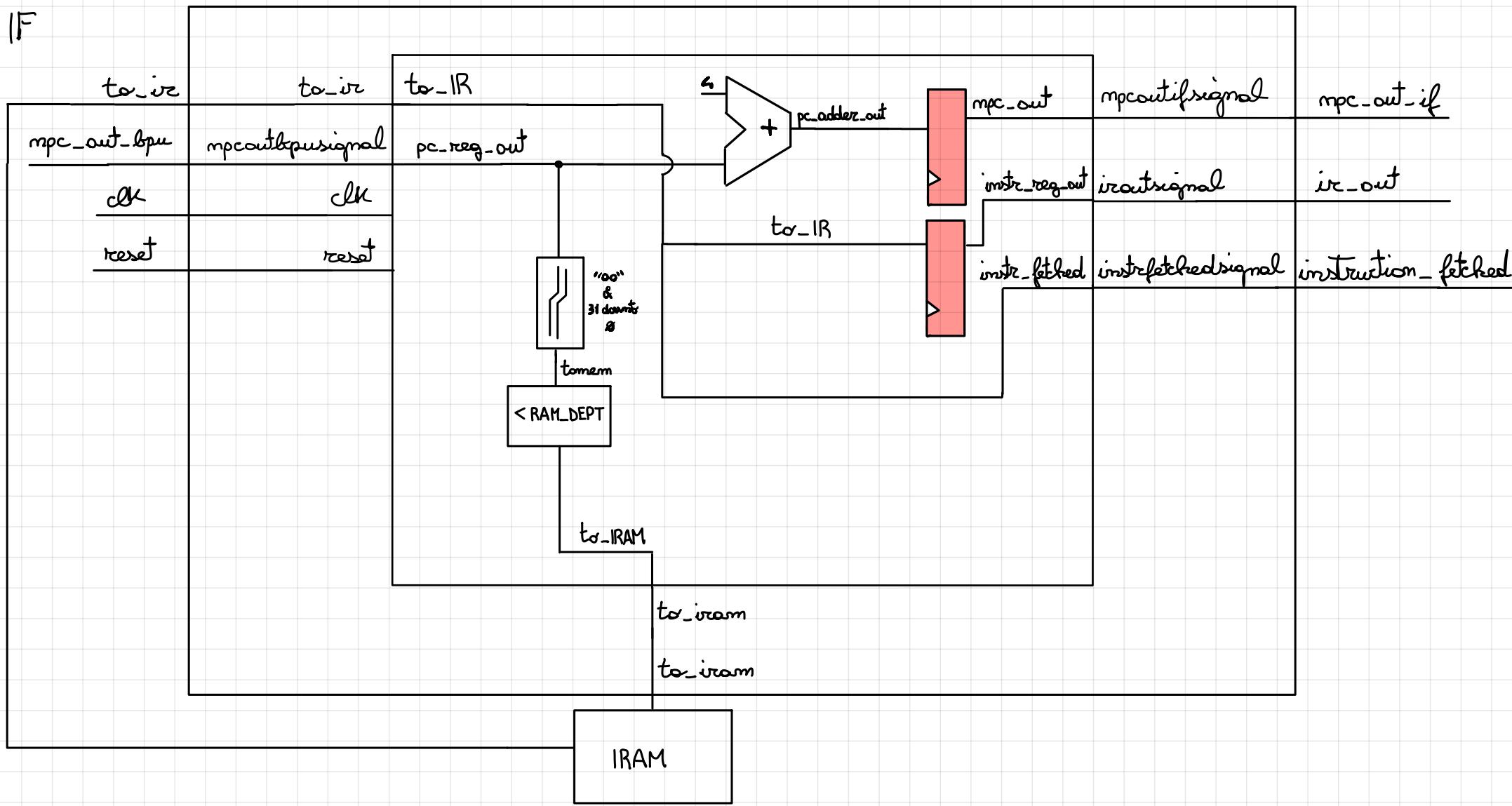




IRAM

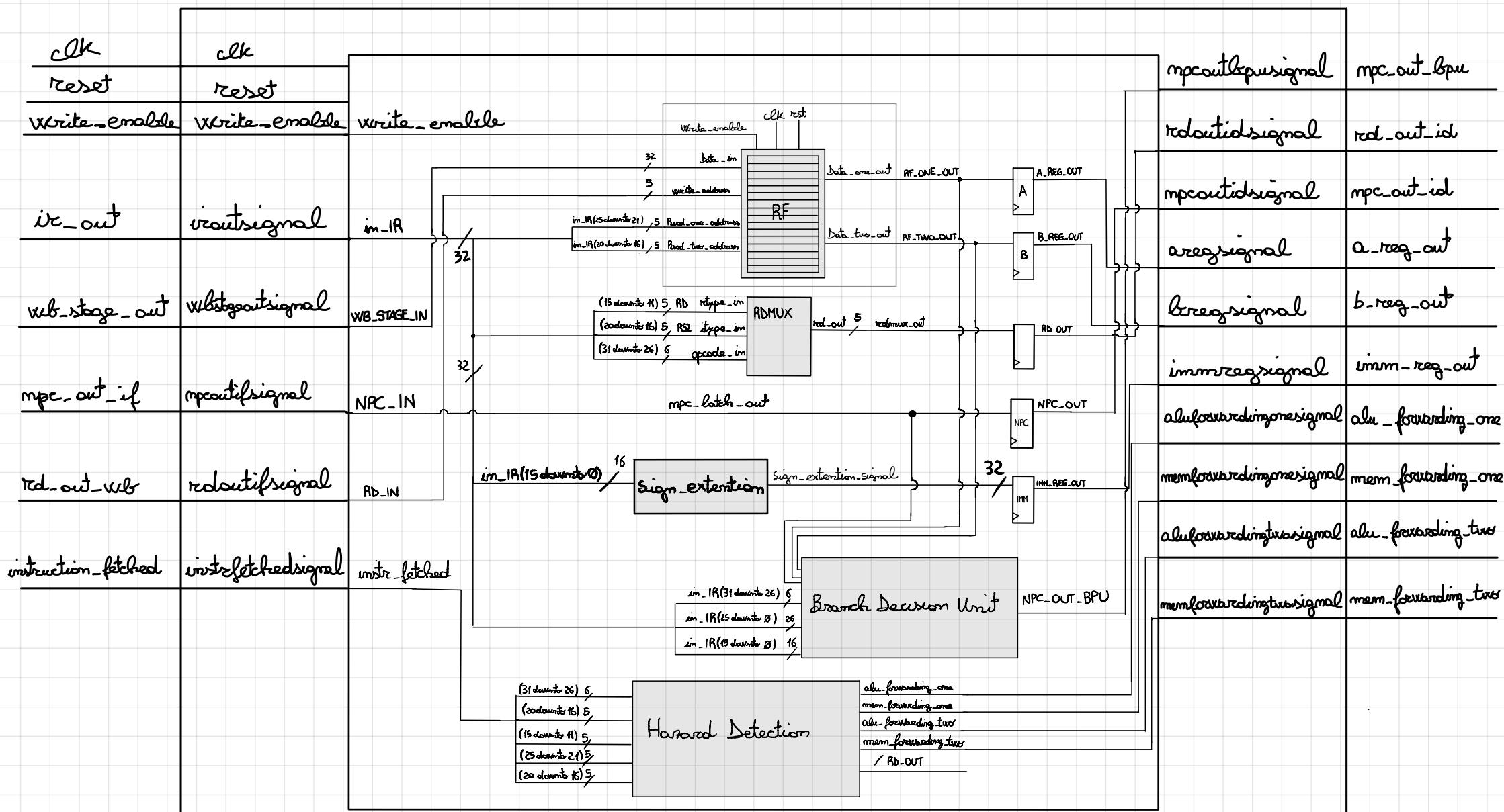
DRAM

IF



mpc_out_bp is an output for datapath.vhd, but an input for fetch_unit

ID



OPCODE	RS1	RS2	RDST	FUNC
31	26 25	21 20	16 15	11 10 0

Hazard detection

