DFM analysis report_JLCDFM

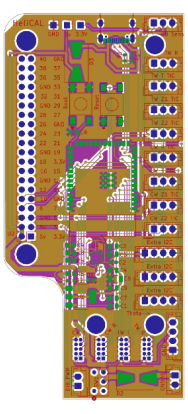
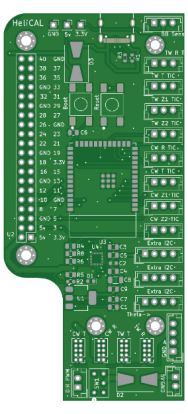
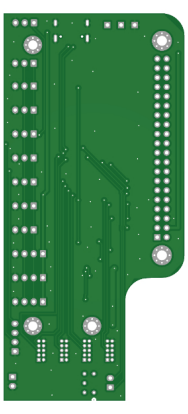
File name: **Drill Files.zip**

Report generated at: **2025-04-10 20:19:02**

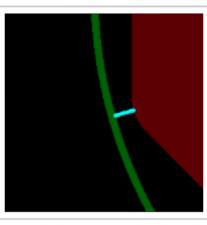
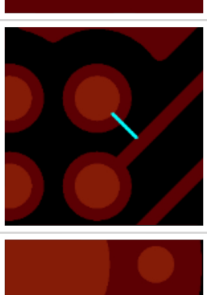
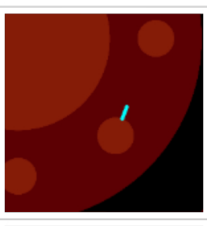
PCB layers: **2**

PCB size: **4.89x10.47cm**

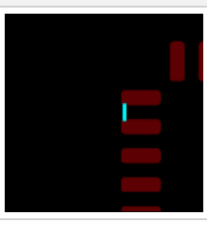
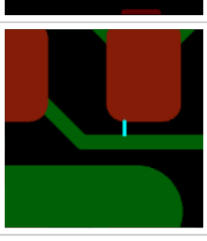
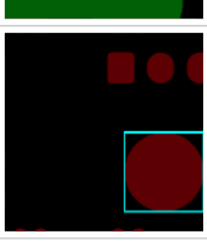
Analyze project: ☑ **PCB DFM** ☐ **SMT DFM**

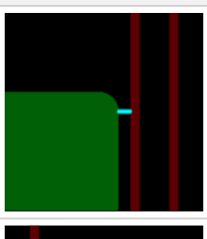
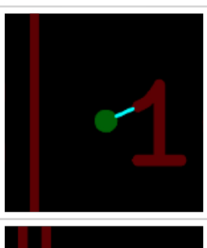
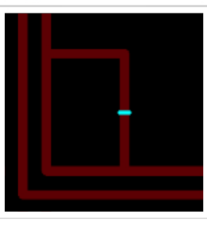
PCB DFM>Routing layer analysis

Analyze project	Analysis results	PCB screenshot	Layer distribution	Statistics
Sharp trace corner (Check for sharp corners in traces)	No	No	No	Danger: 0 Warning: 0 Good: 0
BGA pad (Check BGA pads on the board)	No	No	No	Danger: 0 Warning: 0 Good: 0
Via placed within a pad (Check if there is a via placed within a pad)	No	No	No	Danger: 0 Warning: 0 Good: 0
Trace to board edge (Detect traces too close to the board edge)	0.25mm Good		ESP32_S2_SOLO_N4 Kicad Reference Design-F_Cu.gtl	Danger: 0 Warning: 0 Good: 1
Trace spacing (Measure spacing between adjacent parallel traces)	0.18mm Good		ESP32_S2_SOLO_N4 Kicad Reference Design-B_Cu.gbl ESP32_S2_SOLO_N4 Kicad Reference Design-F_Cu.gtl	Danger: 0 Warning: 0 Good: 5
Unconnected trace end (Free-standing trace ends not connected to pads)	No	No	No	Danger: 0 Warning: 0 Good: 0
Trace width (Trace width information)	0.2mm Good		ESP32_S2_SOLO_N4 Kicad Reference Design-B_Cu.gbl ESP32_S2_SOLO_N4 Kicad Reference Design-F_Cu.gtl	Danger: 0 Warning: 0 Good: 100
Fiducial (Detect fiducial marks on the board)	No	No	No	Danger: 0 Warning: 0 Good: 0
Pad to board edge (Measure distance of pads from the board edge)	0.23mm Good		ESP32_S2_SOLO_N4 Kicad Reference Design-B_Cu.gbl ESP32_S2_SOLO_N4 Kicad Reference Design-F_Cu.gtl	Danger: 0 Warning: 0 Good: 2
Pad spacing (Measure pad to pad spacing)	0.27mm Good		ESP32_S2_SOLO_N4 Kicad Reference Design-B_Cu.gbl ESP32_S2_SOLO_N4 Kicad Reference Design-F_Cu.gtl	Danger: 0 Warning: 0 Good: 100
Plated through-hole to trace clearance (Measure clearance of plated through-holes to traces)	0.47mm Good		ESP32_S2_SOLO_N4 Kicad Reference Design-B_Cu.gbl ESP32_S2_SOLO_N4 Kicad Reference Design-F_Cu.gtl	Danger: 0 Warning: 0 Good: 11
Annular ring (Annular ring width of pads compared to holes)	0.17mm Good		ESP32_S2_SOLO_N4 Kicad Reference Design-B_Cu.gbl ESP32_S2_SOLO_N4 Kicad Reference Design-F_Cu.gtl	Danger: 0 Warning: 0 Good: 100
tht to smd (Detect clearance of vias to pads)	3.47mm Good		ESP32_S2_SOLO_N4 Kicad Reference Design-B_Cu.gbl ESP32_S2_SOLO_N4 Kicad Reference Design-F_Cu.gtl	Danger: 0 Warning: 0 Good: 60
Via to pad (Detect clearance of vias to pads)	No	No	No	Danger: 0 Warning: 0 Good: 0

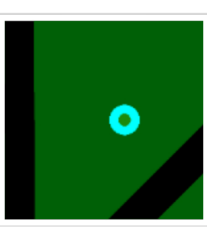
PCB DFM>Soldermask layer analysis

Analyze project	Analysis results	PCB screenshot	Layer distribution	Statistics
Soldermask bridge (Detect distance between parallel soldermask opening edges)	0.2mm Good		ESP32_S2_SOLO_N4 Kicad Reference Design-F_Mask.gts	Danger: 0 Warning: 0 Good: 20
Solder mask opening exposing trace (Detect clearance of solder mask openings to nearby traces)	0.18mm Good		ESP32_S2_SOLO_N4 Kicad Reference Design-F_Mask.gts	Danger: 0 Warning: 0 Good: 15
Soldermask opening with multiple segments (Check if solder mask openings are constructed from multiple geometric shapes)	null Warning		ESP32_S2_SOLO_N4 Kicad Reference Design-B_Mask.gbs ESP32_S2_SOLO_N4 Kicad Reference Design-F_Mask.gts	Danger: 0 Warning: 22 Good: 0
Negative soldermask expansion (Detect solder mask openings smaller than their corresponding pads)	No	No	No	Danger: 0 Warning: 0 Good: 0

PCB DFM>Silkscreen layer analysis

Analyze project	Analysis results	PCB screenshot	Layer distribution	Statistics
Silkscreen to pad (Detect clearance of silkscreen to pads)	0.15mm Warning		ESP32_S2_SOLO_N4 Kicad Reference Design-F_Silkscreen.gto	Danger: 0 Warning: 47 Good: 3
Silkscreen to hole (Detect clearance of silkscreen to holes)	0.24mm Good		ESP32_S2_SOLO_N4 Kicad Reference Design-F_Silkscreen.gto	Danger: 0 Warning: 0 Good: 3
Silkscreen line width (Check silkscreen line width)	0.12mm Warning		ESP32_S2_SOLO_N4 Kicad Reference Design-F_Silkscreen.gto	Danger: 0 Warning: 50 Good: 0

PCB DFM>Drill layer analysis

Analyze project	Analysis results	PCB screenshot	Layer distribution	Statistics
Missing plated through-hole (Detect top and bottom pads at the same location without plated through-holes)	No	No	No	Danger: 0 Warning: 0 Good: 0
Plated through-hole spacing (Measure spacing between plated through-holes)	No	No	No	Danger: 0 Warning: 0 Good: 0
Short slot detection (Detect slots shorter than twice their width)	No	No	No	Danger: 0 Warning: 0 Good: 0
Slot width check (Measure slot width)	0.6mm Danger		ESP32_S2_SOLO_N4 Kicad Reference Design-PTH.drl	Danger: 4 Warning: 0 Good: 0
Via to PTH spacing (Measure spacing of vias to plated through-holes)	No	No	No	Danger: 0 Warning: 0 Good: 0
Unconnected via (Detect isolated unconnected vias)	null Warning		ESP32_S2_SOLO_N4 Kicad Reference Design-PTH.drl	Danger: 0 Warning: 50 Good: 0