

Dineshkumar Bhaskaran

✉ dineshkumarb@gmail.com ☎ 778 893 8274 🔗 dkbhaskaran.github.io in dineshkumarb 📍 Canada (OWP)

Summary

- Expert in high-performance parallel computing, with a strong focus on algorithm parallelization, optimization, and benchmarking for AI/ML workloads, image processing pipelines, and distributed storage systems.
- Extensive experience in Linux kernel and systems programming, covering storage virtualization, device drivers, and board bring-ups for ARM-based architectures.

Experience

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| <p>Actalent, GPU Software Engineer (John Deere)</p> <ul style="list-style-type: none"> • Optimized various image processing algorithms like AutoWhiteBalance, and Blurring algorithms like Gaussian, Bilateral, Median and Homogeneous on CUDA/VPI/VPA backends, achieving 25% performance gains with CUDA, and augmented test infrastructure on ARM and porting VPI based algorithms to Ubuntu. | <p>Vancouver, Aug
2025 - Nov 2025</p> |
| <p>Arista Networks, Software Engineer</p> <ul style="list-style-type: none"> • Refactored the Layer 3 Unicast routing abstraction layer, removing approximately 7K lines of redundant code between protocol and hardware interface layers. • Unified portions of IPv4 and IPv6 handling logic using C++ templates, resulting in a cleaner codebase and 4% improvement in module build times. | <p>Vancouver, Nov
2023 - Apr 2025</p> |
| <p>AMD India, Senior Member Technical Staff</p> <ul style="list-style-type: none"> • Rapids Accelerated Data Science for ROCm: Owned and maintained RAPIDS CUDF sub-projects (i.e. rapids-cmake, RMM, NVComp) to support PyData libraries on AMD GPUs under the ROCm stack. • MLPerf Inferencing: Implemented Python reference code for models Resnet50, YOLOv4 and Bert on AMD Instinct GPUs for multiple backends like pytorch, tensorflow, Tensor virtual machine (TVM) and MIGraphX. Developed a C++ inference server on TVM for ResNet50, improving performance by 51.5%. • ROCm Clang Compiler <ul style="list-style-type: none"> - ROCm Clang compiler : Maintainer from Aug 2019 to Sept. 2021. - Implemented multithreading and in-memory compilation in AMDs Lightning compiler (based on LLVM), improving compile time by 29% on Windows and 1.07x on Linux. | <p>Bengaluru, Aug
2019 - Oct 2023</p> |
| <p>Aricent (Now Capgemini Engineering), Principal Engineer</p> <ul style="list-style-type: none"> • Accelerated Erasure Coding: Conceived and led the Accelerated Storage I/O (ECoE) library for CEPH, offloading erasure coding, encryption, and deduplication to GPUs. Responsible for ideation, budgeting, procurement, recruitment, and technical leadership. Evaluated state-of-the-art erasure code algorithms, collaborating with IISc Bangalore to integrate Minimum Storage Regenerating erasure codes. Drove client engagements through white papers, blogs, and demos, and presented results at SNIA SDC 2018 (India and Santa Clara) under the title Accelerated Erasure Coding: The New Frontiers of Software-Defined Storage. • Open Hardware: Served as technical lead for Aricents Open Hardware program, creating a modular edge platform for SDRs and 5G workloads. Designed OS and platform software from the ground up, enabling Linux bare-metal net-installs, Docker containerization of the OpenAirInterface 4G stack, and offload of FFT components to NVIDIA GPUs and Xilinx FPGA VCU1525. <ul style="list-style-type: none"> - Integrated OpenHW platform with Kubernetes and containerized applications across heterogeneous compute (CPU, GPU, FPGA, DSP). Built business collaterals, demos | <p>Bengaluru, Oct
2017 - Jul 2019</p> |

(including private 4G voice calls), and engaged in client interactions to drive adoption.

Canon Inc, Principal Engineer

Tokyo,
Bengaluru, Mar
2010 - Oct 2017

- **Canon Parallel Image processing library:** Led design and development of a parallelized medical image processing library for Canon medical apparatuses. Implemented and optimized registration algorithms (ICP, Powell, LM, GD, MI, NMI, RIU, SSD, etc.), parallelized image filtering and statistical functions, and ported modules from HLSL to OpenCL. Benchmarked and tuned for NVIDIA, AMD, and x86 platforms, achieving performance surpassing OpenCV/ITK and Canons internal libraries.
 - Managed multi-site teams in Japan and India with responsibilities spanning project planning, execution, budgeting, hiring, and training. Established test automation infrastructure and cross-team workflows that reduced release turnaround time, improved reliability, and quality.
- **Canon Embedded Linux Platform:** Led porting, enhancement, and long-term maintenance of Linux OS for Canon embedded products including surveillance cameras, projectors, and network scanners. Managed kernel bring-up on Intel Haswell, TI AM437x, Xilinx ZC-702/706, and proprietary ARM SoCs; developed and maintained cross-compiler toolchains; ensured real-time kernel support; automated testing frameworks; and streamlined processes for kernel vulnerability detection, patching, and validation.

Early Experience, Software Engineer

Bengaluru, Sep
2003 - Mar 2010

- **Brocade communications (Now Broadcom):** Contributed to storage virtualization and replication solutions as part of Brocades Storage Application Services (SAS). Owned the Virtual Initiator module, drove enhancements from SAS v2.x to v3.x, resolved critical customer issues, and supported global teams with multiple deputations to the U.S. for product coordination and next-gen platform porting.
- **Tata Elxsi:** Delivered kernel-level development across diverse domains, including DVR subsystems (stream scheduler, zero-copy I/O, disk driver optimizations) and Fibre Channel target mode drivers for LSI HBAs for CMS Japan. Implemented Linux kernel utilities, user-space configuration interfaces, and a custom kernel memory leak detector for debugging and reliability.

Education

Deep Learning Theory and Practice IISc Bengaluru

M.S Software systems 2006-2009, BITS Pilani

Bachelor of Technology, Computer Engineering 1999-2003, University of Calicut.

Technical Writing & Talks

- [Blog and Assorted articles](#)
- [Accelerated Erasure Coding](#)
- [Why erasure coding is the future of data resiliency](#)
- [Writing a Network device driver](#)

Technologies

Languages: C, C++, Python, parallel languages (HIP, OpenCL, CUDA, PTX, HLSL), and low-level (ARM/x86 asm).

Protocols stacks: storage (FC, SCSI), networking (USB), telecom (OpenAirInterface 4G).

Tools : ROCm, GNU toolchain, testing frameworks, profilers.

Hardware/SoCs: AMD/NVIDIA DCGPUs, Jetson, Xilinx, TI, Intel, Canon SoCs.