

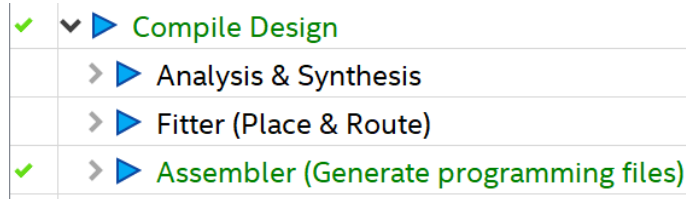
Programming the onboard configuration memory in Intel Quartus

This tutorial is made with Quartus 18.1 for windows but different versions will also work. Its written for the FPGA Board V2.1 By D. Keekstra.

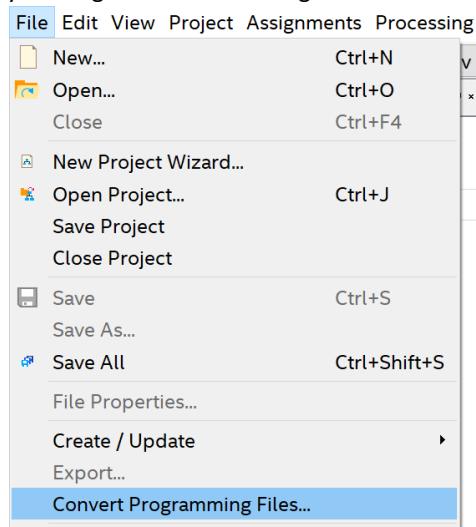
1. Preparing the program file

To program your FPGA configuration to the on the onboard memory we need to convert our SRAM object file (.sof) to an indirect configuration file (.jic).

1. Open your Quartus project in Quartus. Be sure the assembler step in Quartus has completed:



2. Open the conversion window by clicking File->Convert Program Files



3. Now the conversion window will popup. Change the values according to the letters in the list

File Tools Window Search altera.com

Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.

Conversion setup files

Open Conversion Setup Data... Save Conversion Setup...

Output programming file

Programming file type: **A** Programmer Object File (.pof)

Options/Boot info... Configuration device: **B** EPCE16 Mode: **C** 1-bit Passive Serial

File name: output_file.pof **D** ...

Advanced... Remote/Local update difference file: NONE

☒ Create Memory Map File (Generate output_file.map)
☐ Create CvP files (Generate output_file.periph.pof and output_file.core.rbf)
☐ Create config data RPD (Generate output_file_auto.rpd)

Input files to convert

File/Data area	Properties	rt Addr
Options		0x000...
SOF Data	Page_0	<auto>

Add Hex Data
Add Sof Page
Add File...
Remove
Up

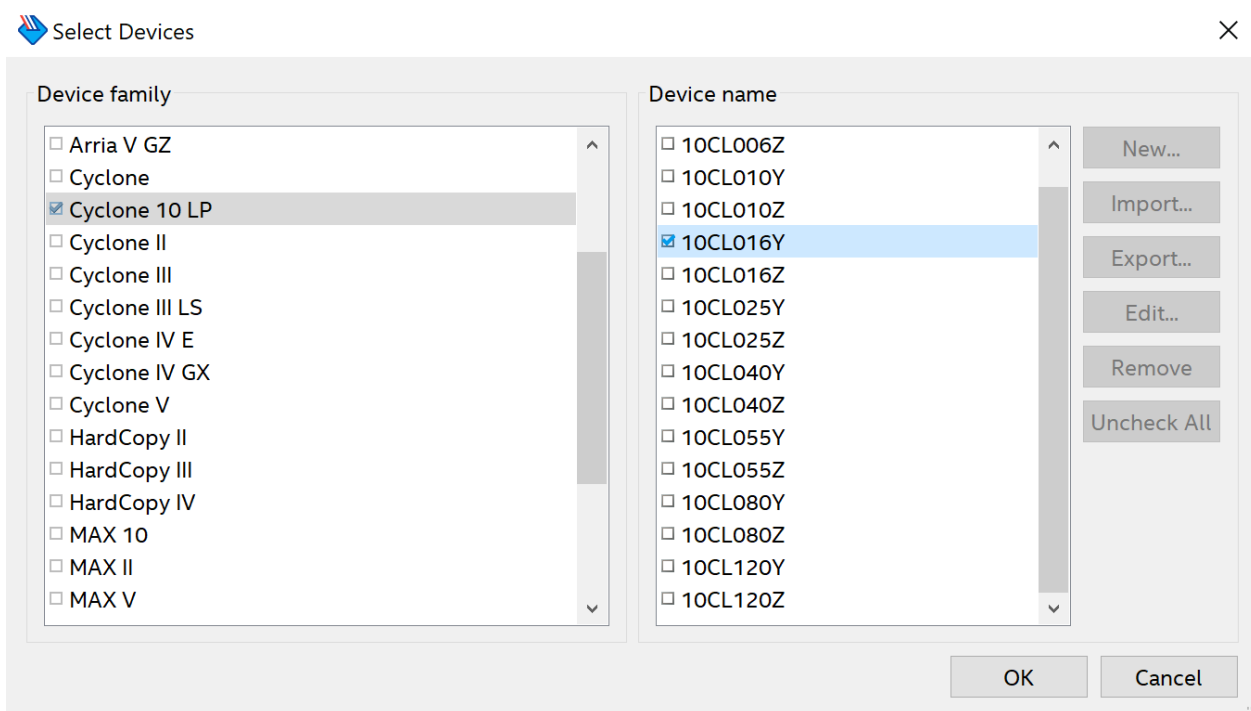
- A. Choose JTAG Indirect Configuration File (.jic)
 - B. Choose EPCS4
 - C. Choose Active Serial
 - D. Select the output directory of your project. (by default in the output_files folder of your project folder)
4. Click on the Flash Loader. Than press the button Add Device..

Input files to convert

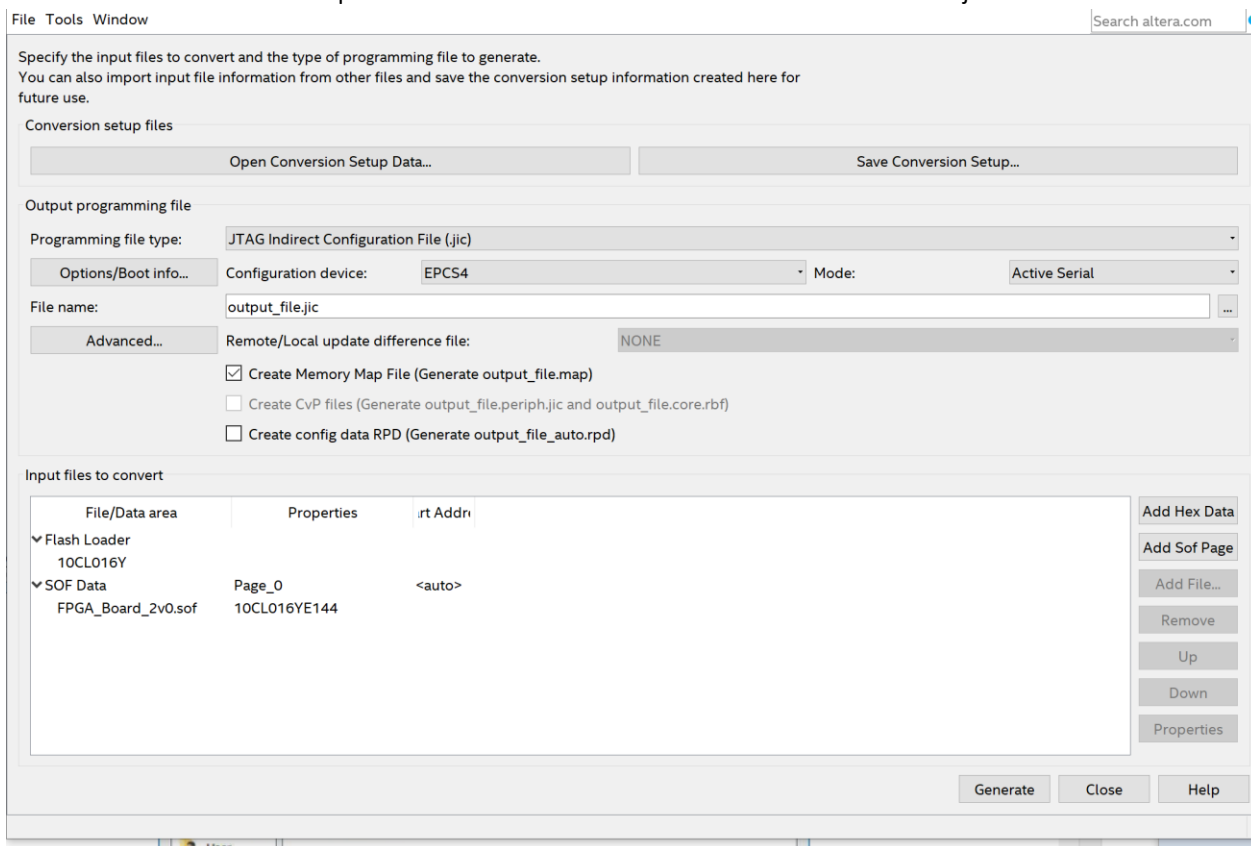
File/Data area	Properties	rt Addr
Flash Loader		
SOF Data	Page_0	<auto>

Add Hex Data
Add Sof Page
Add File...
Remove
Up
Down
Properties

5. Select from the Cyclone 10 LP family the 10CL016Y and click ok.



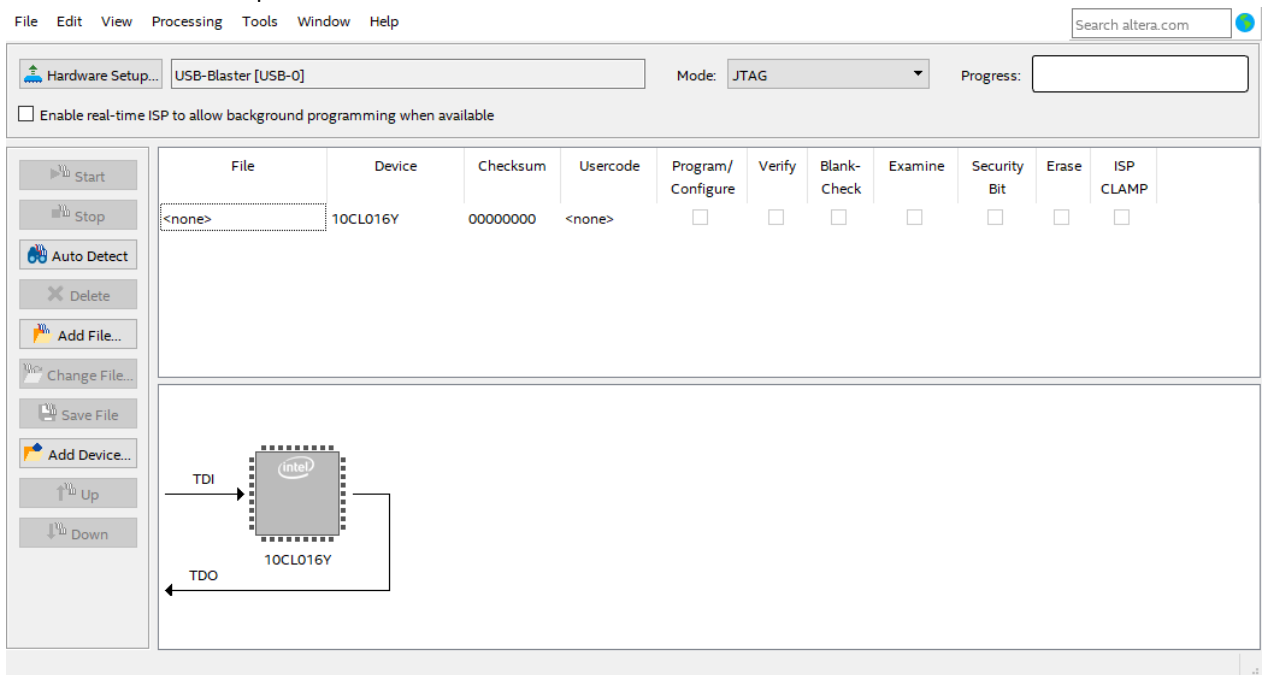
6. Click on SOF Data. Now click on add File.. Here you can select the .sof file from your project. (default in the output_files folder of your project)
7. The result should look like the picture below. When it does click Generate to create the .jic file.



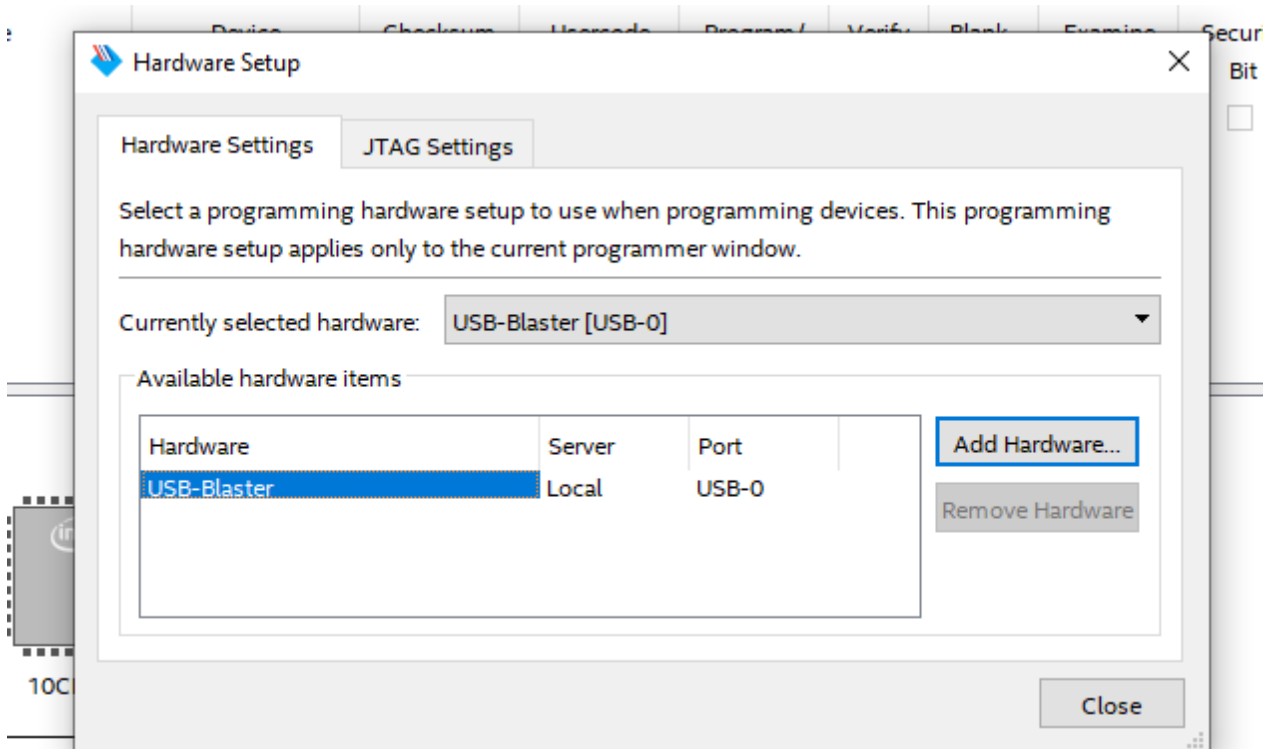
8. When you get the success message you can close the message and the window.

2. Program your device

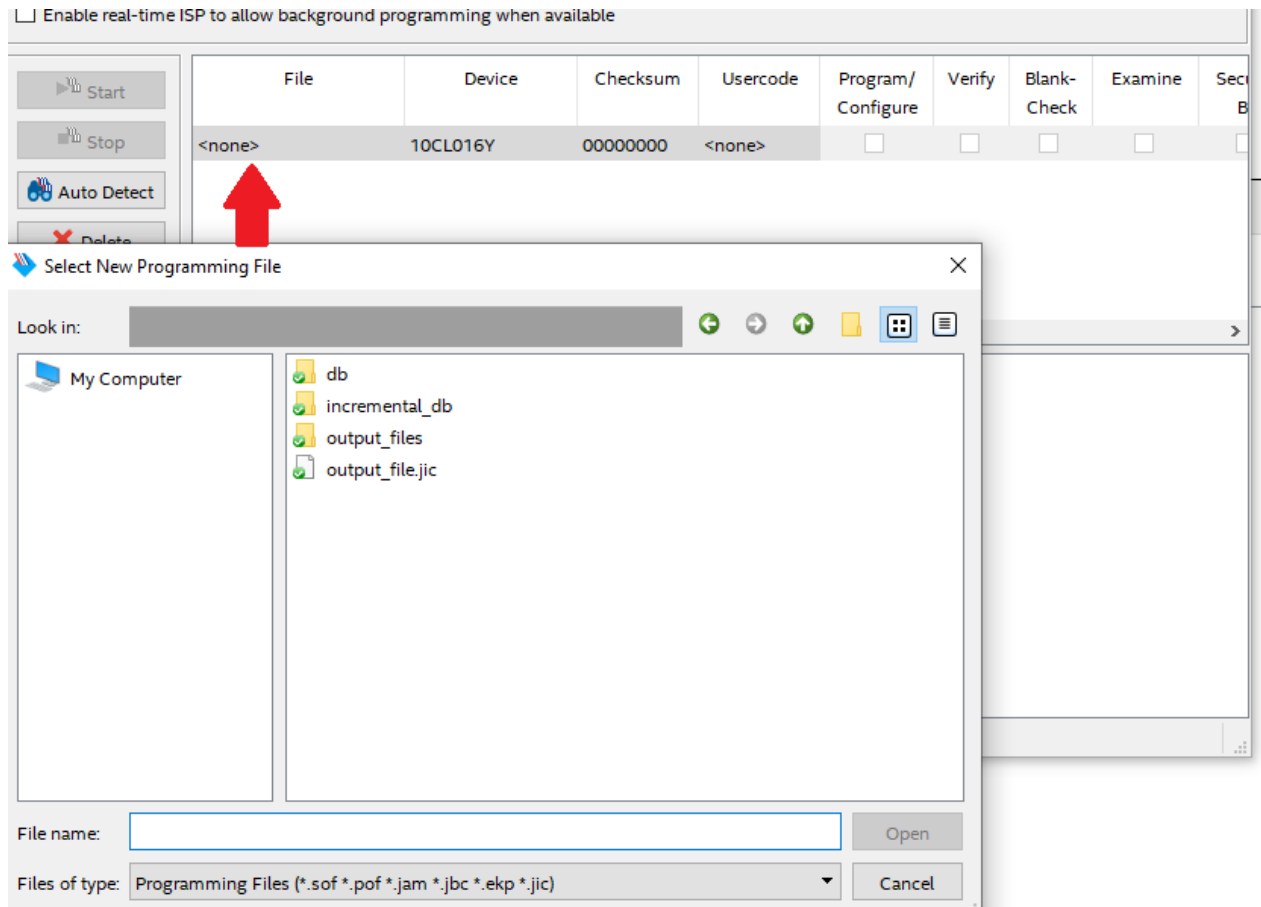
1. Open the programmer tool in the menu under Tools->Programmer
2. The next window will open:



3. When there is no USB-Blaster next to the Hardware Setup button, Click on hardware setup and dubble click the USB-Blaster and click close



- Now click the Auto detect. The USB-Blaster will detect the FPGA and you will see a screen as in the picture of step 2.
- Now Double click on the <none> row and select the generated jic file from part 1



- This will change the view and show a memory next to the FPGA:

File Edit View Processing Tools Window Help Search altera.com

Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress:

☐ Enable real-time ISP to allow background programming when available

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Sec
<none>	10CL016Y	00000000	0010F9E6	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
output_file.jic	EPCS4	0057F4F9		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	

Start Stop Auto Detect Delete Add File... Change File... Save File Add Device... Up Down

7. By selecting Program/Configure you can now press start to program your configuration memory.
8. For erasing deselect the Program/Configure checkbox and select the erase checkbox and press start.