Verilog HDL:
Leftover topics

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Outline

- Fork-join
- Race Condition
- Generate blocks

Fork Join

- Used to create parallel execution of multiple blocks
- Part of the initial or always block.
- All blocks inside fork...join run simultaneously
- Control resumes only after all parallel threads complete
- Commonly used in testbenches, simulation timing, or parallel task modeling

Fork Join

- Code inside fork...join runs in parallel
- Execution resumes after all parallel blocks finish.

```
initial begin
  fork
    // Parallel block 1
    // Parallel block 2
    // ...
  join
end
```

Example: Fork Join

```
1   module fork_join_demo;
2
3     initial begin
4       $display("Simulation starts at time = %0t", $time);
5
6       fork
7         begin
8           #5 $display(">> Task A completed at time = %0t", $time);
9         end
10
11        begin
12          #10 $display(">> Task B completed at time = %0t", $time);
13        end
14
15        begin
16          #3 $displ
17        end
18      join
19
20      $display("All
21    end
22
23  endmodule
```

```
Simulation starts at time = 0
>> Task C completed at time = 3
>> Task A completed at time = 5
>> Task B completed at time = 10
All parallel tasks done. Resuming after fork-join at time = 1
```

Example Output : Fork Join

```
1   module fork_join_demo;
2
3     initial begin
4       $display("Simulation starts at time = %0t", $time);
5
6       fork
7         begin
8           #5 $display(">> Task A completed at time = %0t", $time);
9         end
10
11        begin
12          #10 $display(">> Task B completed at time = %0t", $time);
13        end
14
15        begin
16          #3 $
17        end
18      join
19
20      $display
21    end
22
23  endmodule
```

```
Simulation starts at time = 0
>> Task C completed at time = 3
>> Task A completed at time = 5
>> Task B completed at time = 10
All parallel tasks done. Resuming after fork-join at time = 10
```

Generate Block

- Used in synthesizable Verilog to instantiate modules or logic repetitively or conditionally.
- Mainly used in RTL coding for Arrays of logic, Parameterized designs, Clean and scalable design structure
- Generate block structure
  - for-generate (loop)
  - if-generate (conditional)
  - case-generate (case-based structure)

Generate Block

- Generate loop permits one or more following to be instantiated multiple times using a for loop
  - Variable declarations
  - Modules
  - User defined primitives, gate primitives
  - Continuous assignments
  - Initial and always blocks

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For Generate Block

```
genvar i;
generate
  for (i = 0; i < 4; i = i + 1) begin : gen_loop
    my_module u (.a(in[i]), .b(out[i]));
  end
endgenerate
```

- Instantiates 4 copies of my_module with indexed connections

For Generate Block with gate level primitives

```
1   module bitwise_xor_gate #(parameter N = 8) (
2       input  wire [N-1:0] a,
3       input  wire [N-1:0] b,
4       output wire [N-1:0] y
5   );
6
7   genvar i;
8   generate
9       for (i = 0; i < N; i = i + 1) begin : xor_loop
10          xor (y[i], a[i], b[i]);
11      end
12  endgenerate
13
14  endmodule
```

For Generate Block with assign

```
1  module bitwise_xor #(parameter N = 8) (
2      input  wire [N-1:0] a,
3      input  wire [N-1:0] b,
4      output wire [N-1:0] y
5  );
6
7  genvar i;
8  generate
9      for (i = 0; i < N; i = i + 1) begin : xor_gen
10         assign y[i] = a[i] ^ b[i];
11     end
12 endgenerate
13
14 endmodule
```

For Generate Block with always

```
1  module bitwise_xor #(parameter N = 8) (
2      input  wire [N-1:0] a,
3      input  wire [N-1:0] b,
4      output reg  [N-1:0] y
5  );
6
7  genvar i;
8  generate
9      for (i = 0; i < N; i = i + 1) begin : xor_gen
10         always @(*) begin
11             y[i] = a[i] ^ b[i];
12         end
13     end
14 endgenerate
15
16 endmodule
```

Example : Full Adder

```verilog
module full_adder (
    input  a,
    input  b,
    input  cin,
    output sum,
    output cout
);

wire axorb, aandb, aandcin, bandcin;

// sum = a ^ b ^ cin
xor (axorb, a, b);
xor (sum, axorb, cin);

// cout = (a & b) | (a & cin) | (b & cin)
and (aandb, a, b);
and (aandcin, a, cin);
and (bandcin, b, cin);
or  (cout, aandb, aandcin, bandcin);
```

```verilog
module ripple_carry_adder #(parameter N = 4)(
    input  [N-1:0] a,
    input  [N-1:0] b,
    input          cin,
    output [N-1:0] sum,
    output         cout
);
wire [N:0] carry;
assign carry[0] = cin;
genvar i;
generate
    for (i = 0; i < N; i = i + 1) begin : rca_stage
        full_adder fa (
            .a(a[i]),
            .b(b[i]),
            .cin(carry[i]),
            .sum(sum[i]),
            .cout(carry[i+1])
        );
    end
endgenerate
assign cout = carry[N];
endmodule
```

IF Generate Block (Conditional Instantiation)

```
generate
  if (MODE == 1) begin : gen_mode1
    // logic for mode 1
  end else begin : gen_mode0
    // logic for mode 0
  end
endgenerate
```

- Very useful for selecting implementations based on parameters

IF Generate Block (Conditional Instantiation)

```
1   module simple_if_generate #(
2       parameter USE_AND = 1  // Set to 1 for AND, 0 for OR
3   )(
4       input wire a,
5       input wire b,
6       output wire y
7   );
8
9   // Conditional logic using if-generate
10  generate
11      if (USE_AND) begin : and_block
12          assign y = a & b;
13      end else begin : or_block
14          assign y = a | b;
15      end
16  endgenerate
17
18  endmodule
```

Case-Generate (Select Instantiation)

```
generate
  case (DATA_WIDTH)
    8: begin : gen8
      // logic for 8-bit
    end
    16: begin : gen16
      // logic for 16-bit
    end
    default: begin : gen_default
      // default logic
    end
  endcase
endgenerate
```

- Useful in flexible bus-width or multi-mode designs

Case-Generate (Select Instantiation)

```
1   module generate_case_example #(
2       parameter MODE = 0  // Selects the operation: 0 = AND, 1 = OR, 2 = XOR)
3       (input wire a,
4       input wire b,
5       output wire y
6   );
7   generate
8       case (MODE)
9           0: begin : and_block
10              assign y = a & b;
11          end
12          1: begin : or_block
13              assign y = a | b;
14          end
15          2: begin : xor_block
16              assign y = a ^ b;
17          end
18          default: begin : default_block
19              assign y = 1'b0; // Default output
20          end
21      endcase
22  endgenerate
23  endmodule
```

Thank you !

Happy Learning