0229 ; -----------------------

0229 ; THE 'MAIN DISPLAY' LOOP

0229 ; -----------------------

0229 ; This routine is executed once for every frame displayed.

0229

0229 ;; DISPLAY-1

0229 2A 34 40 L0229: LD HL,($4034) ; fetch two-byte system variable FRAMES.

022C 2B DEC HL ; decrement frames counter.

022D

022D ;; DISPLAY-P

022D 3E 7F L022D: LD A,$7F ; prepare a mask

022F A4 AND H ; pick up bits 6-0 of H.

0230 B5 OR L ; and any bits of L.

0231 7C LD A,H ; reload A with all bits of H for PAUSE test.

0232

0232 ; Note both branches must take the same time.

0232

0232 20 03 JR NZ,L0237 ; (12/7) forward if bits 14-0 are not zero

0234 ; to ANOTHER

0234

0234 17 RLA ; (4) test bit 15 of FRAMES.

0235 18 02 JR L0239 ; (12) forward with result to OVER-NC

0237

0237 ; ---

0237

0237 ;; ANOTHER

0237 46 L0237: LD B,(HL) ; (7) Note. Harmless Nonsensical Timing weight.

0238 37 SCF ; (4) Set Carry Flag.

0239

0239 ; Note. the branch to here takes either (12)(7)(4) cyles or (7)(4)(12) cycles.

0239

0239 ;; OVER-NC

0239 67 L0239: LD H,A ; (4) set H to zero

023A 22 34 40 LD ($4034),HL ; (16) update system variable FRAMES

023D D0 RET NC ; (11/5) return if FRAMES is in use by PAUSE

023E ; command.

023E

023E ;; DISPLAY-2

023E CD BB 02 L023E: CALL L02BB ; routine KEYBOARD gets the key row in H and

0241 ; the column in L. Reading the ports also starts

0241 ; the TV frame synchronization pulse. (VSYNC)

0241

0241 ED 4B 25 40 LD BC,($4025) ; fetch the last key values read from LAST\_K

0245 22 25 40 LD ($4025),HL ; update LAST\_K with new values.

0248

0248 78 LD A,B ; load A with previous column - will be $FF if

0249 ; there was no key.

0249 C6 02 ADD A,$02 ; adding two will set carry if no previous key.

024B

024B ED 42 SBC HL,BC ; subtract with the carry the two key values.

024D

024D ; If the same key value has been returned twice then HL will be zero.

024D

024D 3A 27 40 LD A,($4027) ; fetch system variable DEBOUNCE

0250 B4 OR H ; and OR with both bytes of the difference

0251 B5 OR L ; setting the zero flag for the upcoming branch.

0252

0252 58 LD E,B ; transfer the column value to E

0253 06 0B LD B,$0B ; and load B with eleven

0255

0255 21 3B 40 LD HL,$403B ; address system variable CDFLAG

0258 CB 86 RES 0,(HL) ; reset the rightmost bit of CDFLAG

025A 20 08 JR NZ,L0264 ; skip forward if debounce/diff >0 to NO-KEY

025C

025C CB 7E BIT 7,(HL) ; test compute and display bit of CDFLAG

025E CB C6 SET 0,(HL) ; set the rightmost bit of CDFLAG.

0260 C8 RET Z ; return if bit 7 indicated fast mode.

0261

0261 05 DEC B ; (4) decrement the counter.

0262 00 NOP ; (4) Timing - 4 clock cycles. ??

0263 37 SCF ; (4) Set Carry Flag

0264

0264 ;; NO-KEY

0264 21 27 40 L0264: LD HL,$4027 ; sv DEBOUNCE

0267 3F CCF ; Complement Carry Flag

0268 CB 10 RL B ; rotate left B picking up carry

026A ; C<-76543210<-C

026A

026A ;; LOOP-B

026A 10 FE L026A: DJNZ L026A ; self-loop while B>0 to LOOP-B

026C

026C 46 LD B,(HL) ; fetch value of DEBOUNCE to B

026D 7B LD A,E ; transfer column value

026E FE FE CP $FE ;

0270 9F SBC A,A ;

0271 06 1F LD B,$1F ;

0273 B6 OR (HL) ;

0274 A0 AND B ;

0275 1F RRA ;

0276 77 LD (HL),A ;

0277

0277 D3 FF OUT ($FF),A ; end the TV frame synchronization pulse.

0279

0279 2A 0C 40 LD HL,($400C) ; (12) set HL to the Display File from D\_FILE

027C CB FC SET 7,H ; (8) set bit 15 to address the echo display.

027E

027E CD 92 02 CALL L0292 ; (17) routine DISPLAY-3 displays the top set

0281 ; of blank lines.

0281

0281 ; ---------------------

0281 ; THE 'VIDEO-1' ROUTINE

0281 ; ---------------------

0281

0281 ;; R-IX-1

0281 ED 5F L0281: LD A,R ; (9) Harmless Nonsensical Timing or something

0283 ; very clever?

0283 01 01 19 LD BC,$1901 ; (10) 25 lines, 1 scanline in first.

0286 3E F5 LD A,$F5 ; (7) This value will be loaded into R and

0288 ; ensures that the cycle starts at the right

0288 ; part of the display - after 32nd character

0288 ; position.

0288

0288 CD B5 02 CALL L02B5 ; (17) routine DISPLAY-5 completes the current

028B ; blank line and then generates the display of

028B ; the live picture using INT interrupts

028B ; The final interrupt returns to the next

028B ; address.

028B

028B 2B L028B: DEC HL ; point HL to the last NEWLINE/HALT.

028C

028C CD 92 02 CALL L0292 ; routine DISPLAY-3 displays the bottom set of

028F ; blank lines.

028F

028F ; ---

028F

028F ;; R-IX-2

028F C3 29 02 L028F: JP L0229 ; JUMP back to DISPLAY-1

0292

0292 ; ---------------------------------

0292 ; THE 'DISPLAY BLANK LINES' ROUTINE

0292 ; ---------------------------------

0292 ; This subroutine is called twice (see above) to generate first the blank

0292 ; lines at the top of the television display and then the blank lines at the

0292 ; bottom of the display.

0292

0292 ;; DISPLAY-3

0292 DD E1 L0292: POP IX ; pop the return address to IX register.

0294 ; will be either L0281 or L028F - see above.

0294

0294 FD 4E 28 LD C,(IY+$28) ; load C with value of system constant MARGIN.

0297 FD CB 3B 7E BIT 7,(IY+$3B) ; test CDFLAG for compute and display.

029B 28 0C JR Z,L02A9 ; forward, with FAST mode, to DISPLAY-4

029D

029D 79 LD A,C ; move MARGIN to A - 31d or 55d.

029E ED 44 NEG ; Negate

02A0 3C INC A ;

02A1 08 EX AF,AF' ; place negative count of blank lines in A'

02A2

02A2 D3 FE OUT ($FE),A ; enable the NMI generator.

02A4

02A4 E1 POP HL ; \*\*\*\*

02A5 D1 POP DE ; \*\*\*

02A6 C1 POP BC ; \*\*

02A7 F1 POP AF ; \* Restore Main Registers

02A8

02A8 C9 RET ; return - end of interrupt. Return is to

02A9 ; user's program - BASIC or machine code.

02A9 ; which will be interrupted by every NMI.

02A9

02A9 ; ------------------------

02A9 ; THE 'FAST MODE' ROUTINES

02A9 ; ------------------------

02A9

02A9 ;; DISPLAY-4

02A9 3E FC L02A9: LD A,$FC ; (7) load A with first R delay value

02AB 06 01 LD B,$01 ; (7) one row only.

02AD

02AD CD B5 02 CALL L02B5 ; (17) routine DISPLAY-5

02B0

02B0 2B DEC HL ; (6) point back to the HALT.

02B1 E3 EX (SP),HL ; (19) Harmless Nonsensical Timing if paired.

02B2 E3 EX (SP),HL ; (19) Harmless Nonsensical Timing.

02B3 DD E9 JP (IX) ; (8) to L0281 or L028F

02B5

02B5 ; --------------------------

02B5 ; THE 'DISPLAY-5' SUBROUTINE

02B5 ; --------------------------

02B5 ; This subroutine is called from SLOW mode and FAST mode to generate the

02B5 ; central TV picture. With SLOW mode the R register is incremented, with

02B5 ; each instruction, to $F7 by the time it completes. With fast mode, the

02B5 ; final R value will be $FF and an interrupt will occur as soon as the

02B5 ; Program Counter reaches the HALT. (24 clock cycles)

02B5

02B5 ;; DISPLAY-5

02B5 ED 4F L02B5: LD R,A ; (9) Load R from A. R = slow: $F5 fast: $FC

02B7 3E DD LD A,$DD ; (7) load future R value. $F6 $FD

02B9 FB EI ; (4) Enable Interrupts $F7 $FE

02BA

02BA E9 JP (HL) ; (4) jump to the echo display. $F8 $FF

0038 ; -----------------------

0038 ; THE 'INTERRUPT' RESTART

0038 ; -----------------------

0038 ; The Mode 1 Interrupt routine is concerned solely with generating the central

0038 ; television picture.

0038 ; On the ZX81 interrupts are enabled only during the interrupt routine,

0038 ; although the interrupt

0038 ; This Interrupt Service Routine automatically disables interrupts at the

0038 ; outset and the last interrupt in a cascade exits before the interrupts are

0038 ; enabled.

0038 ; There is no DI instruction in the ZX81 ROM.

0038 ; An maskable interrupt is triggered when bit 6 of the Z80's Refresh register

0038 ; changes from set to reset.

0038 ; The Z80 will always be executing a HALT (NEWLINE) when the interrupt occurs.

0038 ; A HALT instruction repeatedly executes NOPS but the seven lower bits

0038 ; of the Refresh register are incremented each time as they are when any

0038 ; simple instruction is executed. (The lower 7 bits are incremented twice for

0038 ; a prefixed instruction)

0038 ; This is controlled by the Sinclair Computer Logic Chip - manufactured from

0038 ; a Ferranti Uncommitted Logic Array.

0038 ;

0038 ; When a Mode 1 Interrupt occurs the Program Counter, which is the address in

0038 ; the upper echo display following the NEWLINE/HALT instruction, goes on the

0038 ; machine stack. 193 interrupts are required to generate the last part of

0038 ; the 56th border line and then the 192 lines of the central TV picture and,

0038 ; although each interrupt interrupts the previous one, there are no stack

0038 ; problems as the 'return address' is discarded each time.

0038 ;

0038 ; The scan line counter in C counts down from 8 to 1 within the generation of

0038 ; each text line. For the first interrupt in a cascade the initial value of

0038 ; C is set to 1 for the last border line.

0038 ; Timing is of the utmost importance as the RH border, horizontal retrace

0038 ; and LH border are mostly generated in the 58 clock cycles this routine

0038 ; takes .

0038

0038 ;; INTERRUPT

0038 0D L0038: DEC C ; (4) decrement C - the scan line counter.

0039 C2 45 00 JP NZ,L0045 ; (10/10) JUMP forward if not zero to SCAN-LINE

003C

003C E1 POP HL ; (10) point to start of next row in display

003D ; file.

003D

003D 05 DEC B ; (4) decrement the row counter. (4)

003E C8 RET Z ; (11/5) return when picture complete to L028B

003F ; with interrupts disabled.

003F

003F CB D9 SET 3,C ; (8) Load the scan line counter with eight.

0041 ; Note. LD C,$08 is 7 clock cycles which

0041 ; is way too fast.

0041

0041 ; ->

0041

0041 ;; WAIT-INT

0041 ED 4F L0041: LD R,A ; (9) Load R with initial rising value $DD.

0043

0043 FB EI ; (4) Enable Interrupts. [ R is now $DE ].

0044

0044 E9 JP (HL) ; (4) jump to the echo display file in upper

0045 ; memory and execute characters $00 - $3F

0045 ; as NOP instructions. The video hardware

0045 ; is able to read these characters and,

0045 ; with the I register is able to convert

0045 ; the character bitmaps in this ROM into a

0045 ; line of bytes. Eventually the NEWLINE/HALT

0045 ; will be encountered before R reaches $FF.

0045 ; It is however the transition from $FF to

0045 ; $80 that triggers the next interrupt.

0045 ; [ The Refresh register is now $DF ]

0066 ; ------------------------------------

0066 ; THE 'NON MASKABLE INTERRUPT' ROUTINE

0066 ; ------------------------------------

0066 ; with a steady display. Note that the AF' register is reserved for this

0066 ; function and its interaction with the display routines. When counting

0066 ; TV lines, the NMI makes no use of the main registers.

0066 ; The circuitry for the NMI generator is contained within the SCL (Sinclair

0066 ; Computer Logic) chip.

0066 ; ( It takes 32 clock cycles while incrementing towards zero ).

0066 ;; NMI

0066 08 L0066: EX AF,AF' ; (4) switch in the NMI's copy of the

0067 ; accumulator.

0067 3C INC A ; (4) increment.

0068 FA 6D 00 JP M,L006D ; (10/10) jump, if minus, to NMI-RET as this is

006B ; part of a test to see if the NMI

006B ; generation is working or an intermediate

006B ; value for the ascending negated blank

006B ; line counter.

006B

006B 28 02 JR Z,L006F ; (12) forward to NMI-CONT

006D ; when line count has incremented to zero.

006D

006D ; Note. the synchronizing NMI when A increments from zero to one takes this

006D ; 7 clock cycle route making 39 clock cycles in all.

006D

006D ;; NMI-RET

006D 08 L006D: EX AF,AF' ; (4) switch out the incremented line counter

006E ; or test result $80

006E C9 RET ; (10) return to User application for a while.

006F

006F ; ---

006F ; This branch is taken when the 55 (or 31) lines have been drawn.

006F

006F ;; NMI-CONT

006F 08 L006F: EX AF,AF' ; (4) restore the main accumulator.

0070

0070 F5 PUSH AF ; (11) \* Save Main Registers

0071 C5 PUSH BC ; (11) \*\*

0072 D5 PUSH DE ; (11) \*\*\*

0073 E5 PUSH HL ; (11) \*\*\*\*

0074

0074 ; the next set-up procedure is only really applicable when the top set of

0074 ; blank lines have been generated.

0074

0074 2A 0C 40 LD HL,($400C) ; (16) fetch start of Display File from D\_FILE

0077 ; points to the HALT at beginning.

0077 CB FC SET 7,H ; (8) point to upper 32K 'echo display file'

0079

0079 76 HALT ; (1) HALT synchronizes with NMI.

007A ; Used with special hardware connected to the

007A ; Z80 HALT and WAIT lines to take 1 clock cycle.

007A

007A ; ----------------------------------------------------------------------------

007A ; the NMI has been generated - start counting. The cathode ray is at the RH

007A ; side of the TV.

007A ; First the NMI servicing, similar to CALL = 17 clock cycles.

007A ; Then the time taken by the NMI for zero-to-one path = 39 cycles

007A ; The HALT above = 01 cycles.

007A ; The two instructions below = 19 cycles.

007A ; The code at L0281 up to and including the CALL = 43 cycles.

007A ; The Called routine at L02B5 = 24 cycles.

007A ; -------------------------------------- ---

007A ; Total Z80 instructions = 143 cycles.

007A ;

007A ; Meanwhile in TV world,

007A ; Horizontal retrace = 15 cycles.

007A ; Left blanking border 8 character positions = 32 cycles

007A ; Generation of 75% scanline from the first NEWLINE = 96 cycles

007A ; --------------------------------------- ---

007A ; 143 cycles

007A ; Since at the time the first JP (HL) is encountered to execute the echo

007A ; display another 8 character positions have to be put out, then the

007A ; Refresh register need to hold $F8. Working back and counteracting

007A ; the fact that every instruction increments the Refresh register then

007A ; the value that is loaded into R needs to be $F5. :-)

007A ;

007A D3 FD OUT ($FD),A ; (11) Stop the NMI generator.

007C DD E9 JP (IX) ; (8) forward to L0281 (after top) or L028F