High Level
Data Analytics DSLs

Domain-specific operators

Parallel Pattern Backend

a. Common DSL IR
Parallel Patterns

Parallel pattern operators

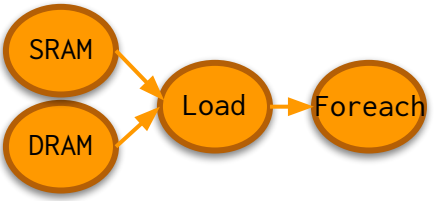
b. Parallel Pattern Compiler
Delite

Array tiling, loop tiling, fusion

Tiled Parallel Pattern IR

Fused and tiled pattern patterns

c. Hardware Lowering



d. Hardware Accelerator IR

Spatial IR

Localized memories and
hardware-specific operations

e. Accelerator Compiler
Spatial

Pipelining, memory banking,
register retiming

FPGA Bitfile

Intermediate Representation (IR)

Compiler / Graph Lowering