High Level Data Analytics DSLs

Domain-specific operators

Parallel Pattern Backend

a. Common DSL IR
Parallel Patterns

Parallel pattern operators

b. Parallel Pattern Compiler
Delite

Array tiling, loop tiling, fusion

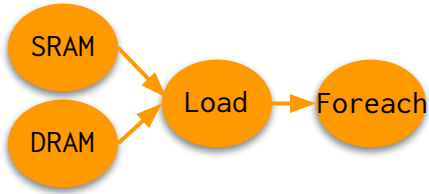
c. Tiled Parallel Pattern IR

Fused and tiled pattern patterns

Hardware Lowering

d. Hardware Accelerator IR

Spatial IR



Localized memories and hardware-specific operations

e. Accelerator Compiler
Spatial

Pipelining, memory banking, register retiming

FPGA Bitfile