Govt. Engineering College, Thrissur

Examination –

DS LAB

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1. Design and Implement binay to gray code Converter.

AIM

Design and Implementation of binary to gray code converter.

DESIGN

Gray code is a non-weighted representation. It is used in telecommunication. There is only one bit change between successive row of data. Here we will be concentrating on 4 bit binary to gray code converter

We have to convert 4 bit binary $B_3\ B_2\ B_1\ B_0$ (B_3 MSB B_0 is LSB) to $G_3\ G_2\ G_1\ G_0$ (Gray bits)
Consider the following truth table.

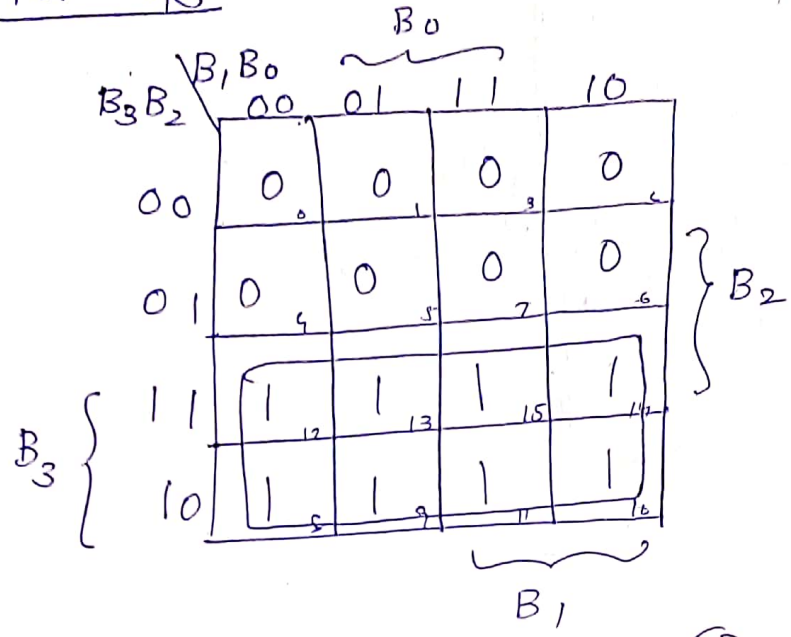
Steps we must follow

① Construct Truth Table P.T.O
② Get the function after inference from truth table by doing K Map (Karnaugh Map)
③ Write the minimised function from K Map
④ Do the combinational circuit using K Map

	Binary				Gray			
	B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

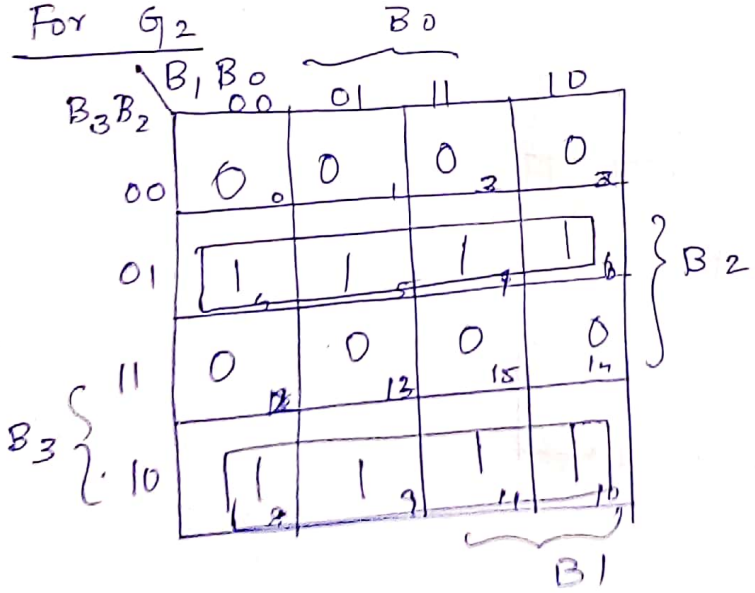
K MAP FROM TRUTH TABLE

For G_3



$\therefore G_3 = B_3$ ——— (1)

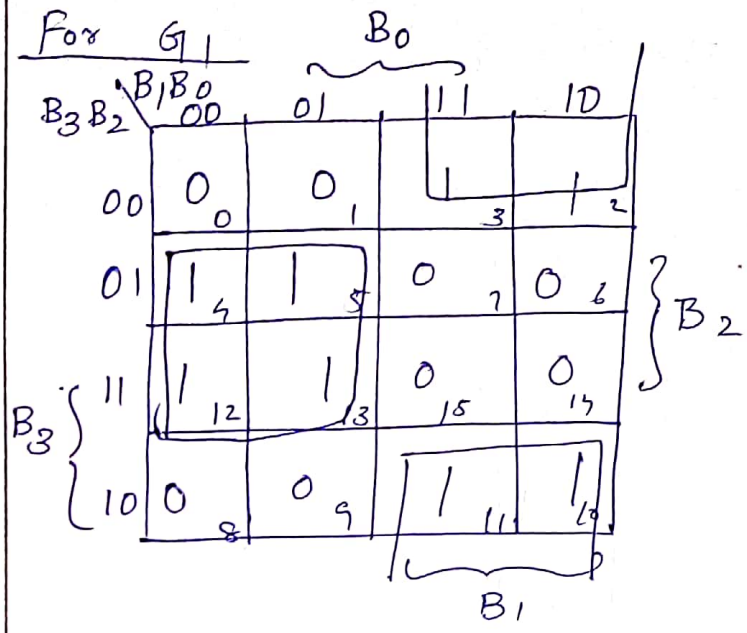
For G_2



$G_2 = \overline{B_3} B_2 + \overline{B_2} B_3$

$G_2 = B_3 \oplus B_2$ ——— (2)

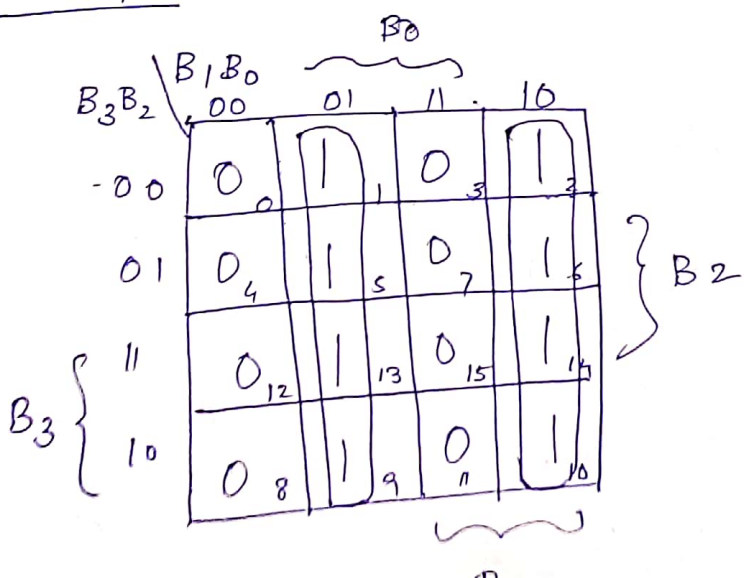
For G_1



$$G_1 = B_2\overline{B_1} + B_1\overline{B_2}$$

$$G_1 = B_1 \oplus B_2 \quad \text{---(3)}$$

For G_0



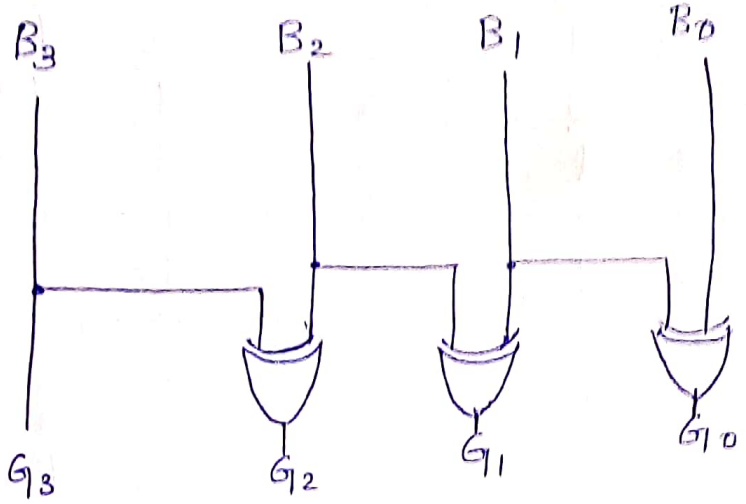
$$G_0 = B_0\overline{B_1} + \overline{B_0}B_1$$

$$G_0 = B_0 \oplus B_1$$

G_0 functions are

$G_3 = B_3$ $G_2 = B_3 \oplus B_2$ $G_1 = B_2 \oplus B_1$ $G_0 = B_1 \oplus B_0$

Combinational circuit:



PROCEDURE

1. Test the components
   - Here components are IC 7486 (XOR) and IC, connecting wires, probes.
   - IC can be tested in digital IC tester.
   - Wires with multimeter.
2. Set up the above circuit on bread board
4. Observe the output of the circuit and compare with truth table & verify.

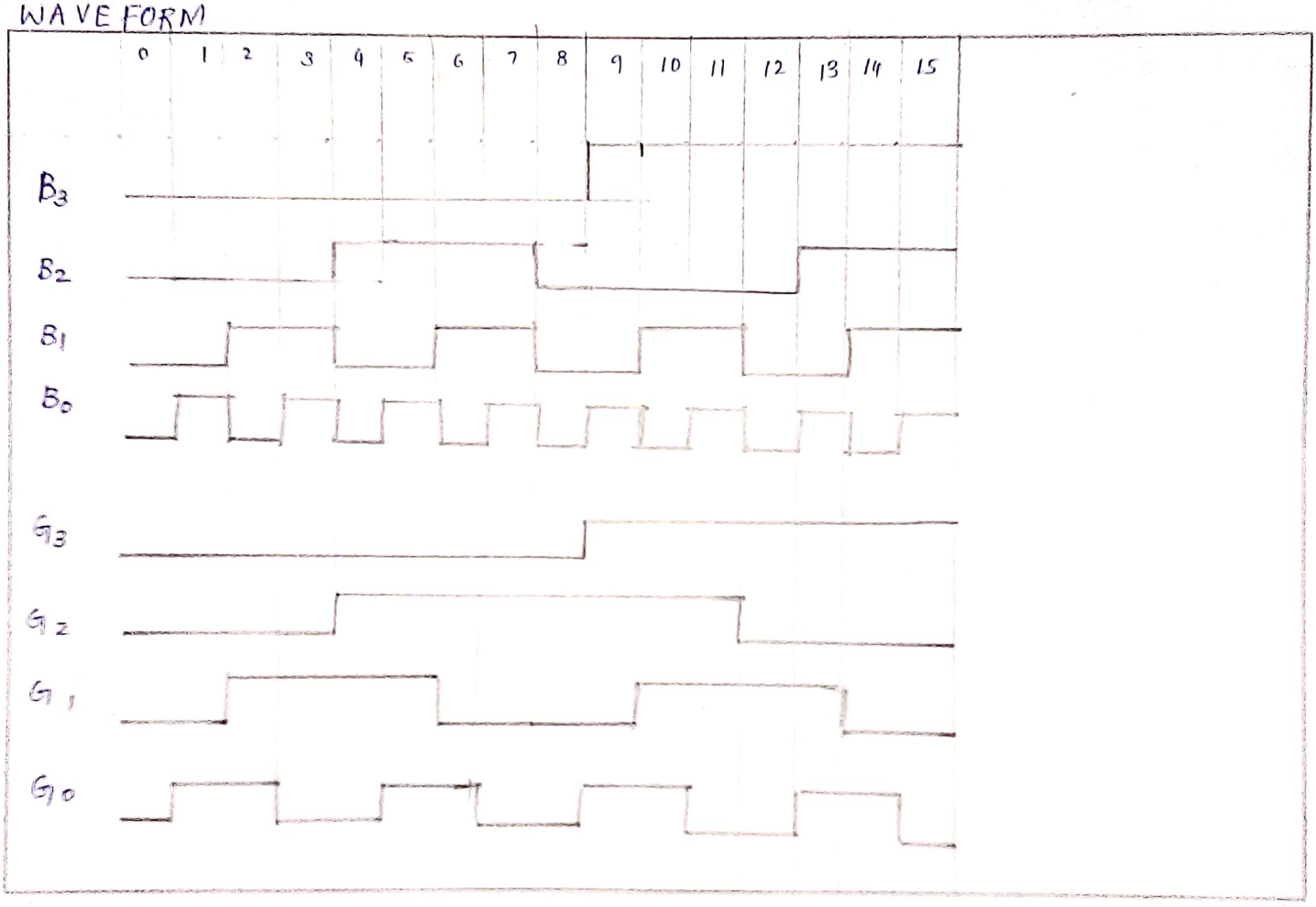
EXPECTED OUTPUT

Expected output when we apply the $B_3B_2B_1B_0$ we should get the output $G_3G_2G_1G_0$ is exactly like truth table.

B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

P.T.O

WAVE FORM



VIVA QUESTIONS

1.

- First 4 clock pulse to enter data 1011 to shift register 1 because its series in series still
- Next 4 is required to make shift register 4 bits of the form 1011. With last clock pulse the output to shift register 3 is obtained.
- Next 4 clock pulse required to get the output in output in series.

→ SISO → SIPO → PISO → out
in 4ck 4ck 4ck

12 clock pulses

2.

a. (i) Synchronous Sequential Circuit (Its RS flip flop is triggered)

(ii) S=1 R=1 is undefined state in truth table of RS flipflop.

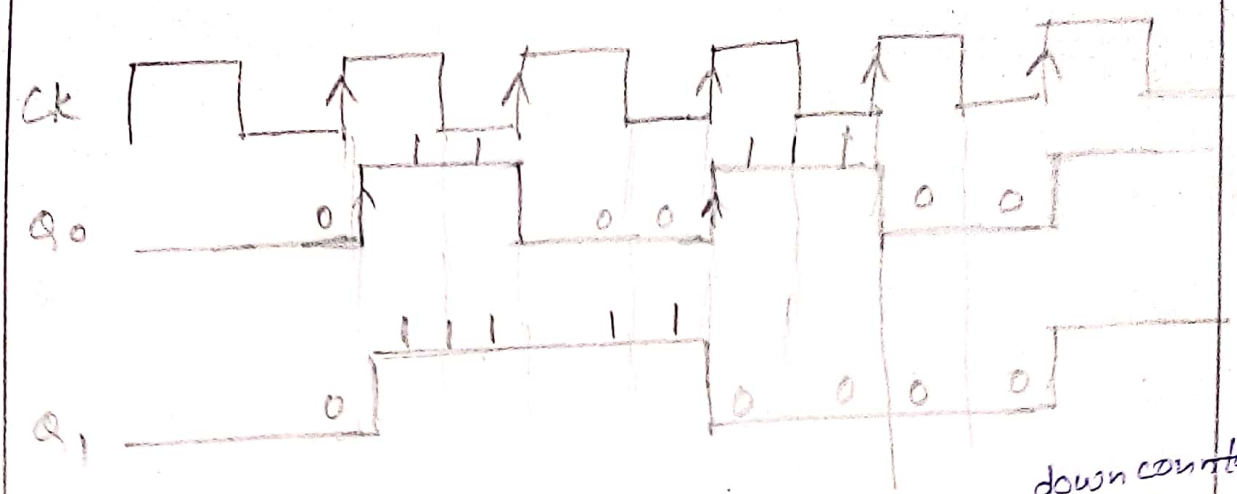
It is called Racecondition (Race Around in JK)

The output toggles.

* When their is a transition from high to low the output just toggle once if out put of Q is Q then after transition the out put will be $\bar{Q}$ of Q.

Ck	R	S	Q	$\bar{Q}$
1	1	1	Q	$\bar{Q}$
↓Transition				
X	1	1	$\bar{Q}$	Q → No change then after since clock is OFF/LOW

3



It is positive edge triggered asynchronous down counter so the output is like above waveform.