BoW Statistical Channel Model Simulations

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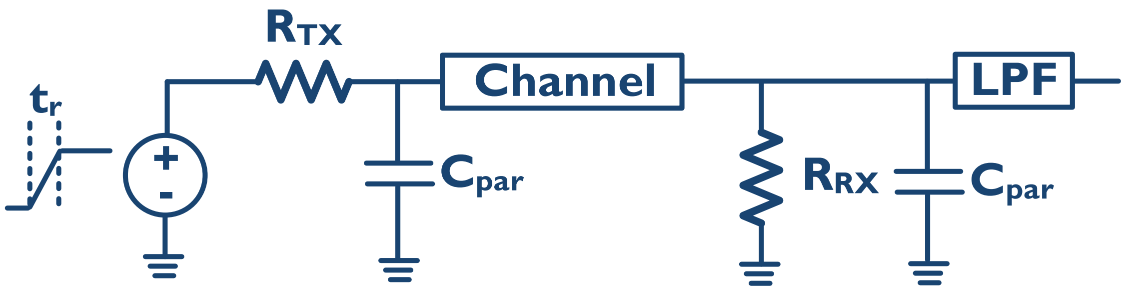
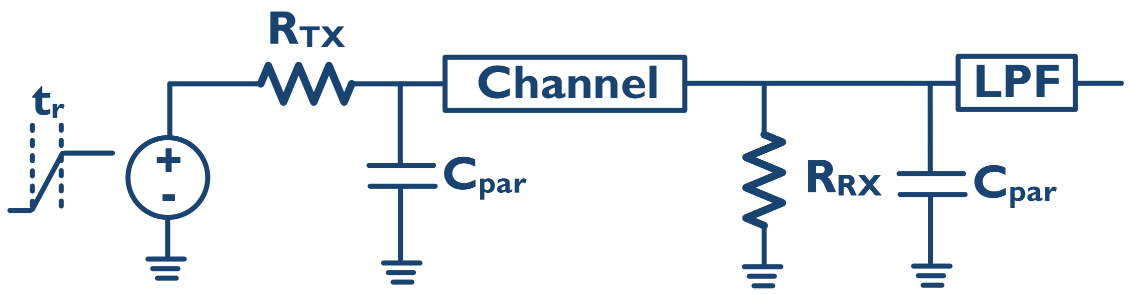
Global Setup: Channel / TX / RX Models



- **TX/RX simplified models currently use the same parasitic capacitance on both sides**
  - But these can be decoupled; in general we've seen similar SI impact from cap on either side
  - Unterminated signaling modeled by setting R_{RX} to a large value (e.g., ~10KΩ)

- **Note that as of 12-1-201, risetime is <u>before</u> the RC filter, which is slightly pessimistic**
  - Results so far show that risetime does not have a significant impact on margin

Global Setup: Channel / TX / RX Models



- **LPF = Low-Pass Filter**
  - Modeled as a first-order filter
  - Bandwidth of this filter is set to achieve continuous time bandwidth of 2/3/Tbit (as required in the spec) considering the filtering caused by the channel driving R_{RX} and C_{par}
  - (For reasonable values of R_{RX} and C_{par}, most of the bandwidth is really set by the LPF)

Global Setup: Analysis

- **All TX data ports are excited with data, and responses/statistics on all data RX ports are computed**
  - In channels that include TX ports for the CLK, those ports are excited with differential clocks
  - In channels that include RX ports for the CLK, those are used to compute jitter due crosstalk
    - Clock RX common-mode to differential voltage conversion gain assumed to be 0.2
- **Timing margins are always reported from whatever the worst-case RX data port within a given channel model is**
- **From BoW spec (as of 12-1-2021), 68% margin is required for a channel to be compliant**
  - 50% (eye opening at RX) + 18% (skew / jitter for TX)

Global Setup: Analysis

- **Items not yet included in the analysis (as of 1-3-2022):**
  - Interaction between TX circuit skew and crosstalk statistics
  - Allowed channel skew (all margin numbers assume no skew or perfect per-bit adjustment)

Updated Global Setup (1-12-2022)

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- **Current spec for line-to-line skew on the channel allows for +/-1mm, which without per-bit correct capabilities, requires an additional ~21.3% of UI additional peak-to-peak margin at 16Gb/s**
  - Basically implies that one would have to support per-bit delay correction at 16Gb/s for channels with this kind of skew
  - Or that we need to tighten the length mismatch and recover margin elsewhere

- **All previous sims lumped true random voltage noise at RX into sensitivity figure**
  - This is (intentionally) pessimistic, but may want to revisit this choice to close the overall link budget

Proposals from 1-12-2022 Meeting

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(1) Reduce capacitance from 300fF to 250fF for BoW 256 (and scale capacitance for other rates accordingly)

(2) Tighten 20% - 80% risetime to 23% UI

- Combination of (1) and (2) improves margin by ~7% UI

(3) Split TX and RX timing budgets into deterministic and random

- Reduces pessimism by ~5% UI

(4) Split RX voltage sensitivity into deterministic and random

- Reduces pessimism by ~4% UI

(5) Readjust TX vs. RX total timing budgets to reduce burden on TX

- Roughly, reduced ~50% eye at RX to ~40%
- Tighten RX deterministic timing error at lowest rates (BoW 64 and BoW 32) in order to relax RX voltage sensitivity requirements

(6) Tighten nominal allowed channel skew to +/-2% UI

- But will note that implementers may choose to implement per-bit deskew and exceed this

(7) Tighten RX sensitivity to 100mV for BoW 128, 150mV for BoW 64 & BoW 32

- Original RX sensitivity made even very low rates non-functional due to shape of eye diagram and significant reflections with unterminated signaling

Proposed Timing Budgets

BoW-256, BoW-128

Item	Value	Required Range	Remaining One-Sided Margin
TX Risetime + Channel (ISI + XTALK + CLK DJ) Eye Opening (UI)	64.00%		0.32
Channel Residual Static Clk-Data Skew (UI, p2p)	4.00%		0.3
TX Deterministic Clk-Data + Duty Cycle Error (UI, p2p)	14.00%		0.23
Deterministic Margin at RX (UI)	46.00%		0.23
RX Deterministic Clk-Data Error (UI, p2p)	32.00%		0.07
One-Sided Margin for Jitter (UI)		14.00%	0.07
Random Jitter Subcomponents		**Value in ps at 16Gb/s**	
TX Random Jitter After RX Delay (σ, UI)	0.69%	0.43	
Total TX Random Jitter @ 1e-15 (UI, p2p)	11.00%	6.875	
RX Random Jitter (σ, UI)	0.54%	0.34	
Total RX Random Jitter @ 1e-15 (UI, p2p)	8.66%	5.41	
Total Random Jitter After RX Delay (σ, UI)	0.88%	0.55	
Total Random Jitter @ 1e-15 (UI, p2p)	14.00%	8.75	

BoW-64, BoW-32

Item	Value	Required Range	Remaining One-Sided Margin
TX Risetime + Channel (ISI + XTALK + CLK DJ) Eye Opening (UI)	60.00%		0.3
Channel Residual Static Clk-Data Skew (UI, p2p)	4.00%		0.28
TX Deterministic Clk-Data + Duty Cycle Error (UI, p2p)	14.00%		0.21
Deterministic Margin at RX (UI)	42.00%		0.21
RX Deterministic Clk-Data Error (UI, p2p)	28.00%		0.07
One-Sided Margin for Jitter (UI)		14.00%	0.07
Random Jitter Subcomponents		**Value in ps at 16Gb/s**	
TX Random Jitter After RX Delay (σ, UI)	0.69%	0.43	
Total TX Random Jitter @ 1e-15 (UI, p2p)	11.00%	6.875	
RX Random Jitter (σ, UI)	0.54%	0.34	
Total RX Random Jitter @ 1e-15 (UI, p2p)	8.66%	5.41	
Total Random Jitter After RX Delay (σ, UI)	0.88%	0.55	
Total Random Jitter @ 1e-15 (UI, p2p)	14.00%	8.75	

Available Channel Models

- **Channel models contributed by Namhoon Kim (“Full Slice”)**
  - Representative only – not associated with any real design/project
  - Full 16 data wires + clocks for each slice; slices on layers 2 (stripline) and 4 (stripline) are included in a single model
    - Worst-case RX within both slices is found / reported
  - 2mm, 10mm, 25mm reach

- **Channel models developed by ARM**
  - Full 18 data wires + clocks
  - Layers 2 (stripline), 4 (stripline), and 8 (stripline), ~20mm reach

- **Channel model from Keysight**
  - Includes only 5 wires
    - For clock jitter, run a separate sim with two of the middle lines chosen as CLK+/CLK-
  - 6mm reach

Summary of Results

Channel Rate / Term	Scenario	Full Slice 2mm	Full Slice 10mm	Full Slice 25mm	ARM Layer A	ARM Layer B	ARM Layer D	Keysight
16 Gb/s, Doubly Terminated	C = 250fF, t_r = 23% $\sigma_{rx,vn}$ = 2.2mV, $V_{sens,det}$ = 40mV	68.4% (72% / 3.6%)	64.8% (67.6% / 2.8%)	64.8% (67.2% / 2.4%)	71.2% (74% / 2.8%)	63.4% (66% / 3.6%)	49.6% (54.4% / 4.8%)	66.8% (71.6% / 4.8%)
	C = 200fF, t_r = 23% $\sigma_{rx,vn}$ = 2.2mV, $V_{sens,det}$ = 40mV			67.6% (70% / 2.4%)	74.4% (76.4% / 2%)	66.4% (69.2% / 2.8%)	54% (58% / 4%)	
16 Gb/s, Source Terminated	C = 200fF, t_r = 23% $\sigma_{rx,vn}$ = 2.2mV, $V_{sens,det}$ = 40mV	59.6% (65.6% / 6%)						
8 Gb/s, Source Terminated	C = 500fF, t_r = 23% $\sigma_{rx,vn}$ = 3.14mV, $V_{sens,det}$ = 100mV	74% (75.6% / 1.6%)	47.6% (55.2% / 7.6%)					58.8% (61.6% / 2.8%)
	C = 400fF, t_r = 23% $\sigma_{rx,vn}$ = 3.14mV, $V_{sens,det}$ = 100mV	78.4% (79.6% / 1.2%)						62.4% (64.4% / 2%)
4 Gb/s, Doubly Terminated	C = 1pF, t_r = 23% $\sigma_{rx,vn}$ = 2.2mV, $V_{sens,det}$ = 65mV			71.2% (73.2% / 2%)			68% (71.2% / 3.2%)	76.4% (78% / 1.6%)
	C = 800fF, t_r = 23% $\sigma_{rx,vn}$ = 2.2mV, $V_{sens,det}$ = 65mV							
4 Gb/s, Source Terminated	C = 1pF, t_r = 23% $\sigma_{rx,vn}$ = 3.14mV, $V_{sens,det}$ = 150mV	61.2% (63.2% / 2%)	60% (63.6% / 3.6%)		48.8% (56.8% / 8%)		39.2% (48.8% / 9.6%)	68.8% (71.2% / 2.4%)
	C = 800fF, t_r = 23% $\sigma_{rx,vn}$ = 3.14mV, $V_{sens,det}$ = 150mV							

Update 2-9-2022

- **New set of channel models from ARM**
  - Now have full set of slices (layers 2, 4, 6, and 8)
  - Improvements were made to the package design, particularly to address reduced margins available on deeper layers

Summary of Results (2-9-2022)

Channel Rate / Term	Scenario	Full Slice 2mm	Full Slice 25mm	ARM Layer A	ARM Layer B	ARM Layer C	ARM Layer D	Keysight
16 Gb/s, Doubly Terminated	C = 250fF, t_r = 23% $\sigma_{rx,vn}$ = 2.2mV, $V_{sens,det}$ = 40mV	68.4% (72% / 3.6%)	64.8% (67.2% / 2.4%)					66.8% (71.6% / 4.8%)
	C = 200fF, t_r = 23% $\sigma_{rx,vn}$ = 2.2mV, $V_{sens,det}$ = 40mV		67.6% (70% / 2.4%)	74% (76.4% / 2.4%)	65.6% (68.8% / 3.2%)	60.8% (64.4% / 3.6%)	57.6% (61.2% / 3.6%)	
16 Gb/s, Source Terminated	C = 200fF, t_r = 23% $\sigma_{rx,vn}$ = 2.2mV, $V_{sens,det}$ = 40mV	59.6% (65.6% / 6%)						
8 Gb/s, Source Terminated	C = 500fF, t_r = 23% $\sigma_{rx,vn}$ = 3.14mV, $V_{sens,det}$ = 100mV	74% (75.6% / 1.6%)						58.8% (61.6% / 2.8%)
	C = 400fF, t_r = 23% $\sigma_{rx,vn}$ = 3.14mV, $V_{sens,det}$ = 100mV	78.4% (79.6% / 1.2%)						62.4% (64.4% / 2%)
4 Gb/s, Doubly Terminated	C = 1pF, t_r = 23% $\sigma_{rx,vn}$ = 2.2mV, $V_{sens,det}$ = 65mV		71.2% (73.2% / 2%)				68% (71.2% / 3.2%)	76.4% (78% / 1.6%)
	C = 800fF, t_r = 23% $\sigma_{rx,vn}$ = 2.2mV, $V_{sens,det}$ = 65mV							
4 Gb/s, Source Terminated	C = 1pF, t_r = 23% $\sigma_{rx,vn}$ = 3.14mV, $V_{sens,det}$ = 150mV	61.2% (63.2% / 2%)						68.8% (71.2% / 2.4%)
	C = 800fF, t_r = 23% $\sigma_{rx,vn}$ = 3.14mV, $V_{sens,det}$ = 150mV			56.4% (62.8% / 6.4%)		51.4% (58% / 7.6%)		

16Gb/s Doubly Terminated

Full Slice 2mm Results:
20%-80% risetime = 23% UI, Cpar = 250fF

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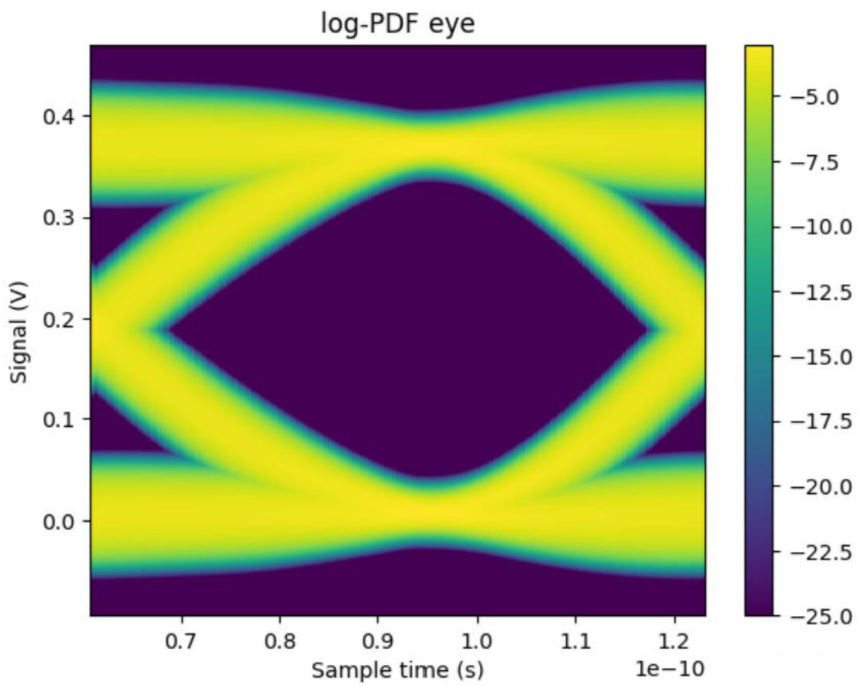
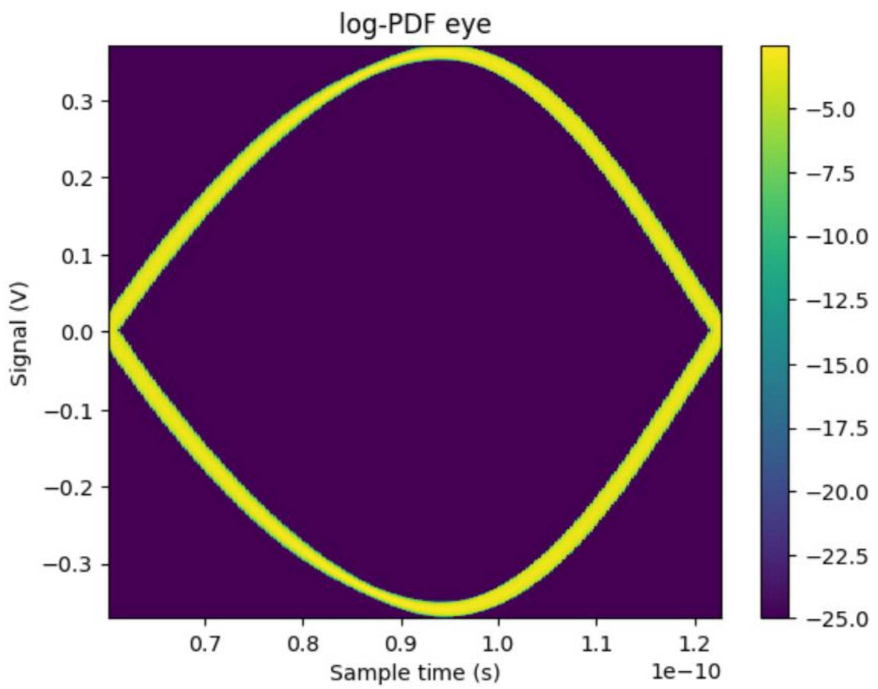
Worst Data Eye | **Diff. Clock**

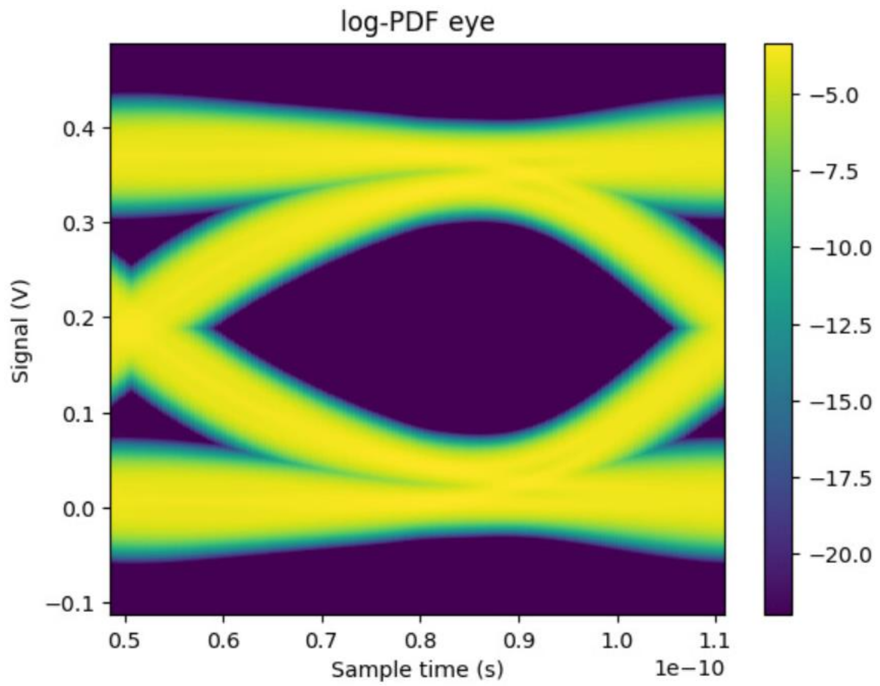




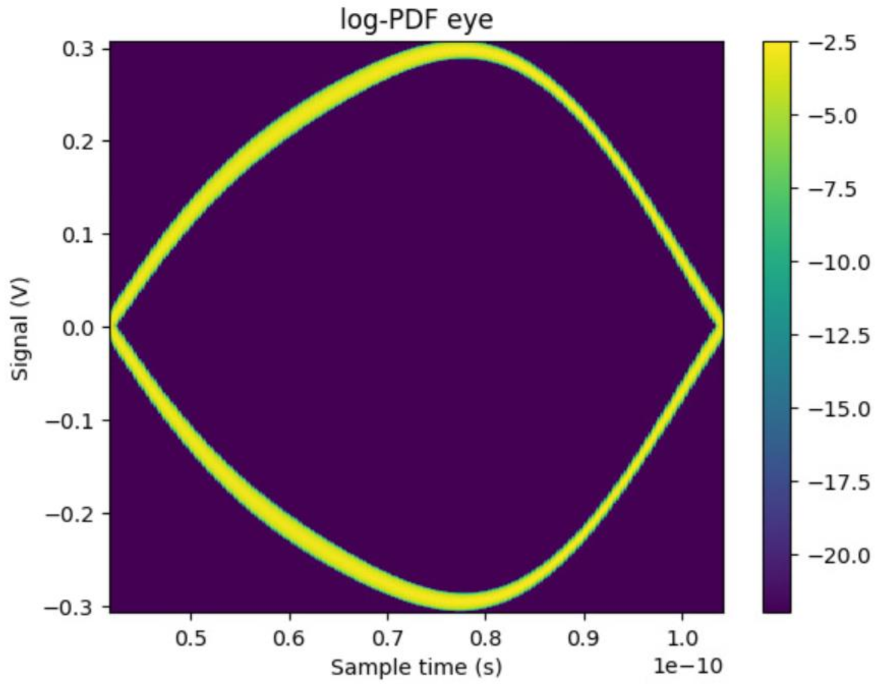
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 72% / 3.6%**

Full Slice 10mm Results:
20%-80% risetime = 23% UI, Cpar = 250fF

Worst Data Eye



Diff. Clock



- Worst line timing margin / crosstalk jitter @ 1e-15 BER: 67.6% / 2.8%

Full Slice 25mm Results:
20%-80% risetime = 23% UI, Cpar = 250fF

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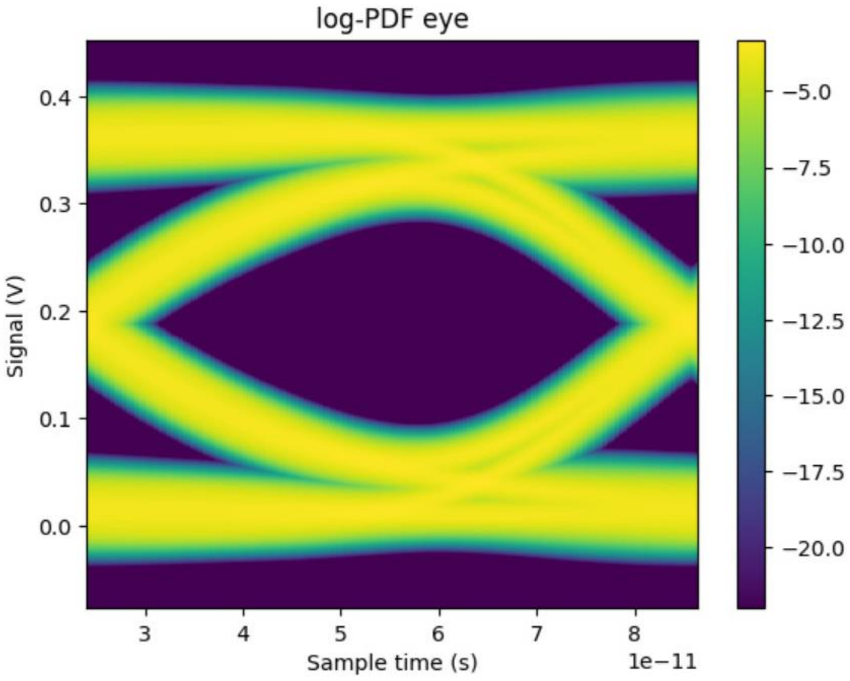
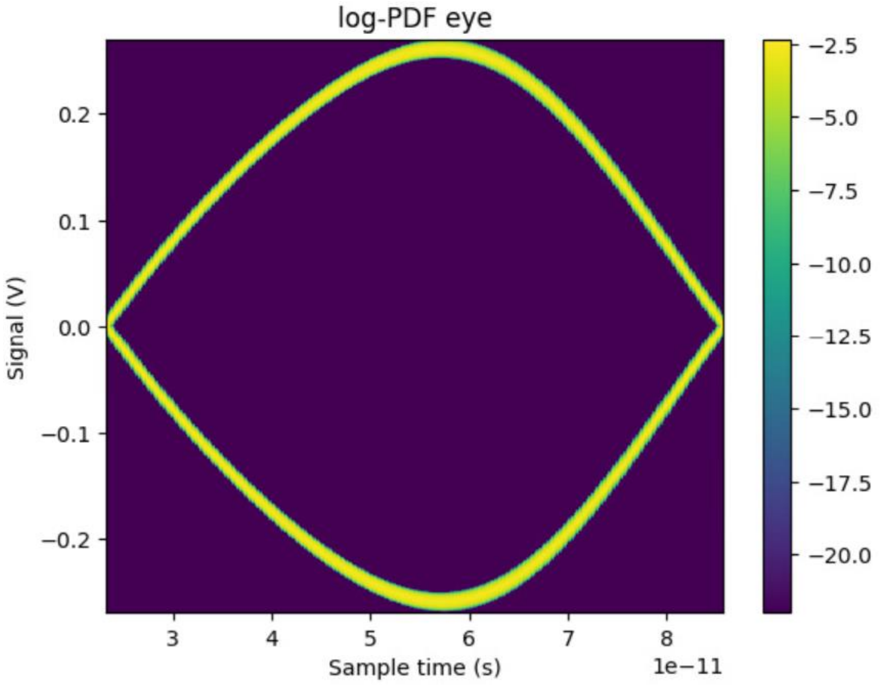
Worst Data Eye



Diff. Clock



- Worst line timing margin / crosstalk jitter @ 1e-15 BER: 67.2% / 2.4%

Full Slice 25mm Results:
20%-80% risetime = 23% UI, Cpar = 200fF

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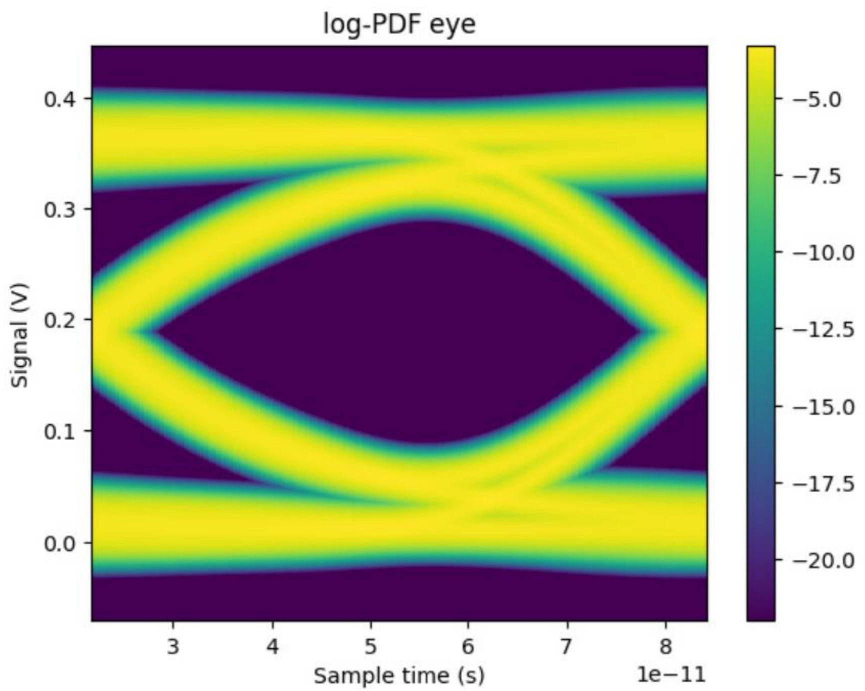
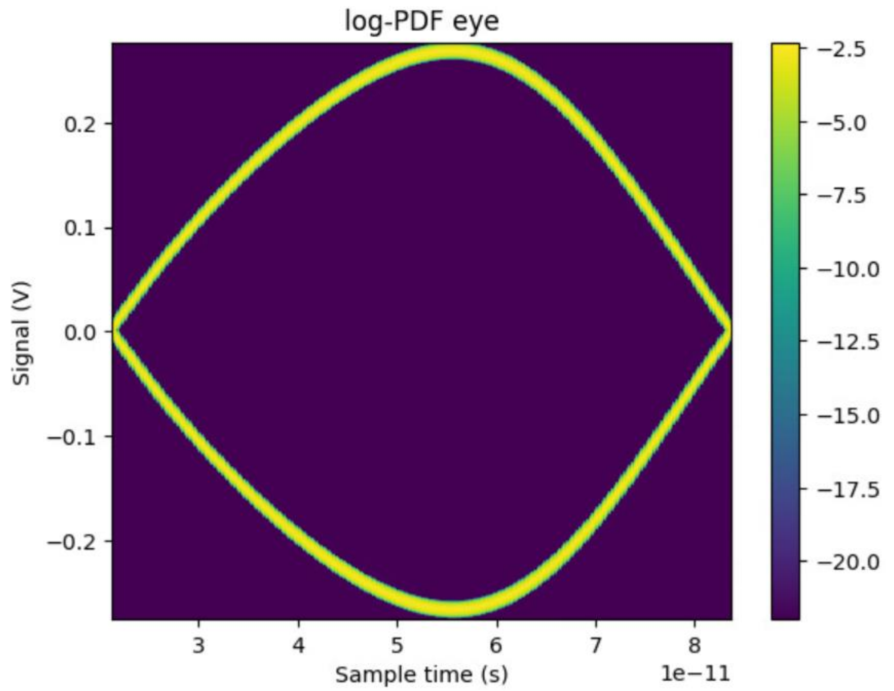
Worst Data Eye



Diff. Clock



- Worst line timing margin / crosstalk jitter @ 1e-15 BER: 70% / 2.4%

ARM Layer A Results:
20%-80% risetime = 23% UI, Cpar = 250fF

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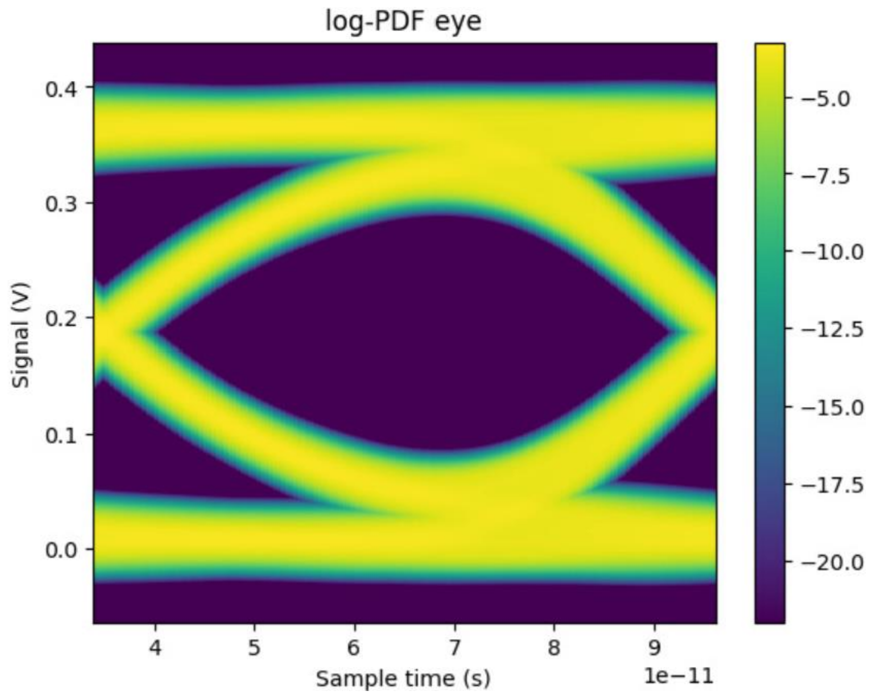
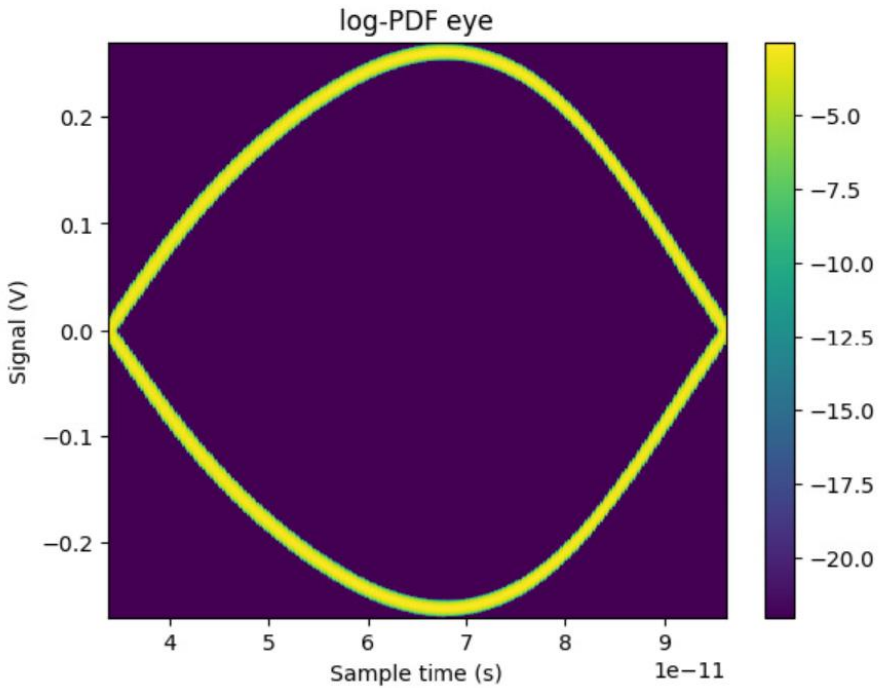
Worst Data Eye



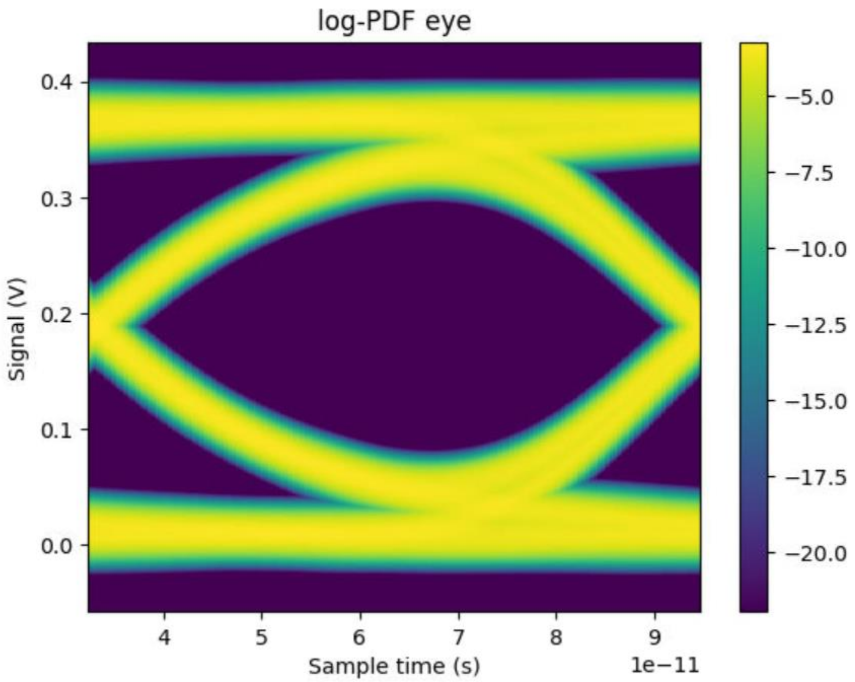
Diff. Clock



- Worst line timing margin / crosstalk jitter @ 1e-15 BER: 74% / 2.8%

ARM Layer A Results:
20%-80% risetime = 23% UI, Cpar = 200fF

Worst Data Eye



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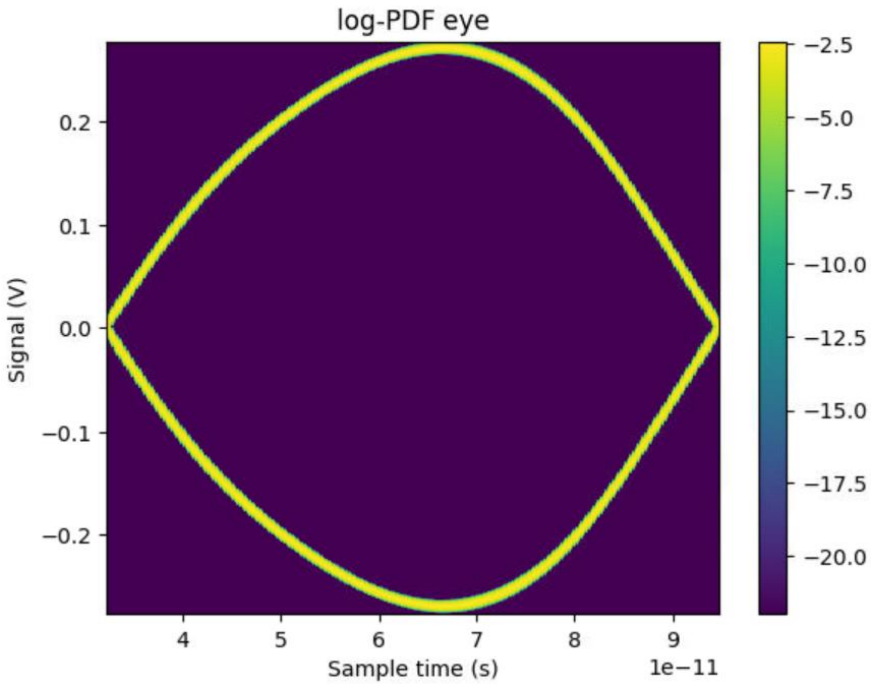
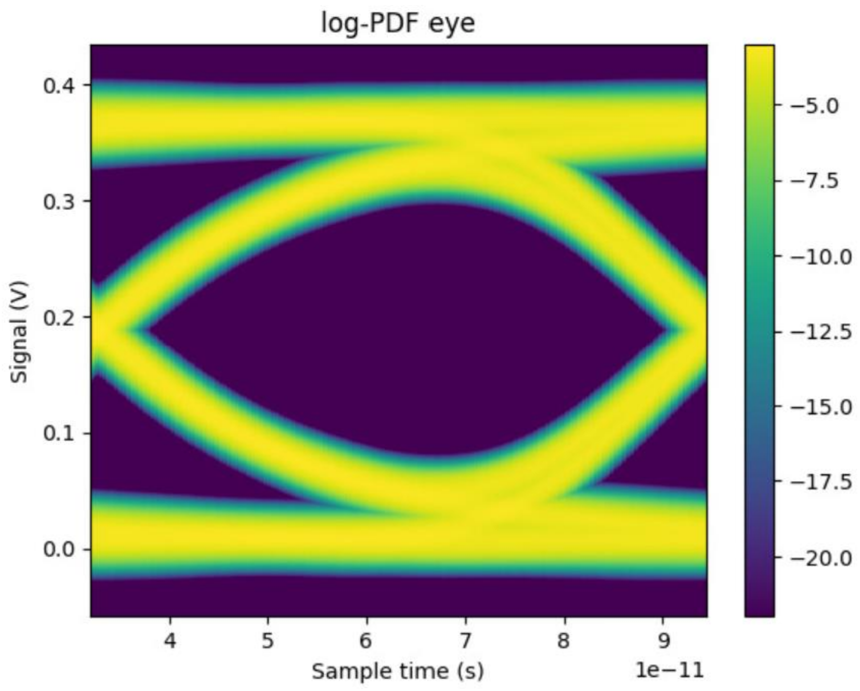


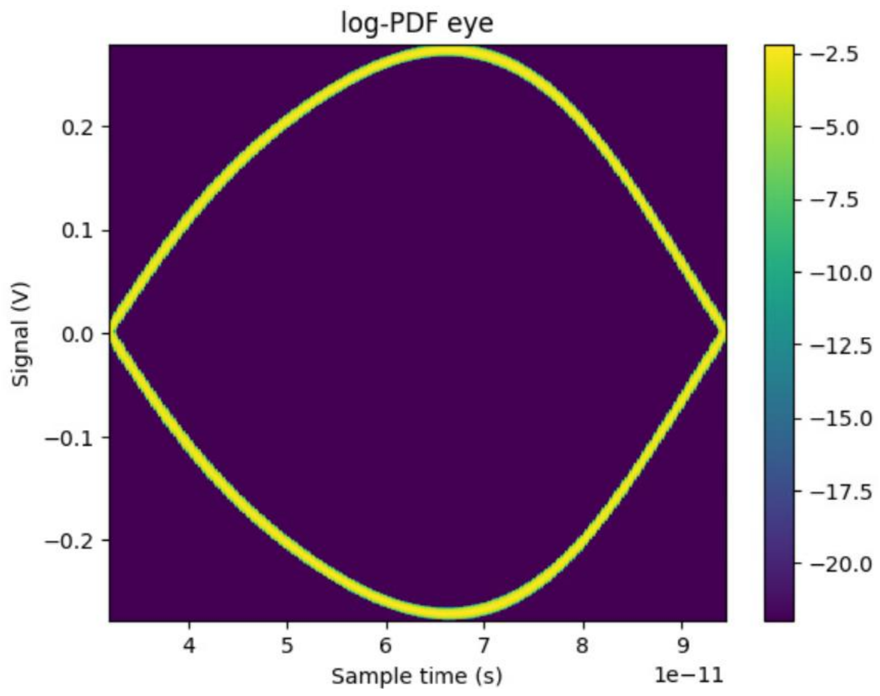
- Worst line timing margin / crosstalk jitter @ 1e-15 BER: 76.4% / 2%

(2-9-2022) ARM Layer A Results:
20%-80% risetime = 23% UI, Cpar = 200fF

Worst Data Eye



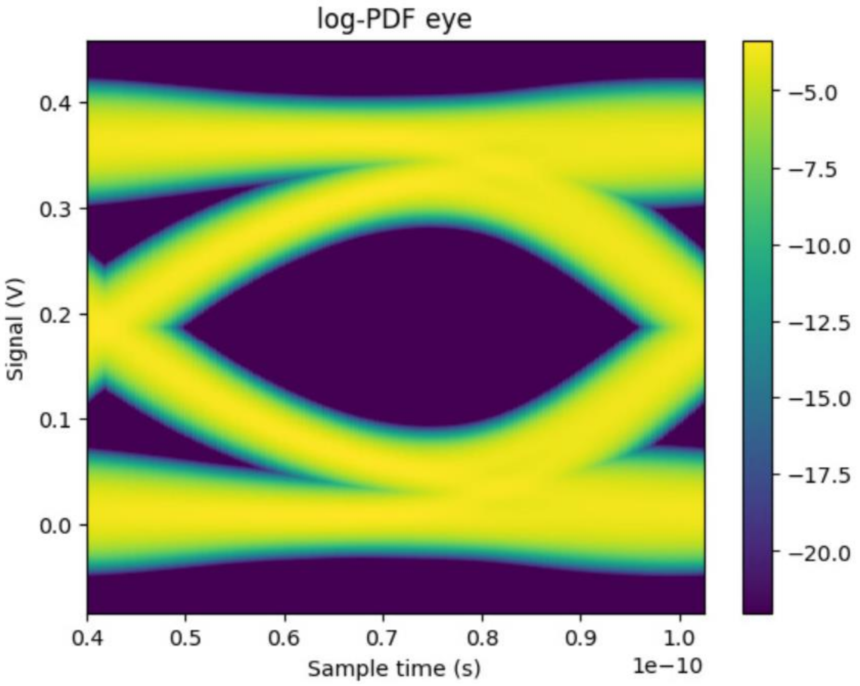
Diff. Clock



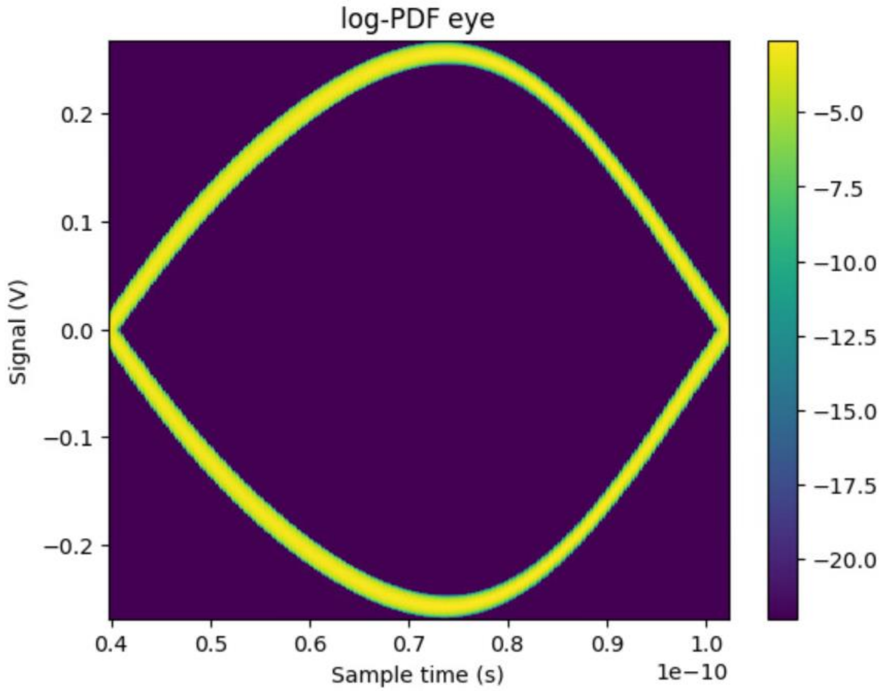
- Worst line timing margin / crosstalk jitter @ 1e-15 BER: 76.4% / 2.4%

ARM Layer B Results:
20%-80% risetime = 23% UI, Cpar = 250fF

Worst Data Eye



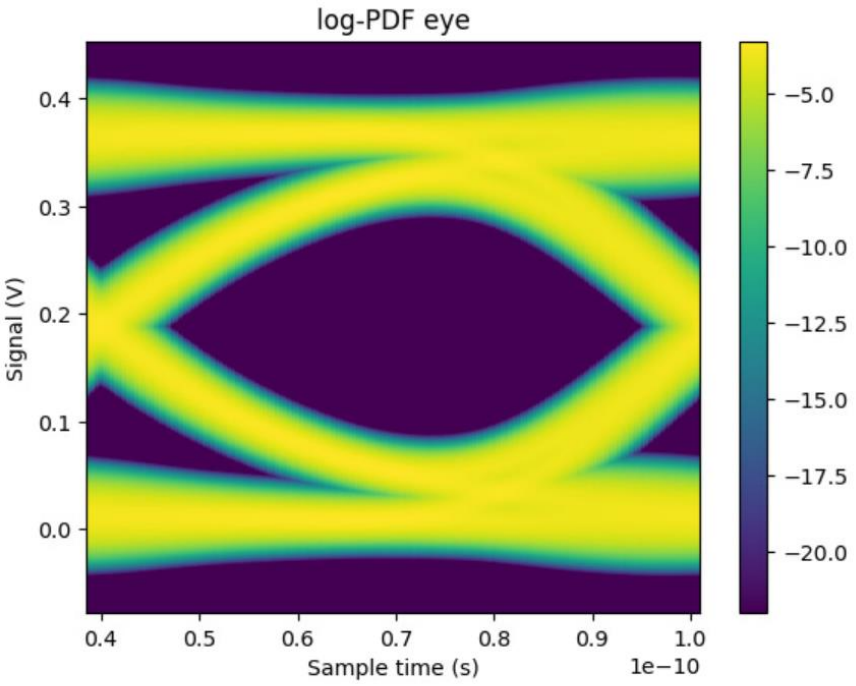
Diff. Clock



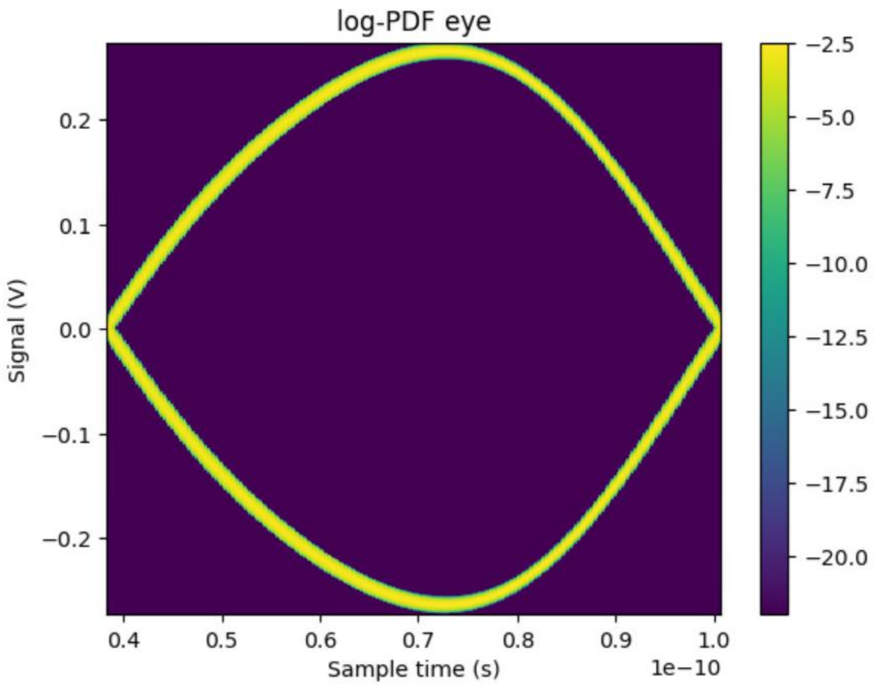
- Worst line timing margin / crosstalk jitter @ 1e-15 BER: 66% / 3.6%

ARM Layer B Results:
20%-80% risetime = 23% UI, Cpar = 200fF

Worst Data Eye



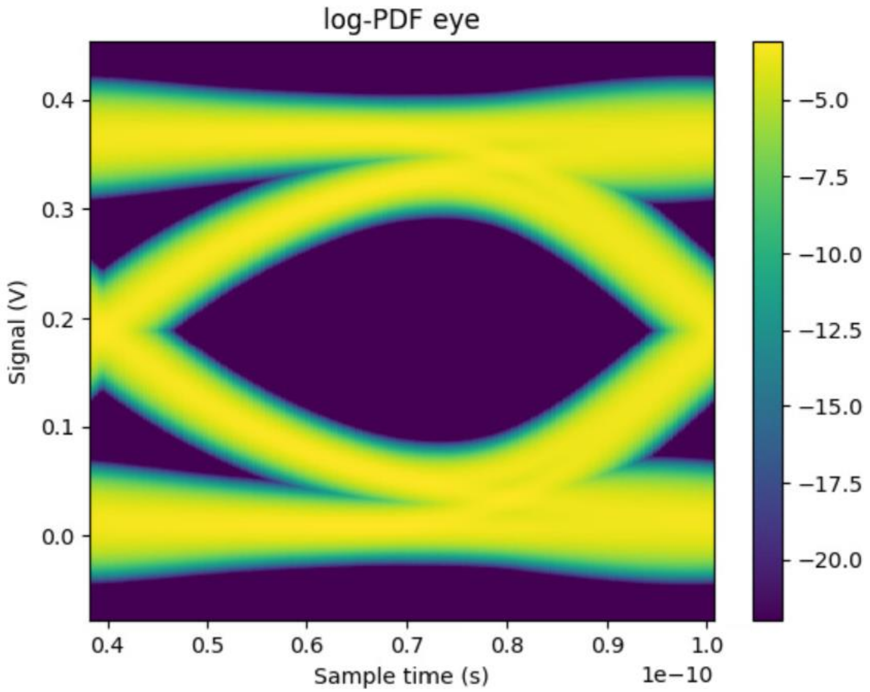
Diff. Clock



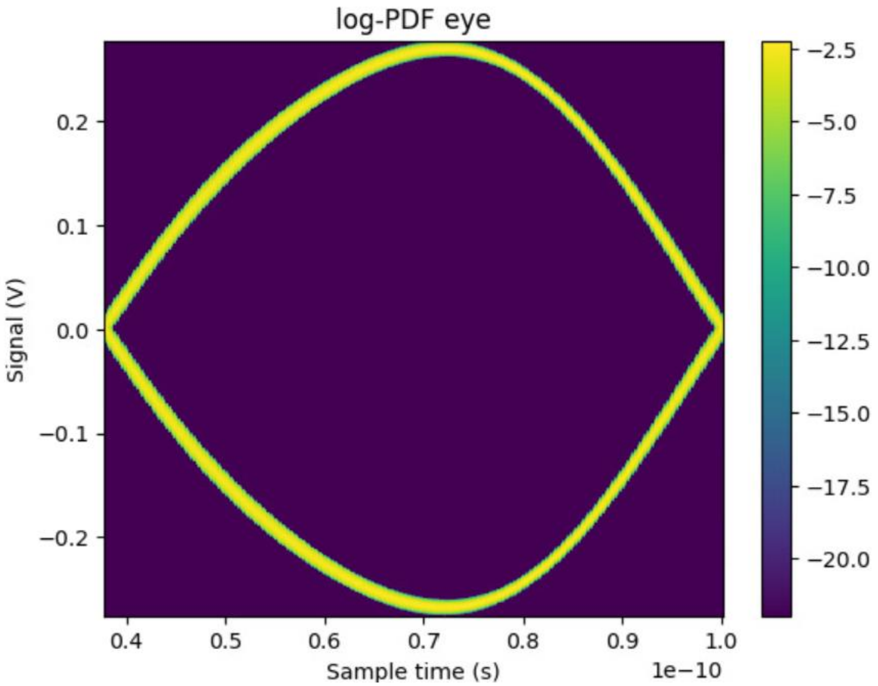
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 69.2% / 2.8%**

(2-9-2022) ARM Layer B Results:
20%-80% risetime = 23% UI, Cpar = 200fF

Worst Data Eye



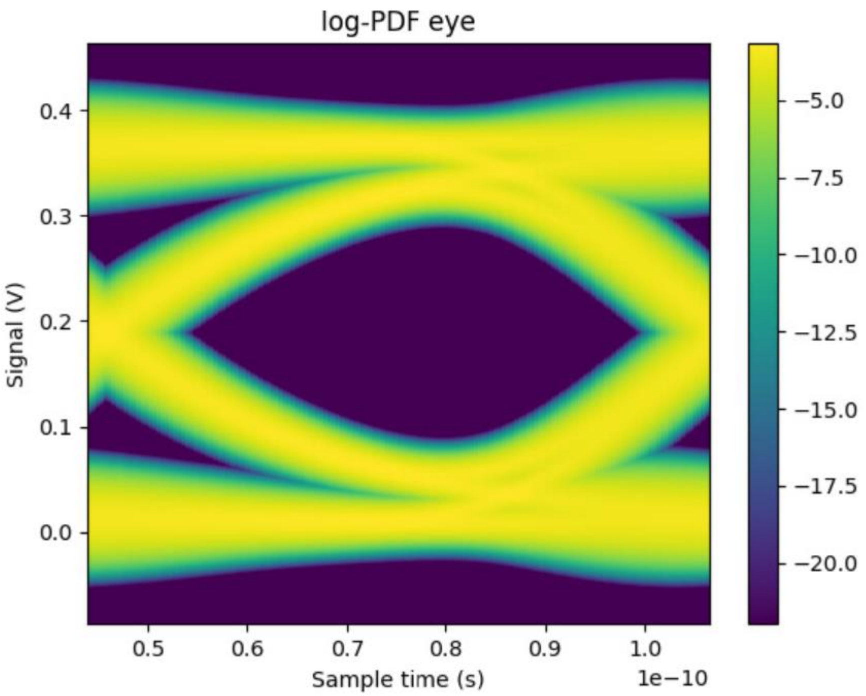
Diff. Clock



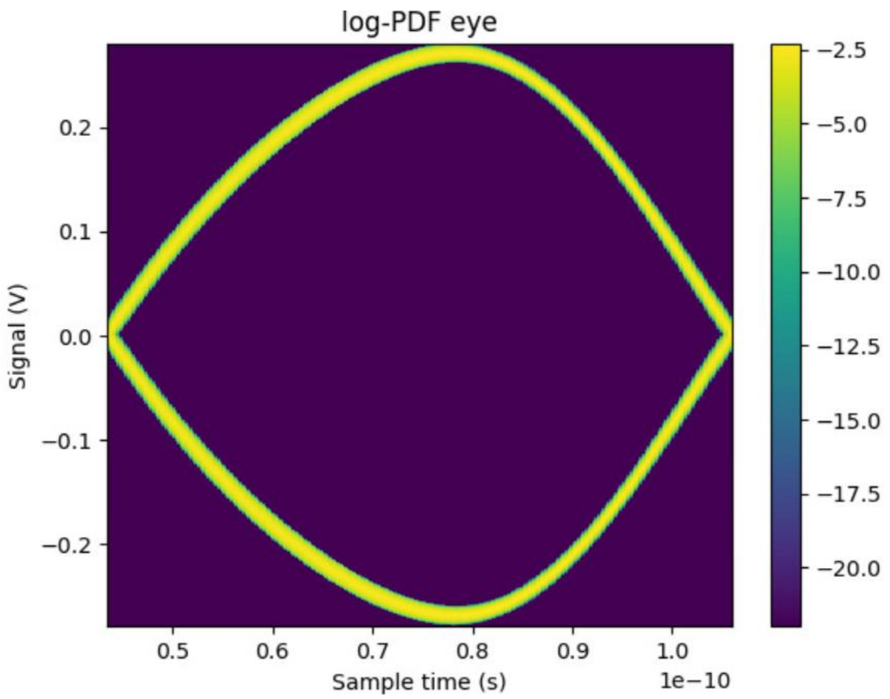
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 68.8% / 3.2%**

(2-9-2022) ARM Layer C Results:
20%-80% risetime = 23% UI, Cpar = 200fF

Worst Data Eye



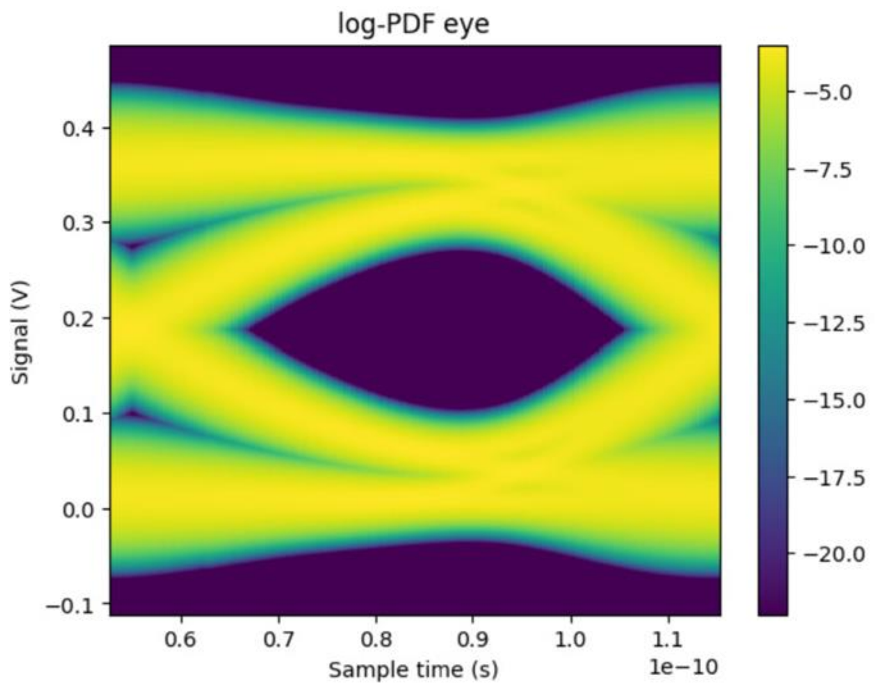
Diff. Clock



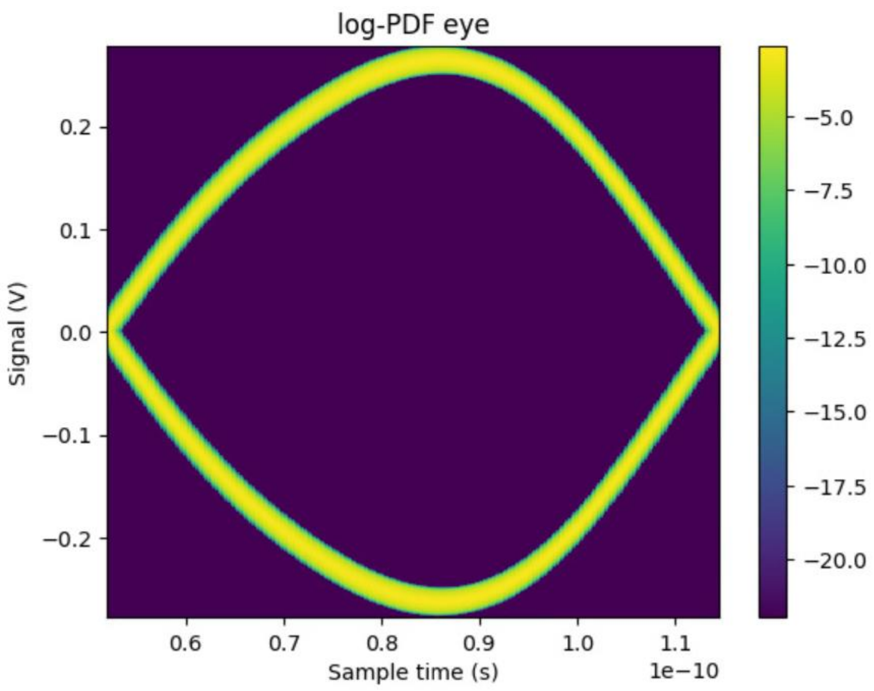
- Worst line timing margin / crosstalk jitter @ 1e-15 BER: 64.4% / 3.6%

ARM Layer D Results:
20%-80% risetime = 23% UI, Cpar = 250fF

Worst Data Eye



Diff. Clock



- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 54.4% / 4.8%**

ARM Layer D Results:

20%-80% risetime = 23% UI, Cpar = 200fF

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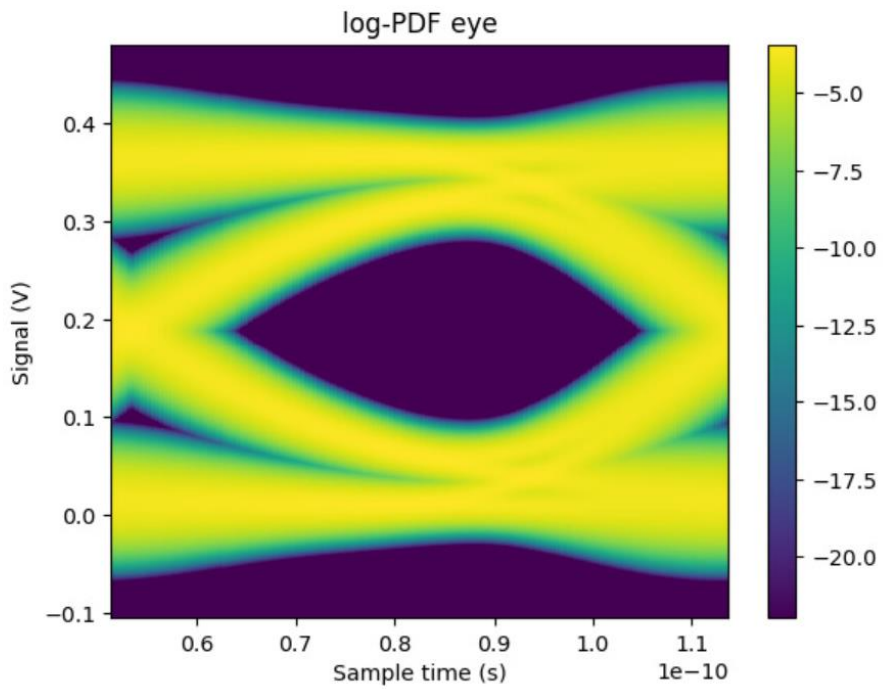
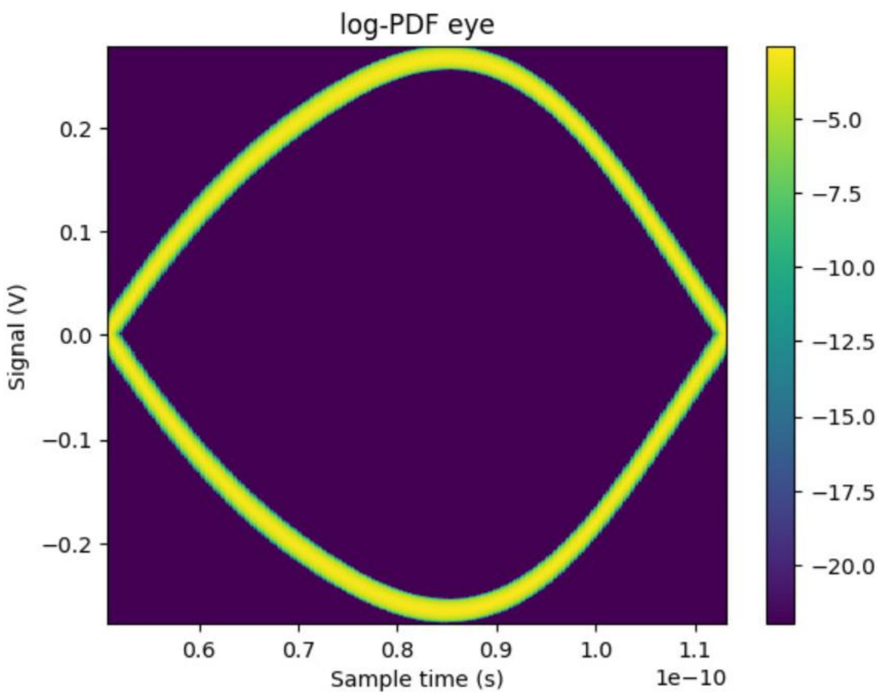
Worst Data Eye



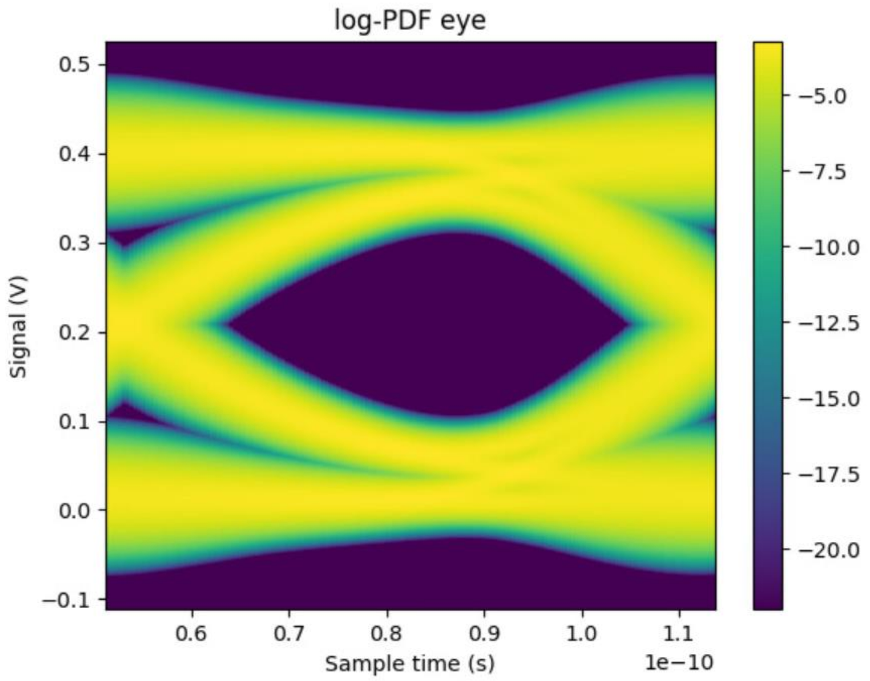
Diff. Clock



- Worst line timing margin / crosstalk jitter @ 1e-15 BER: 58% / 4%

ARM Layer D Results:
23% UI, 200fF, RTX = 45Ω, RRX = 55Ω

Worst Data Eye



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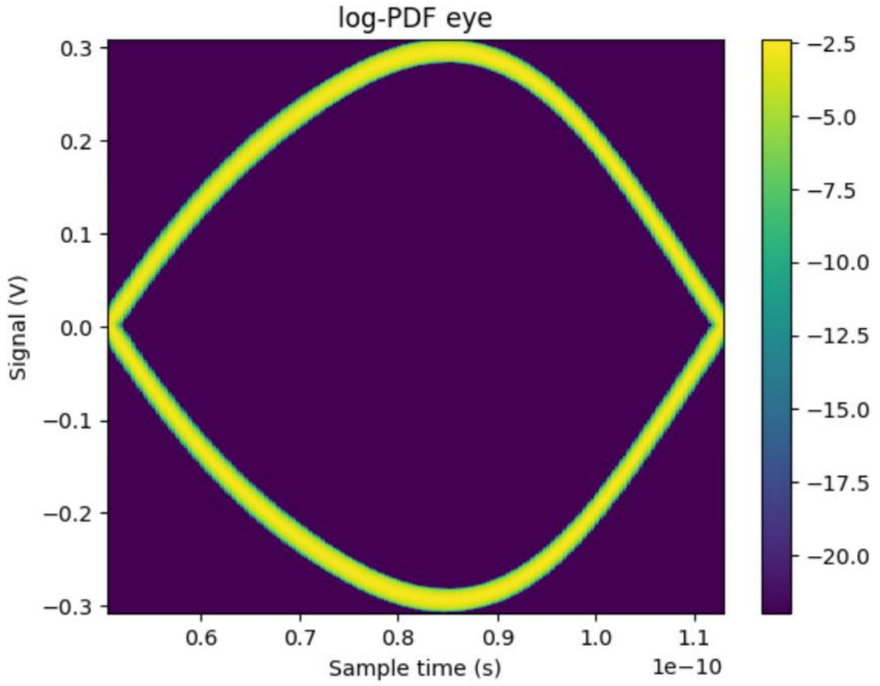
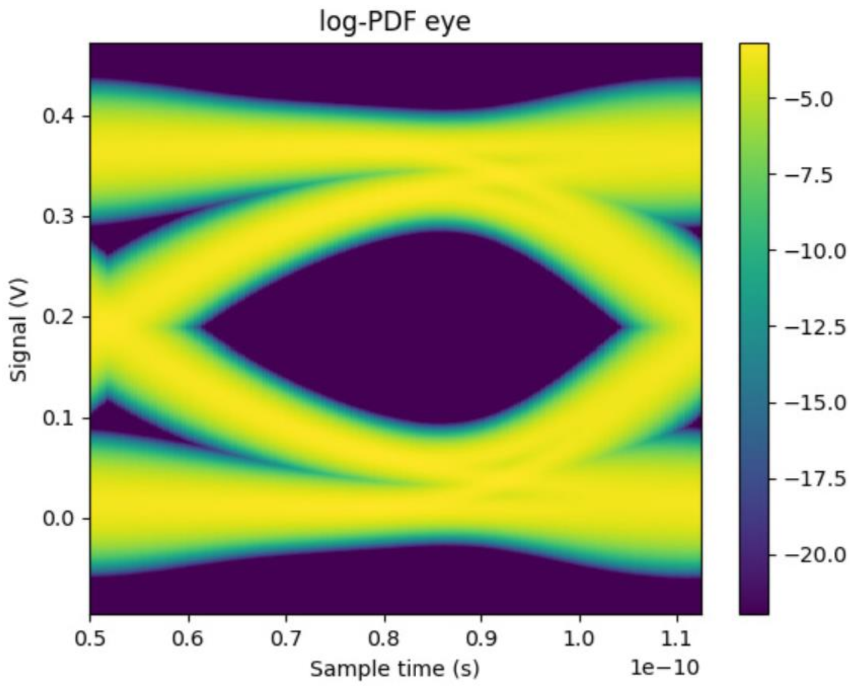


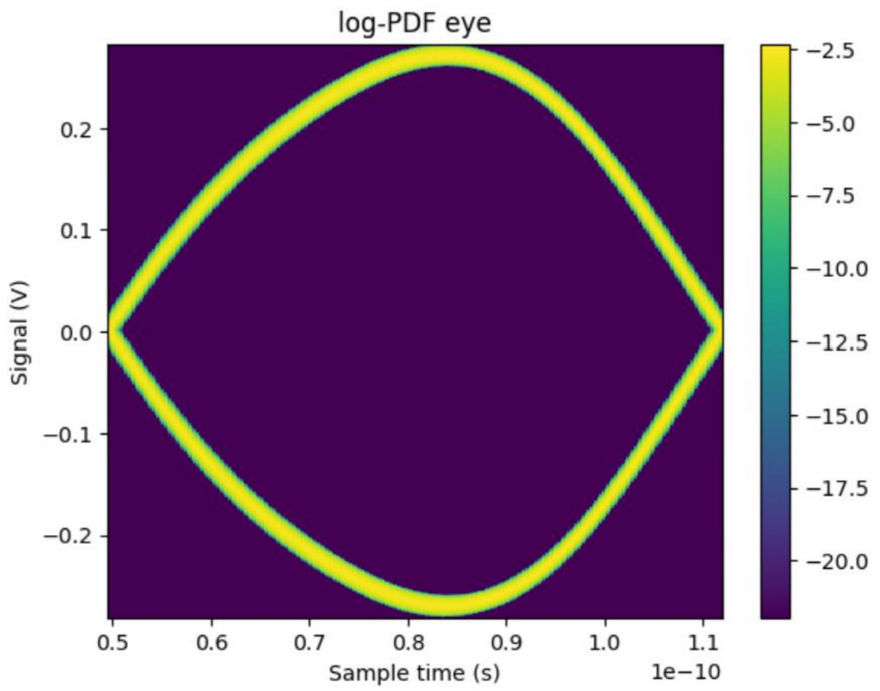
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 59.2% / 4.4%**

2-9-22 ARM Layer D Results:
20%-80% risetime = 23% UI, Cpar = 200fF

Worst Data Eye



Diff. Clock

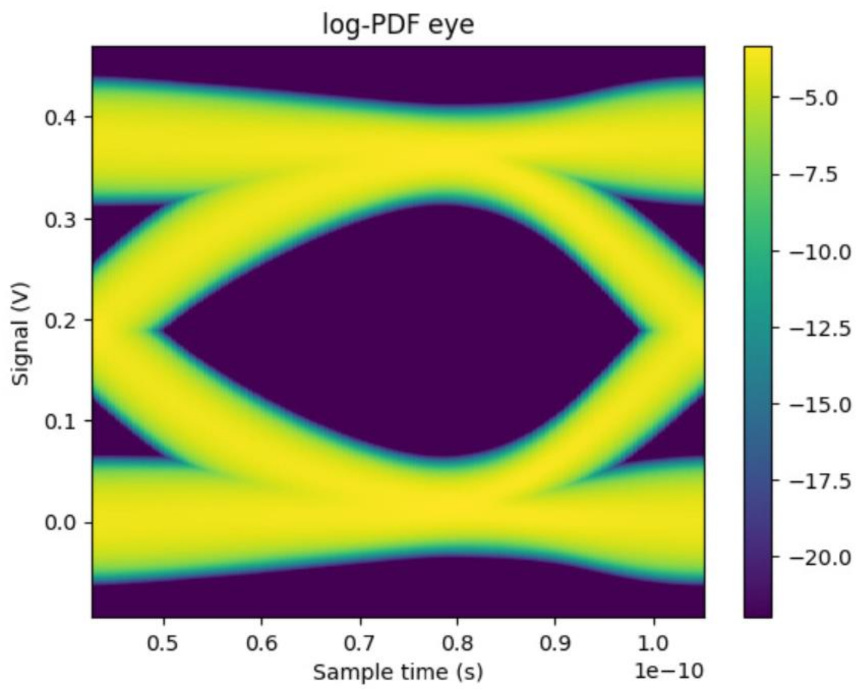


- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 61.2% / 3.6%**

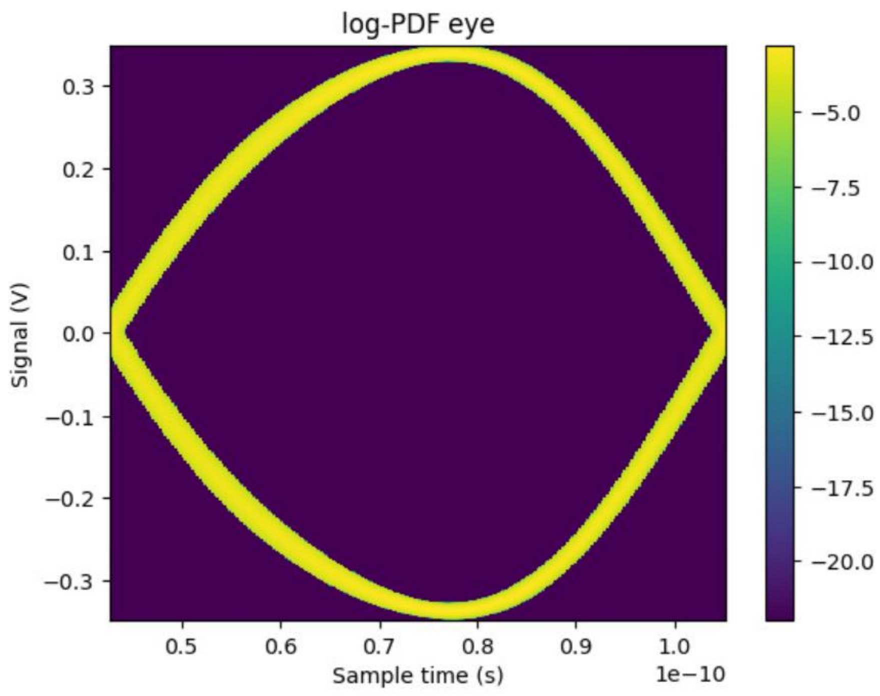
Keysight Results:
20%-80% risetime = 23% UI, Cpar = 250fF

BLUE CHEETAH ANALOG DESIGN

Worst Data Eye



Diff. Clock

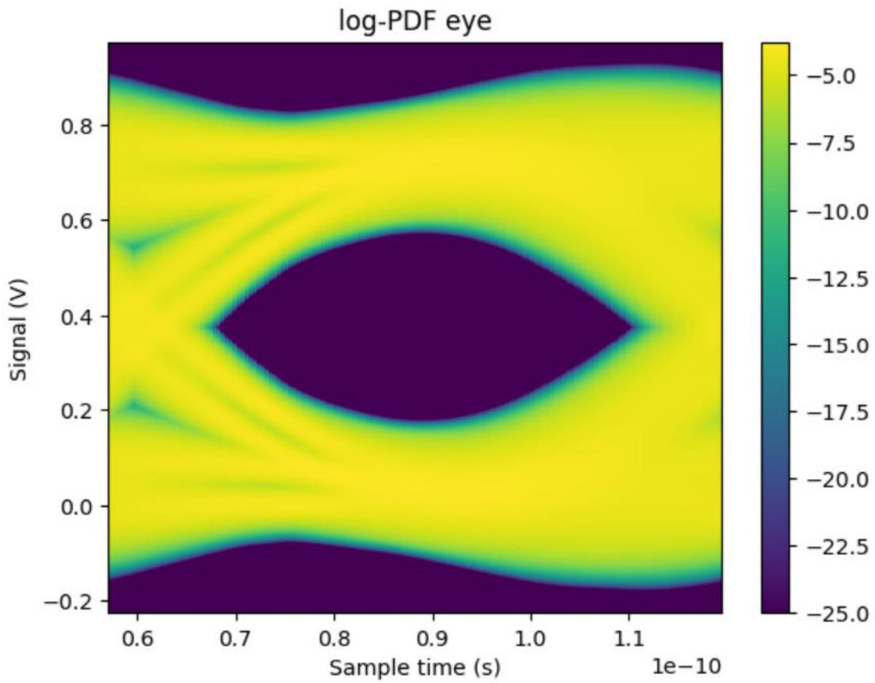


- Worst line timing margin / crosstalk jitter @ 1e-15 BER: 71.6% / 4.8%

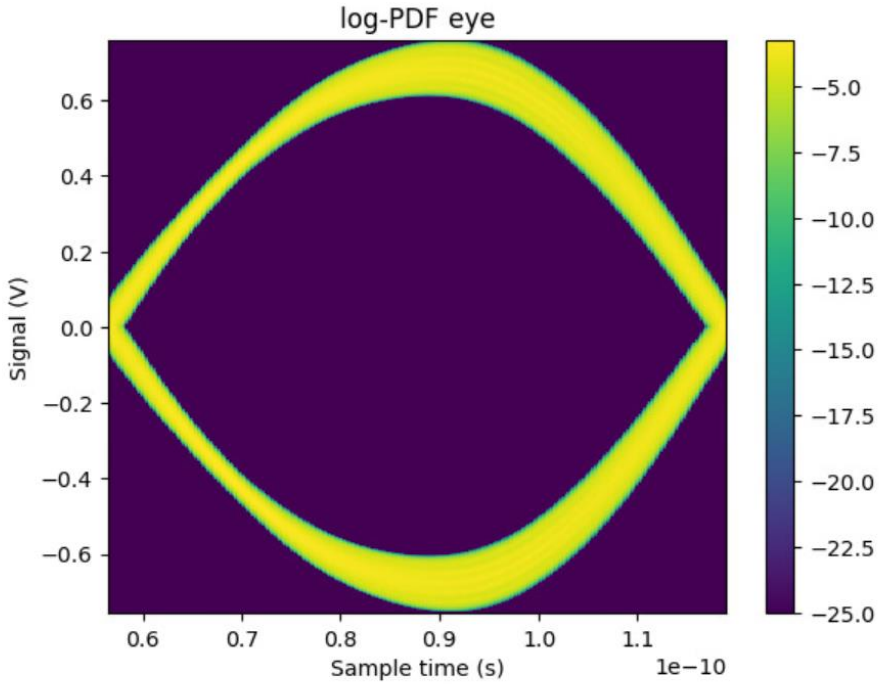
16Gb/s Source Terminated

Full Slice 2mm Results:
20%-80% risetime = 23% UI, Cpar = 200fF

Worst Data Eye



Diff. Clock

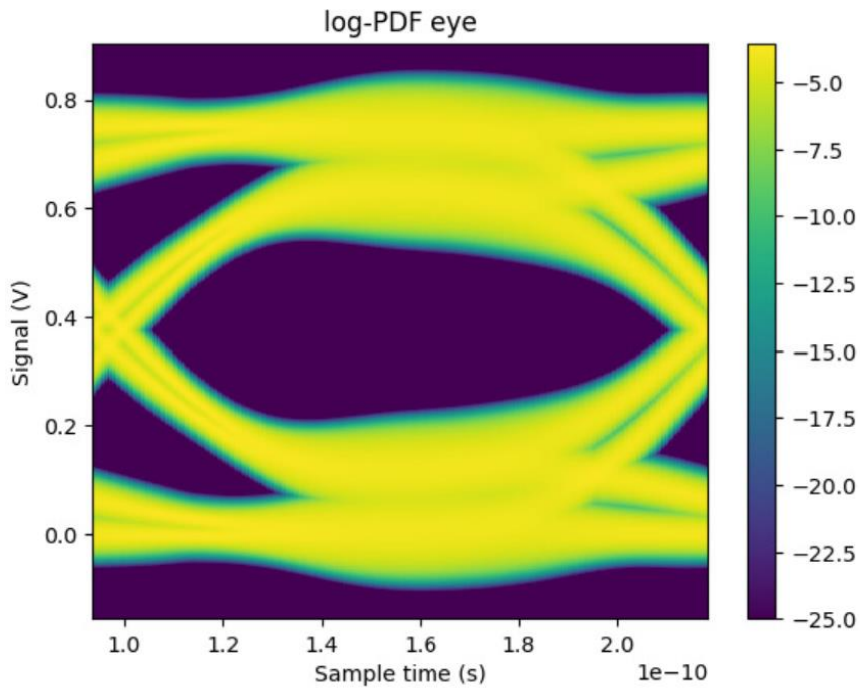


- Worst line timing margin / crosstalk jitter @ 1e-15 BER: 65.6% / 6%

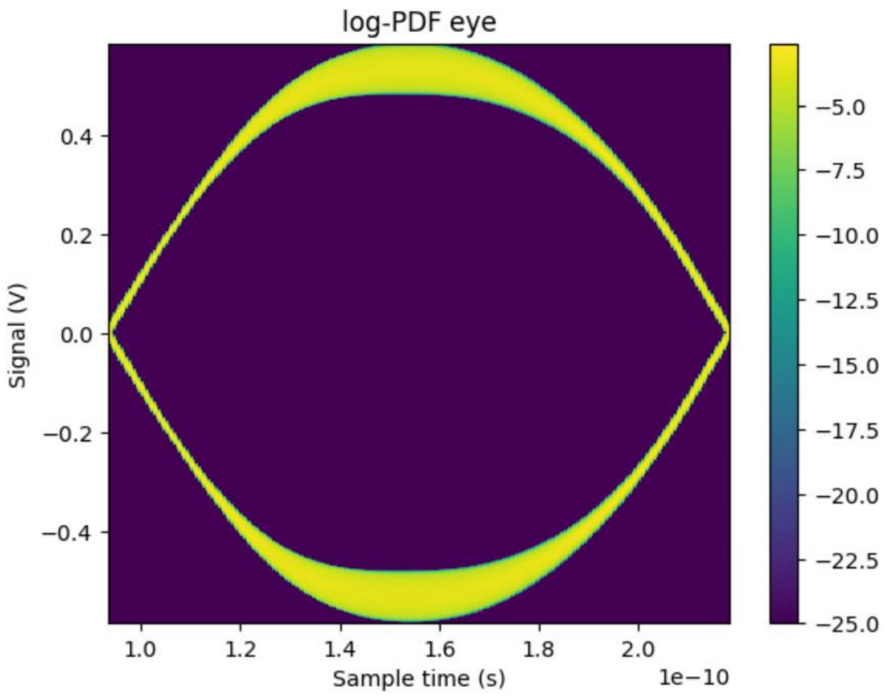
8Gb/s Source Terminated

Full Slice 2mm Results:
20%-80% risetime = 23% UI, Cpar = 500fF

Worst Data Eye



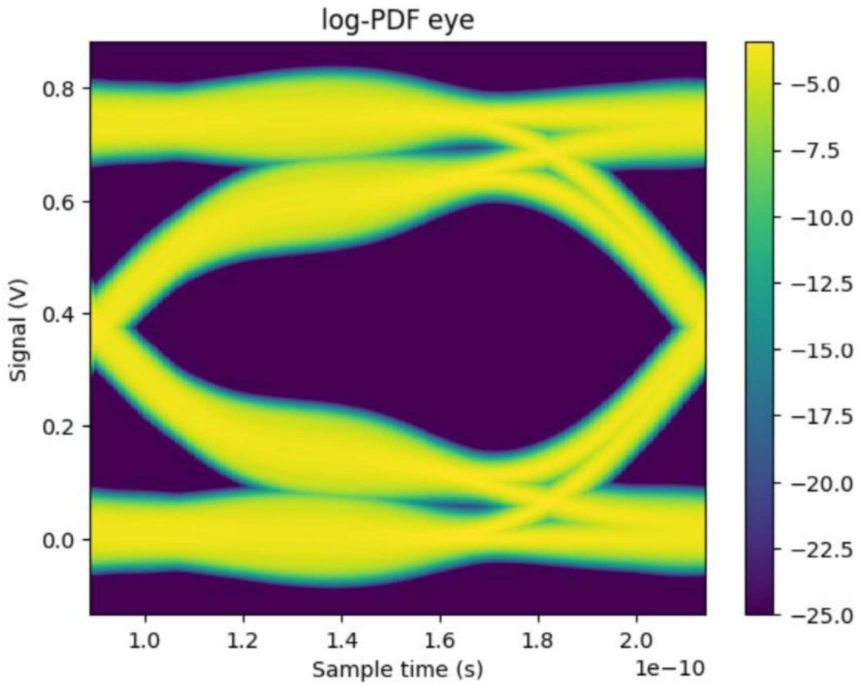
Diff. Clock



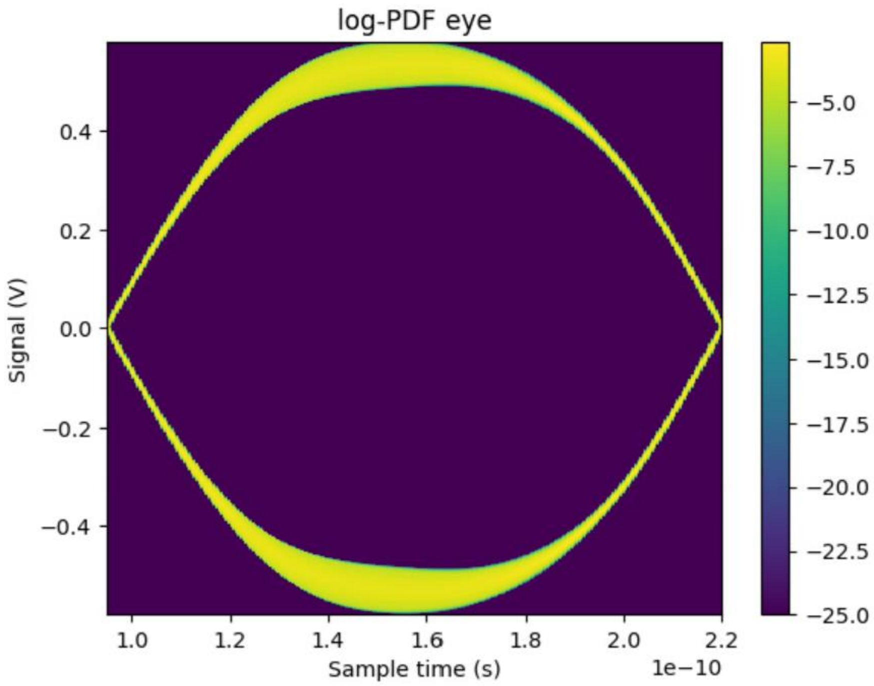
- Worst line timing margin / crosstalk jitter @ 1e-15 BER: 65.6% / 1.6%

Full Slice 2mm Results:
20%-80% risetime = 23% UI, Cpar = 400fF

Worst Data Eye



Diff. Clock

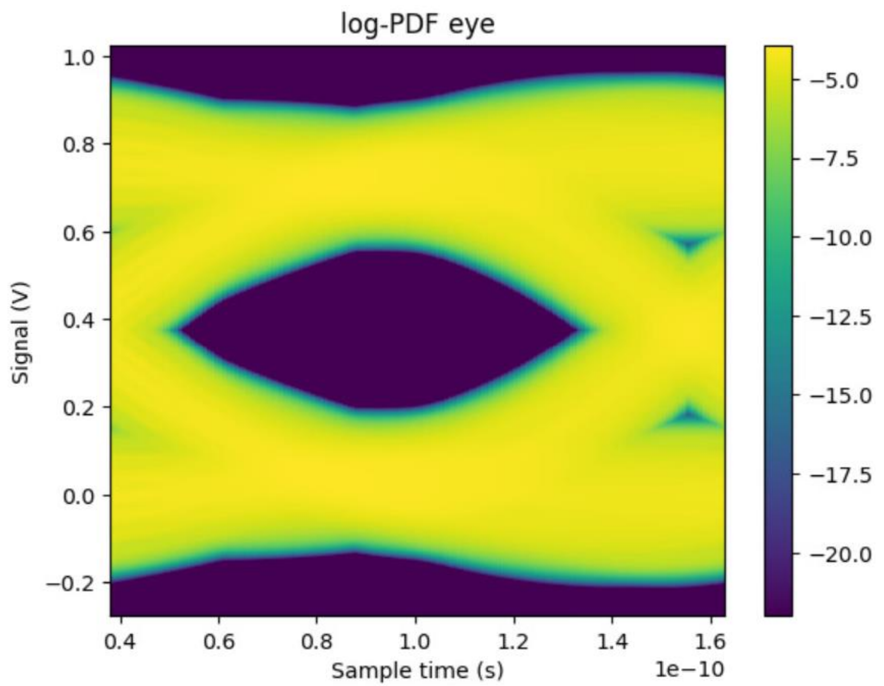


- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 79.6% / 1.2%**

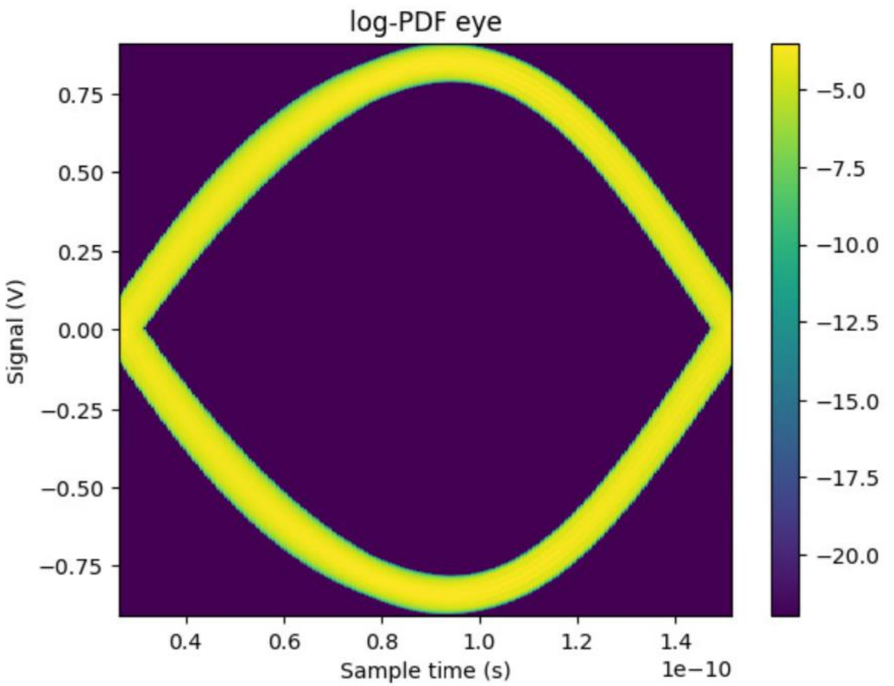
Full Slice 10mm Results:
20%-80% risetime = 23% UI, Cpar = 500fF

BLUE CHEETAH
ANALOG DESIGN

Worst Data Eye



Diff. Clock

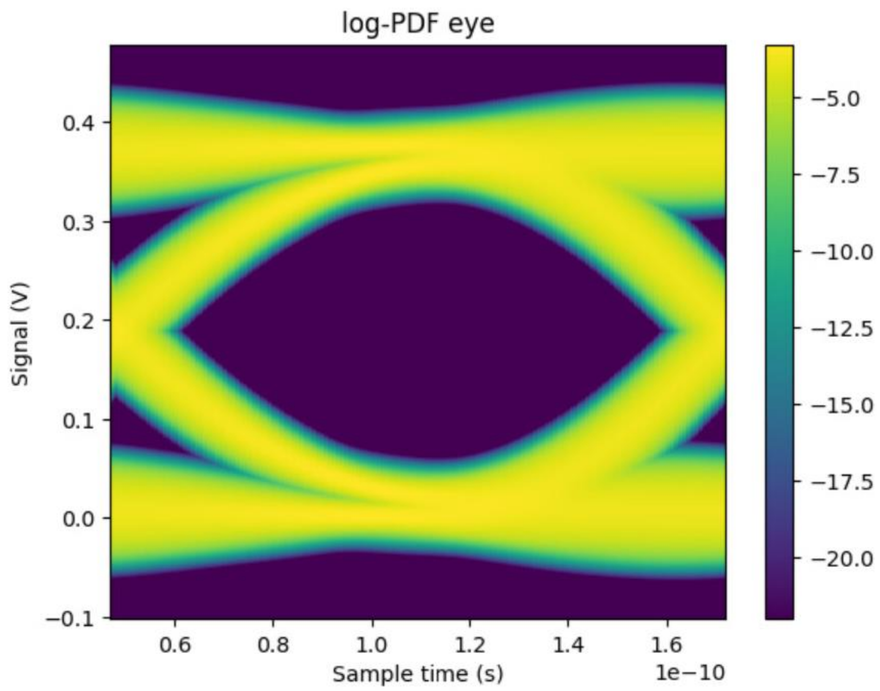


- Worst line timing margin / crosstalk jitter @ 1e-15 BER: 55.2% / 7.6%

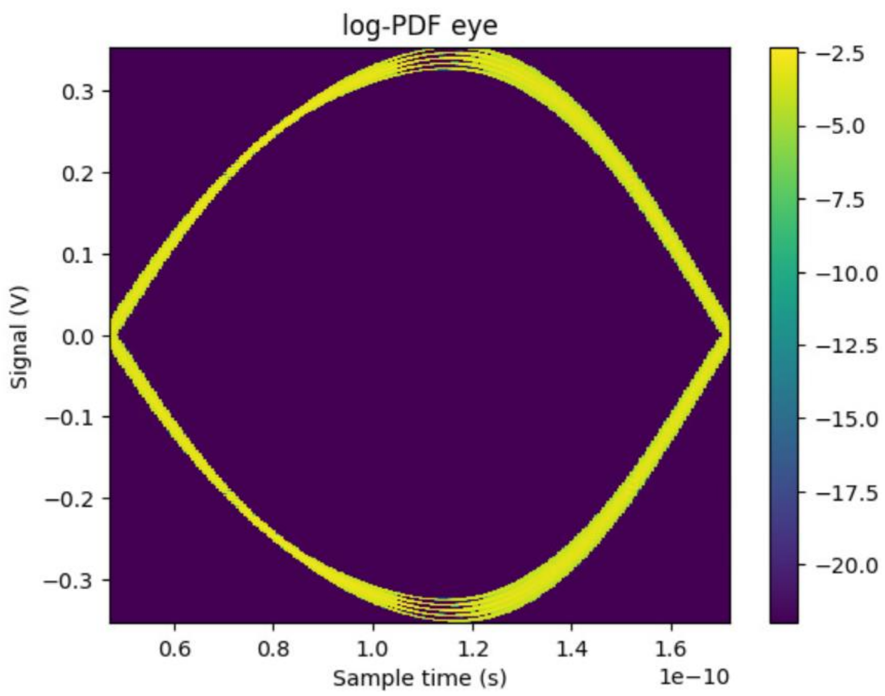
Keysight Results:

20%-80% risetime = 23% UI, Cpar = 500fF

Worst Data Eye



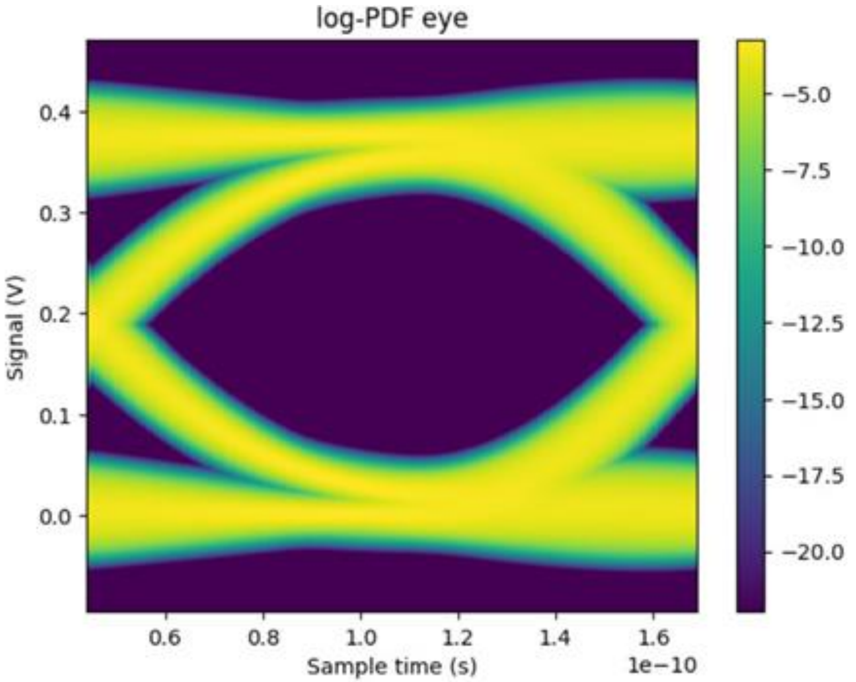
Diff. Clock



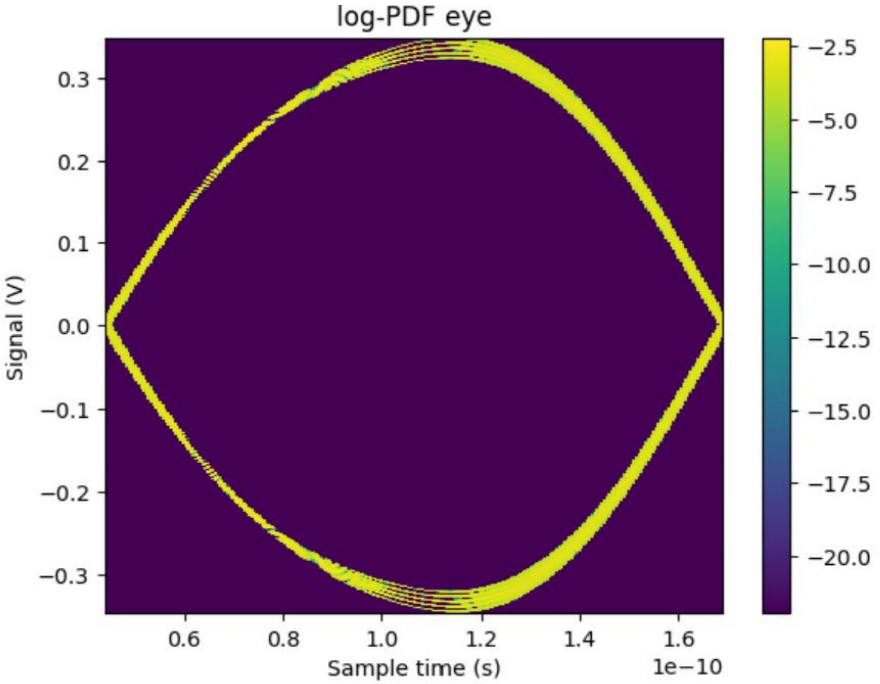
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 61.6% / 2.8%**

Keysight Results:
20%-80% risetime = 23% UI, Cpar = 400fF

Worst Data Eye



Diff. Clock

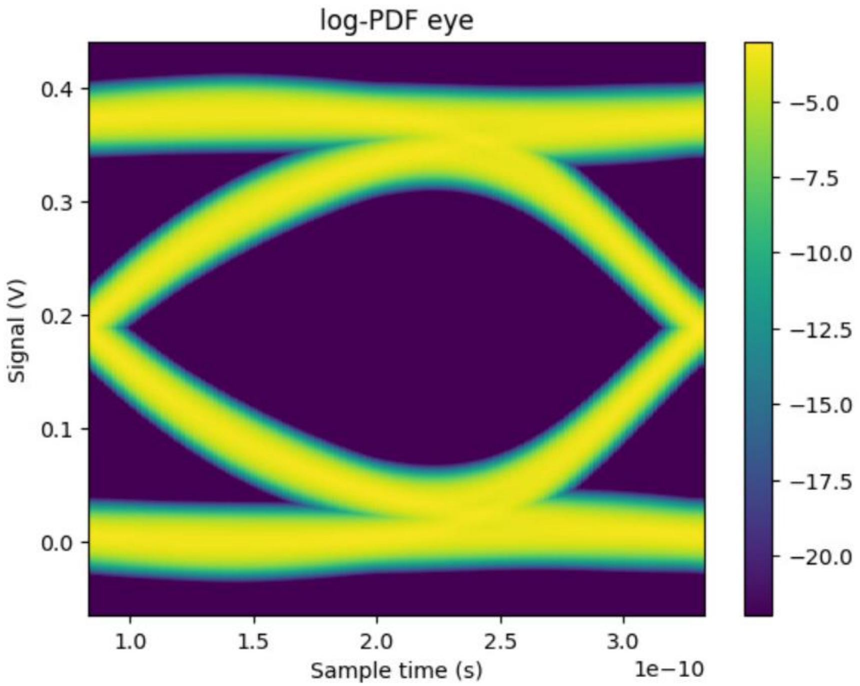


- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 64.4% / 2%**

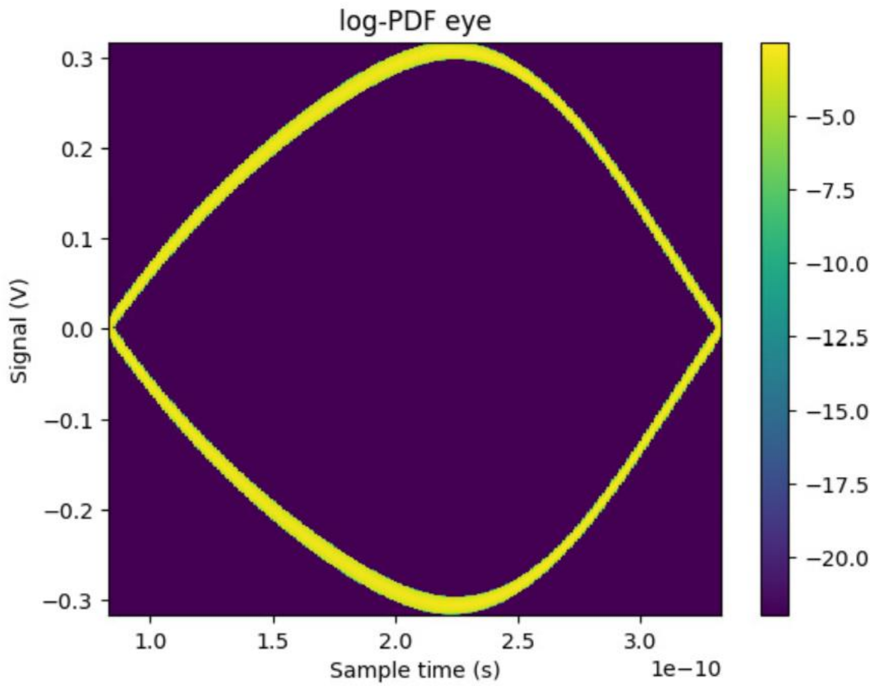
4Gb/s Doubly Terminated

Full Slice 25mm Results:
20%-80% risetime = 23% UI, Cpar = 1pF

Worst Data Eye



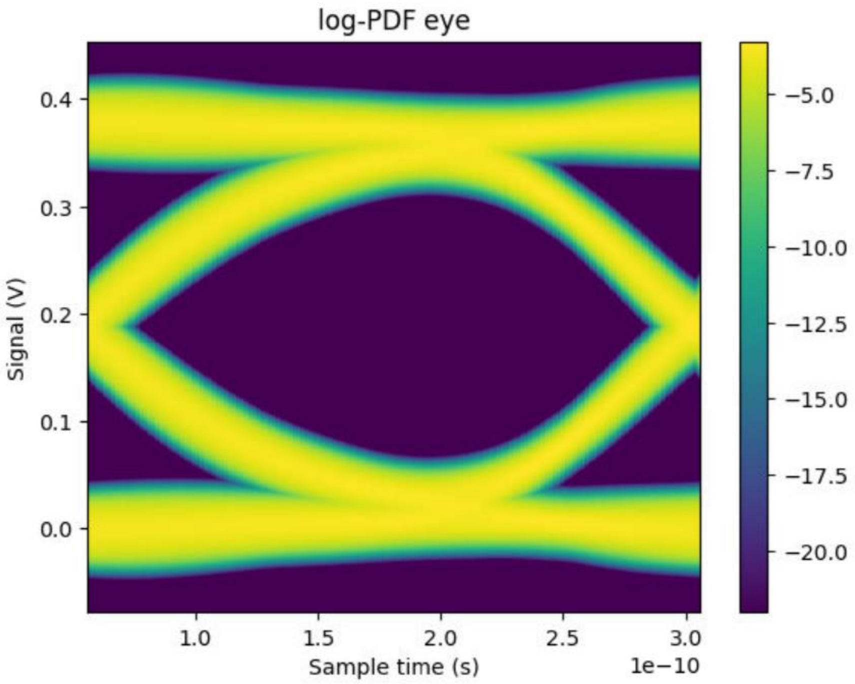
Diff. Clock



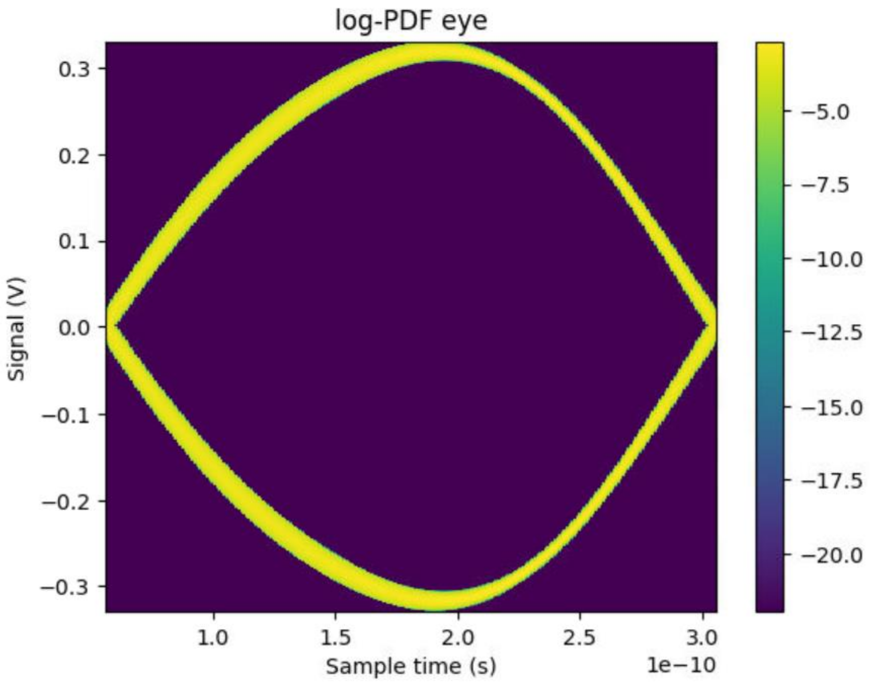
- Worst line timing margin / crosstalk jitter @ 1e-15 BER: 73.2% / 2%

ARM Layer D Results:
20%-80% risetime = 23% UI, Cpar = 1pF

Worst Data Eye



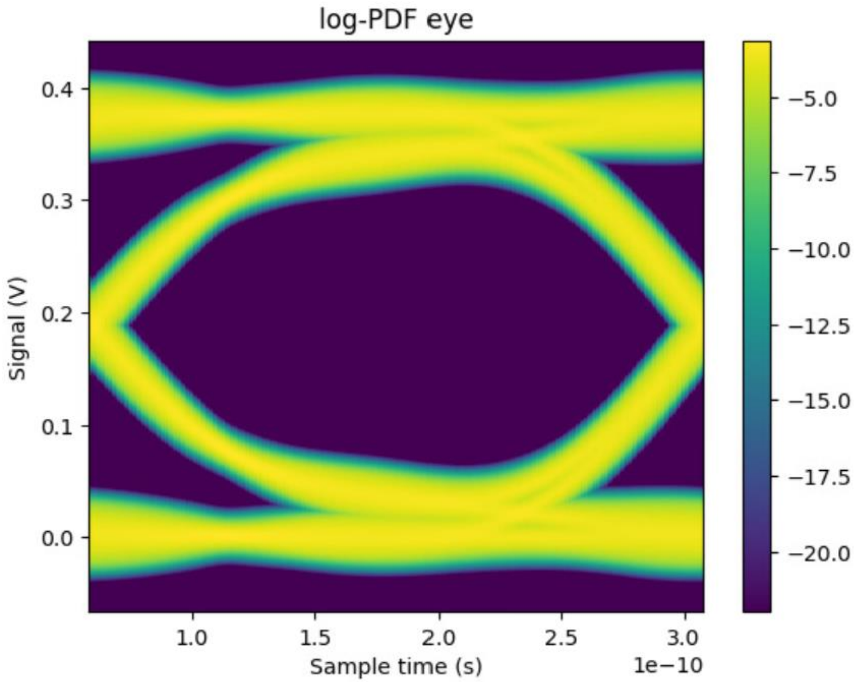
Diff. Clock



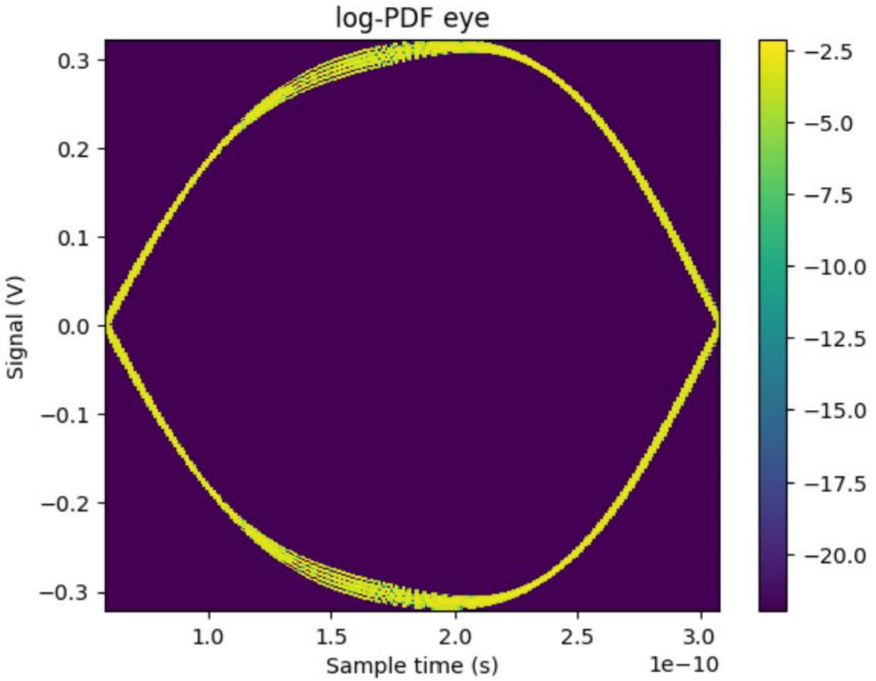
- Worst line timing margin / crosstalk jitter @ 1e-15 BER: 71.2% / 3.2%

Keysight Results:
20%-80% risetime = 23% UI, Cpar = 1pF

Worst Data Eye



Diff. Clock

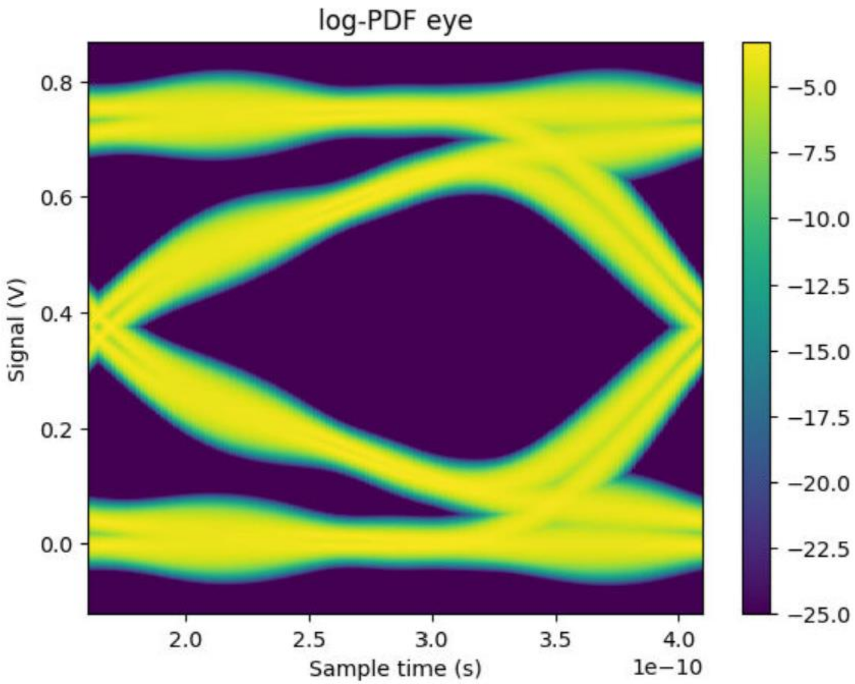


- Worst line timing margin / crosstalk jitter @ 1e-15 BER: 78% / 1.6%

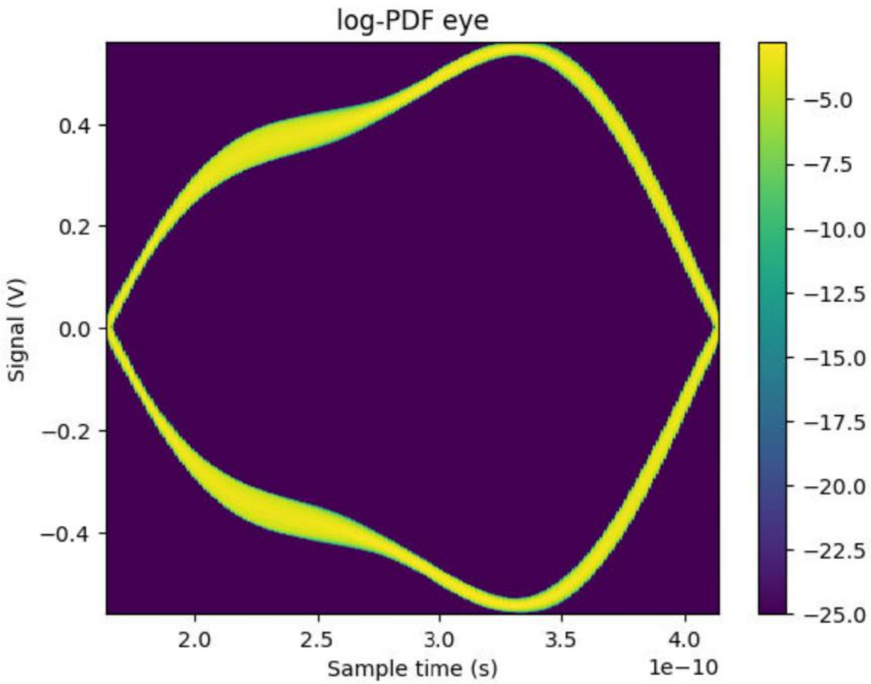
4Gb/s Source Terminated

Full Slice 2mm Results:
20%-80% risetime = 23% UI, Cpar = 1pF

Worst Data Eye



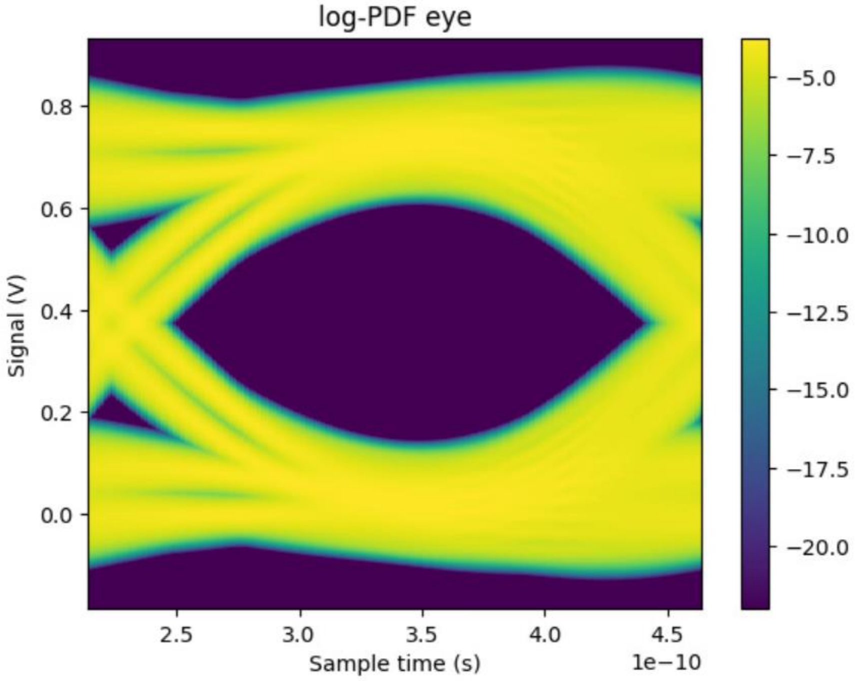
Diff. Clock



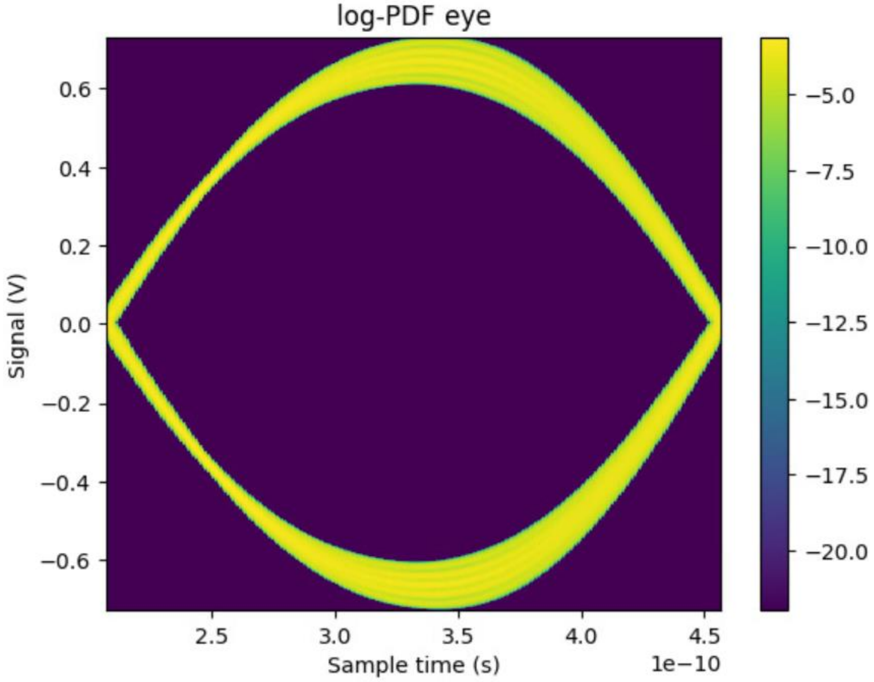
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 63.2% / 2%**

Full Slice 10mm Results:
20%-80% risetime = 23% UI, Cpar = 1pF

Worst Data Eye



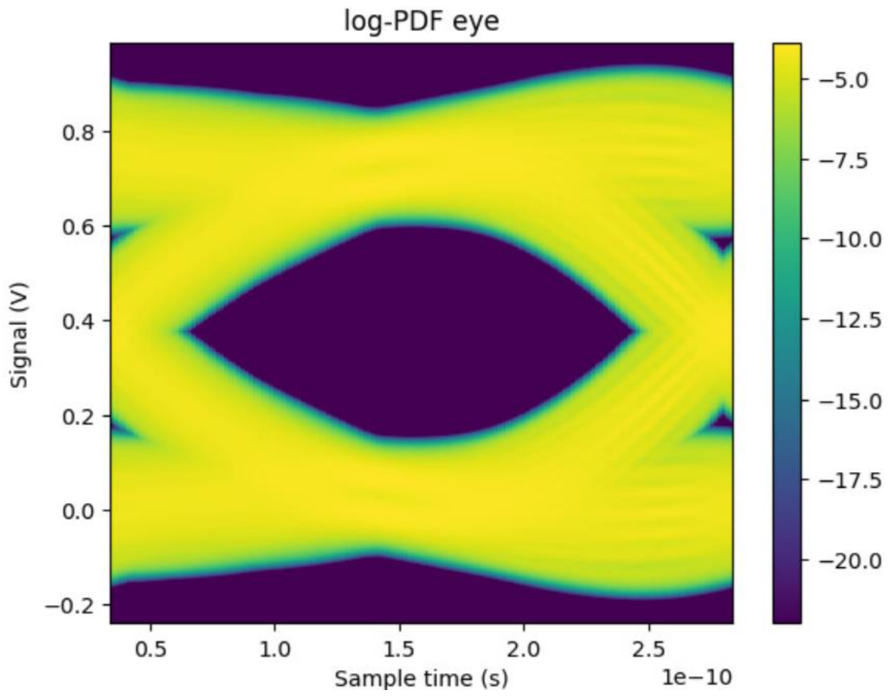
Diff. Clock



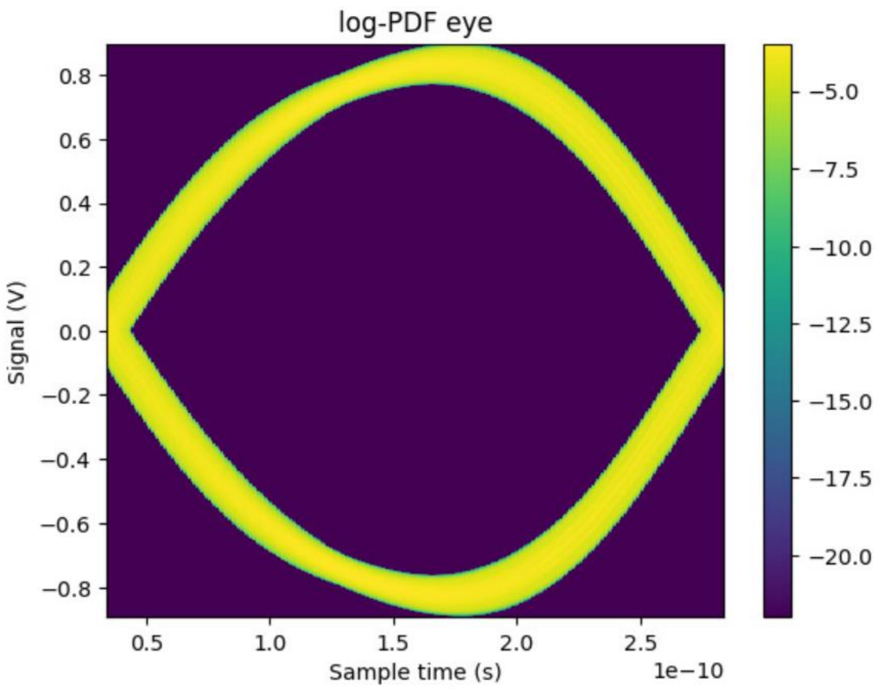
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 63.6% / 3.6%**

ARM Layer A Results:
20%-80% risetime = 23% UI, Cpar = 1pF

Worst Data Eye



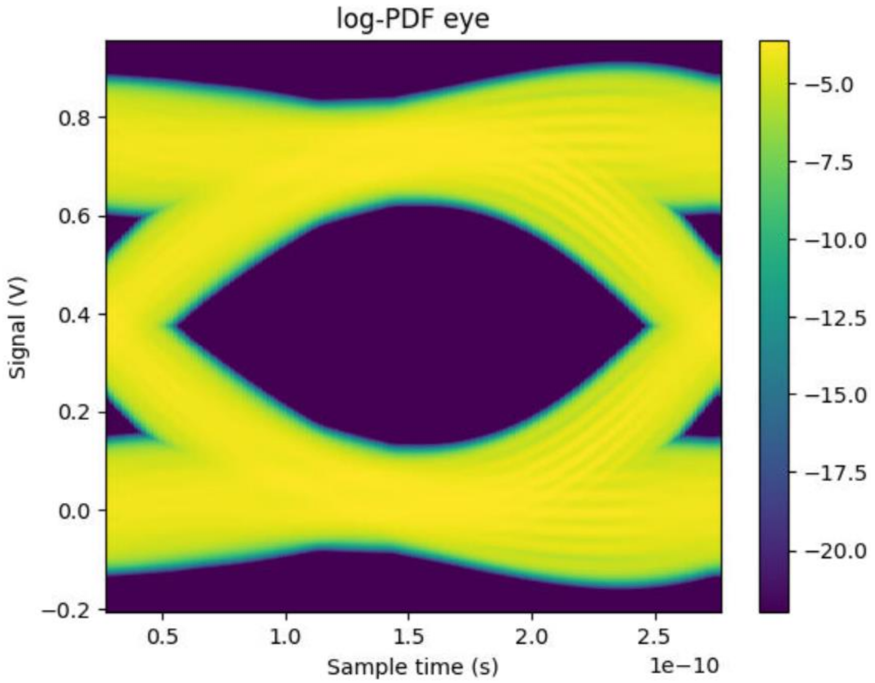
Diff. Clock



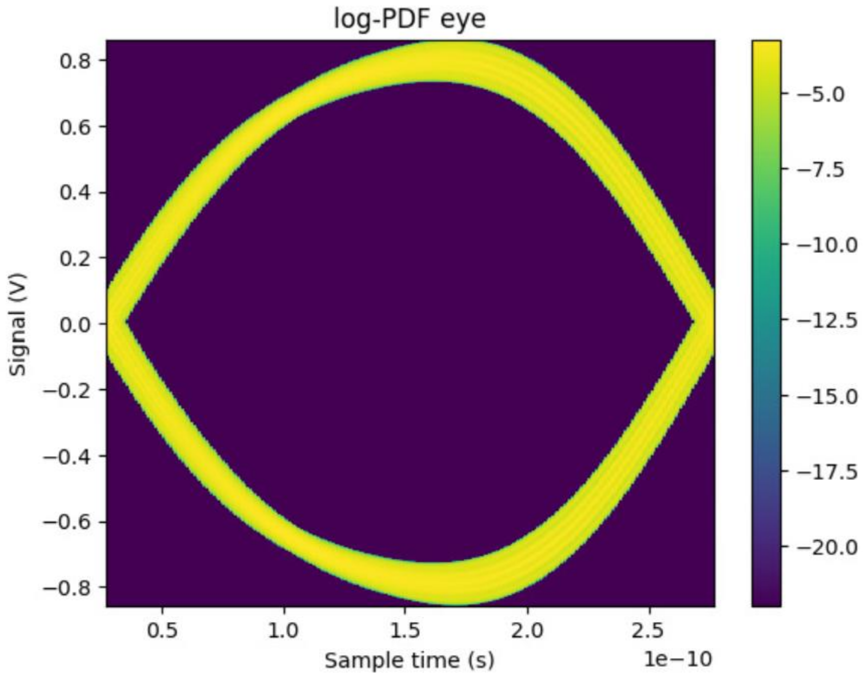
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 56.8% / 8%**

(2-9-2022) ARM Layer A Results: 20%-80% risetime = 23% UI, Cpar = 800fF

Worst Data Eye



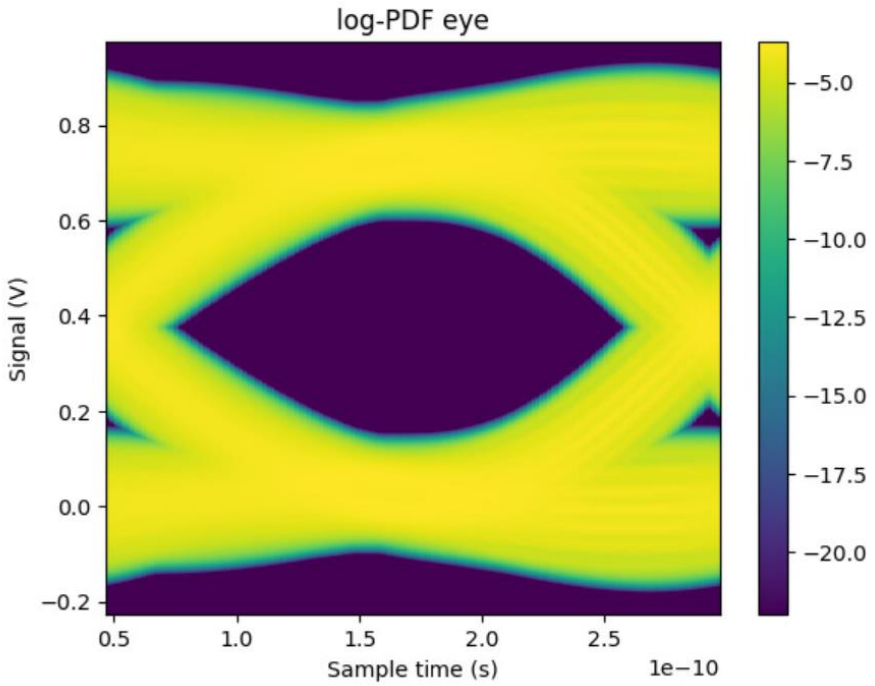
Diff. Clock



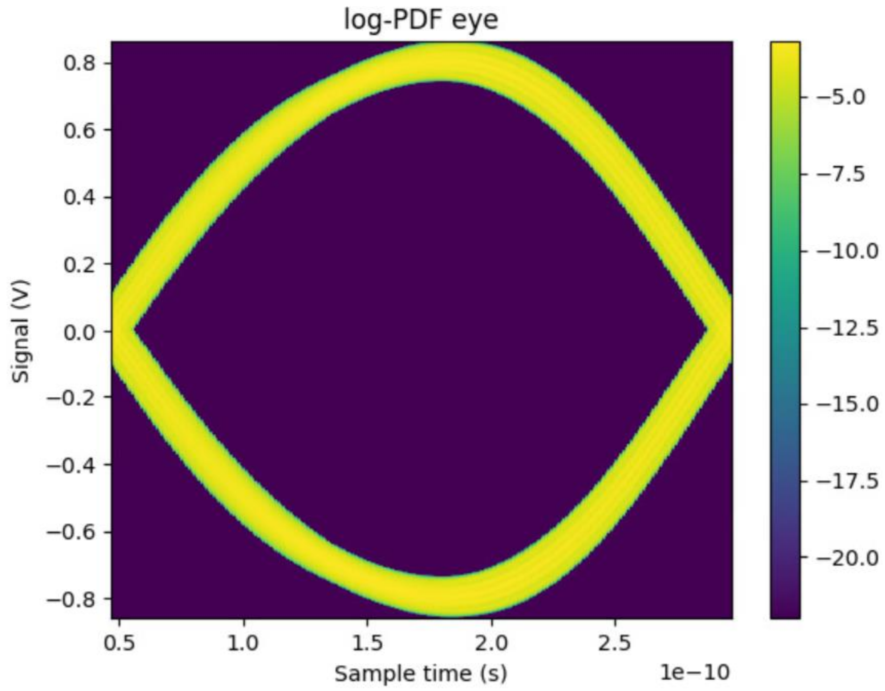
- Worst line timing margin / crosstalk jitter @ 1e-15 BER: 62.8% / 6.4%

(2-9-2022) ARM Layer C Results:
20%-80% risetime = 23% UI, Cpar = 800fF

Worst Data Eye



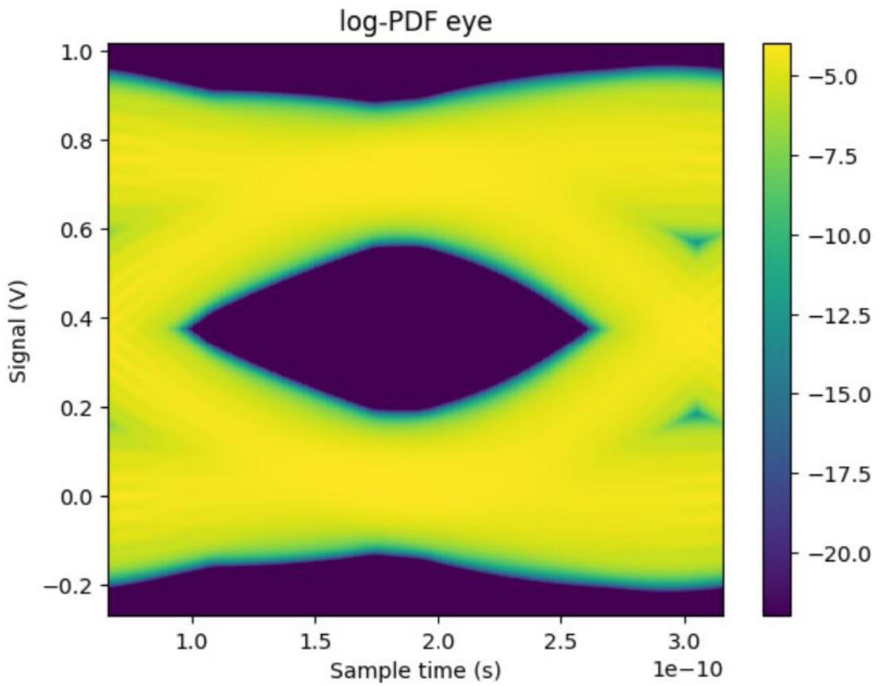
Diff. Clock



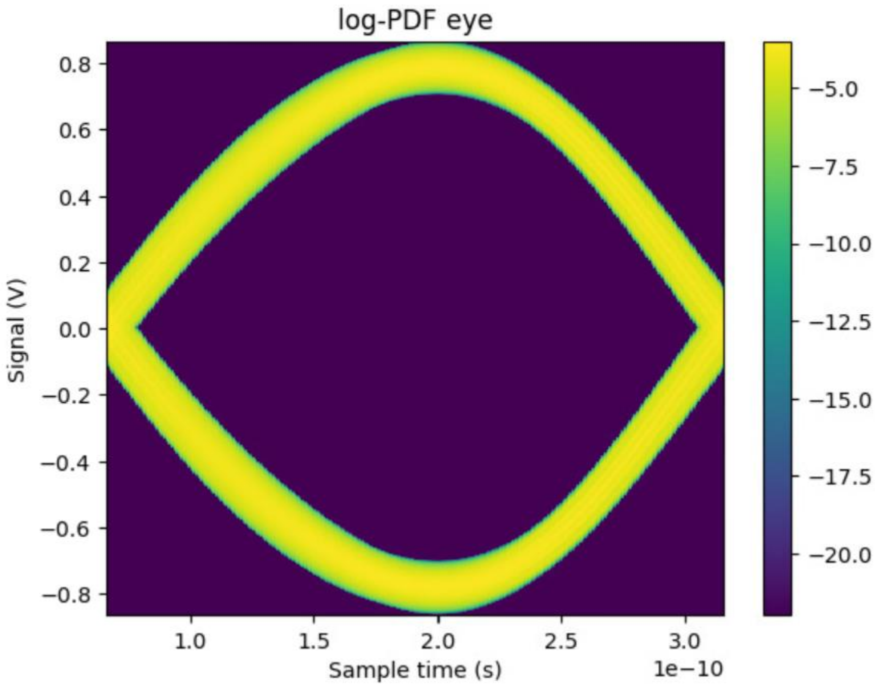
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 58% / 7.6%**

ARM Layer D Results:
20%-80% risetime = 23% UI, Cpar = 1pF

Worst Data Eye



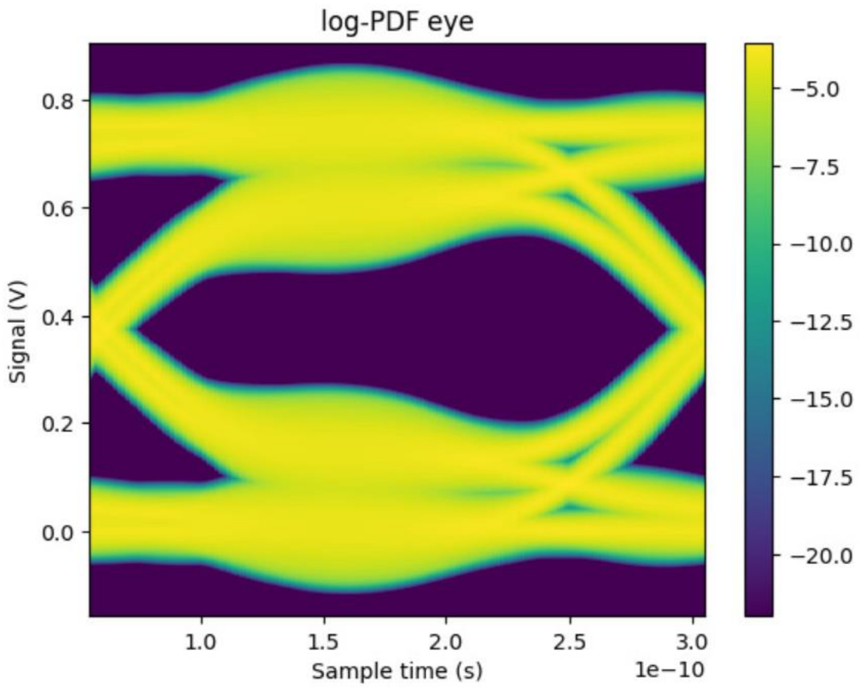
Diff. Clock



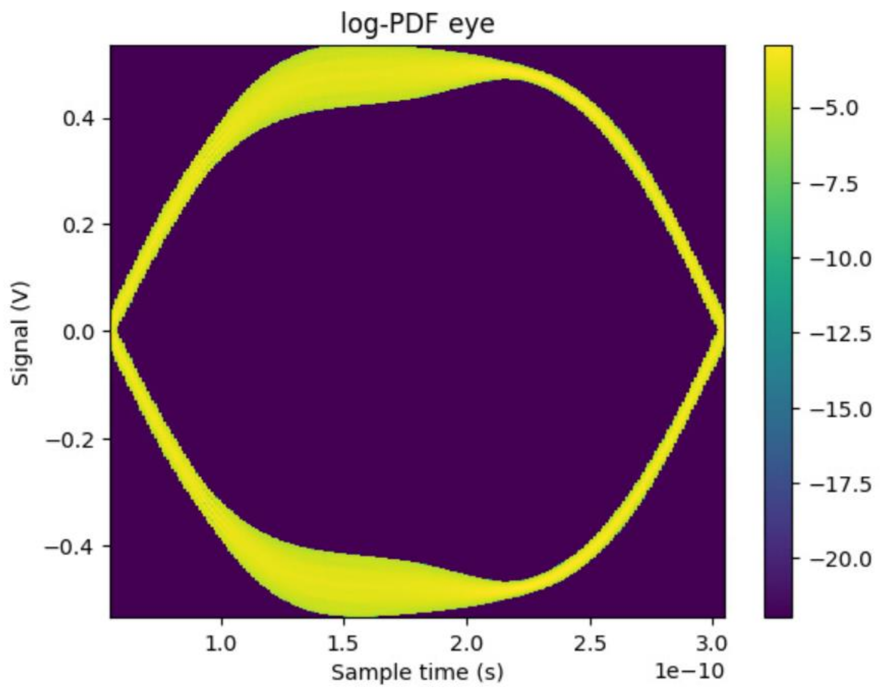
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 48.8% / 9.6%**

Keysight Results:
20%-80% risetime = 23% UI, Cpar = 1pF

Worst Data Eye



Diff. Clock



- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 71.2% / 2.4%**