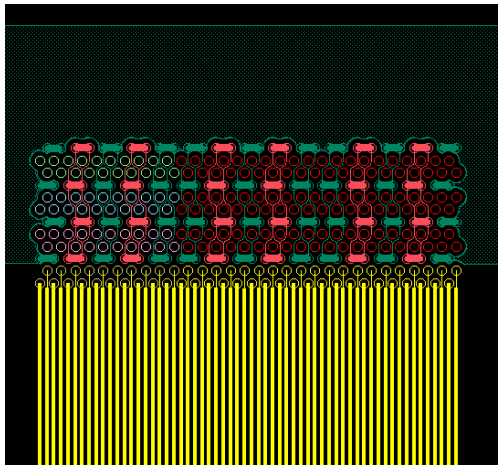
BOW 4slices_3stacks channel

- V1.5

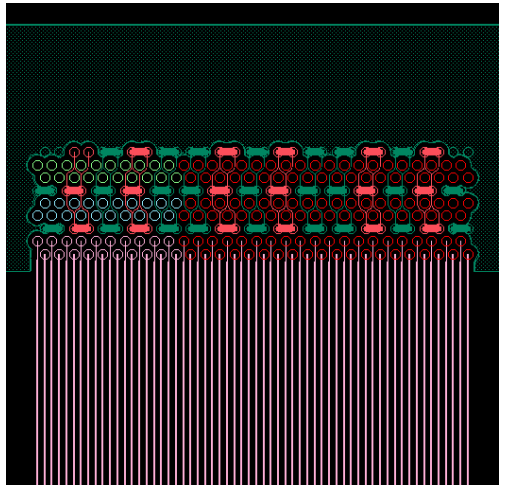
BOW models introduction.

- This analysis has been done on a BOW channel that contains 3 stacks of 4 slices deep.
- 40 ports models have been generated for slice A (layer 2), slice B (layer 4) and slice D (layer 8)
- Package type
  - Stack-up: 8-2-8 (4 slices deep)
  - Build-up material:ABF-GXT31
  - Build-up thickness:30um
  - Metal thickness:15um
  - Trace width: 21um
- Routing strategy:
  - Signal routing is done in Layer 2,4,6 and 8 for slice A, B,C and D
    - All Slices are striplines.
    - The signal routing has been done to have direct connections between the 2 dies (straight lines: see slide 3 &4)
  - Ground planes are in layer 1,3,5,7 and 9
  - VDD plane is in layer 10

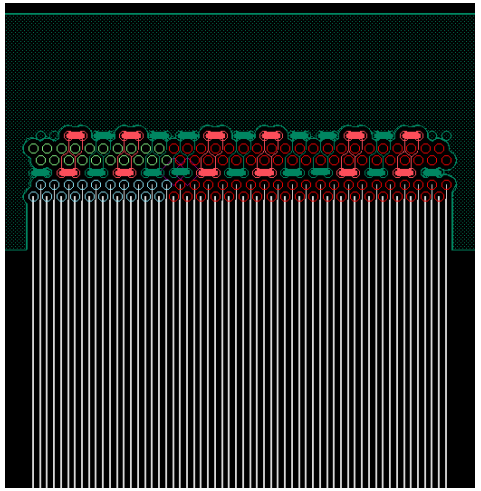
Layout samples



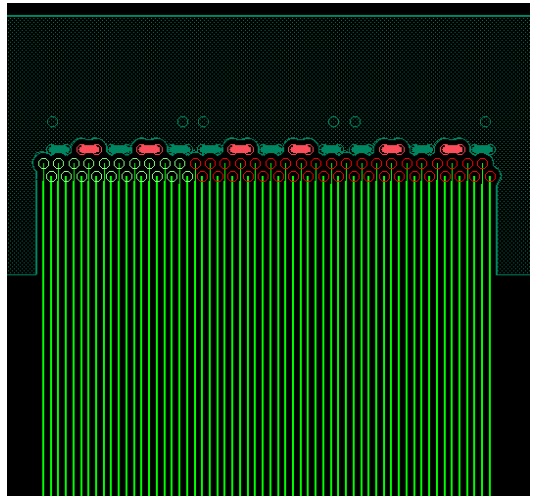
Layer 2



Layer 4

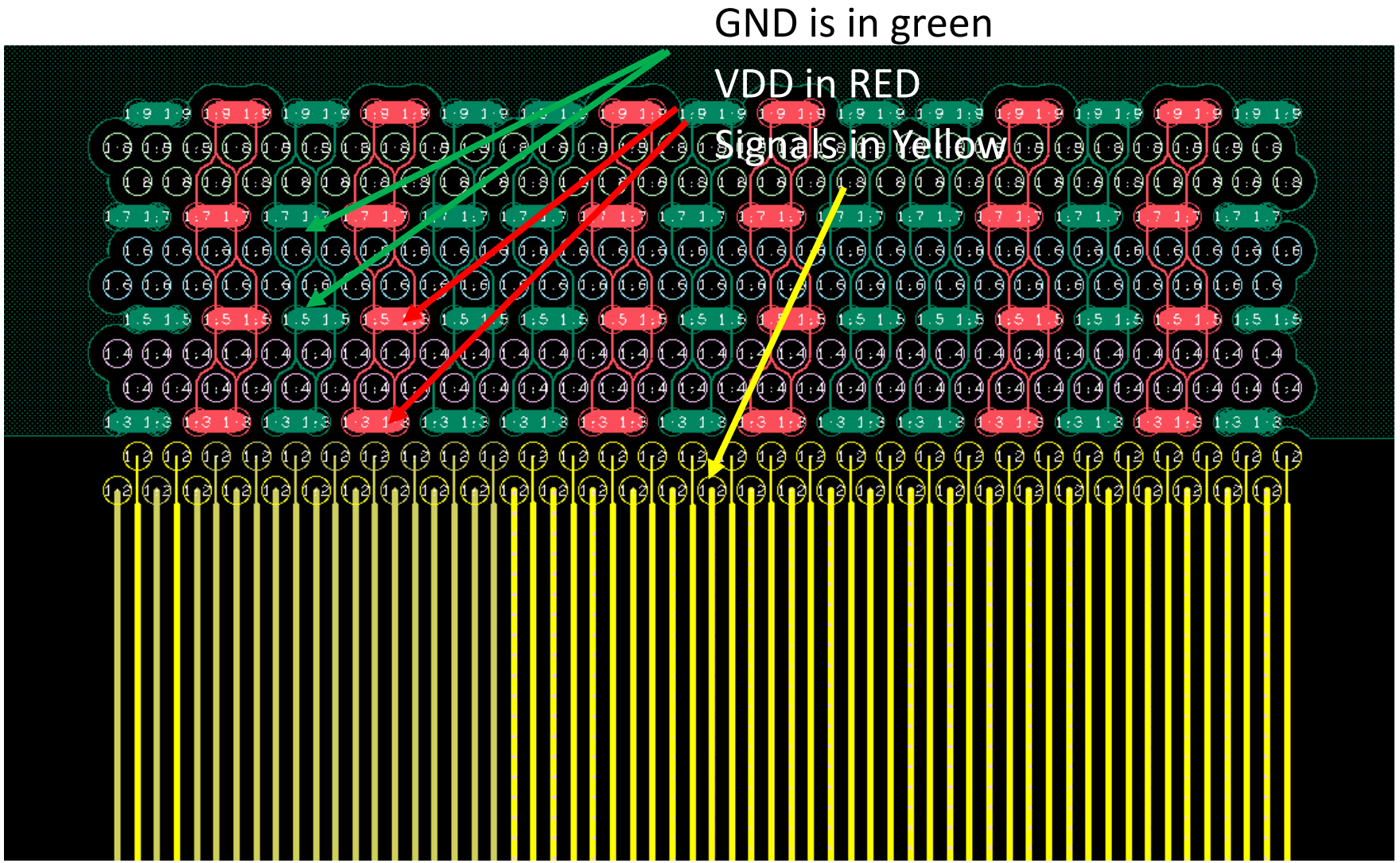


Layer 6



Layer 8

Layout samples (zoom on Slice A)



BOW Channel models

- Slide 28 summary table is based on February 1st optimized Channel model.
  - These models are an optimized version of the January 19th
- Slide 7 to 27 are still based on January 19th models
  - The S-parameters and eye diagram curves have not been updated
    - S-parameters are very similar between these 2 models.

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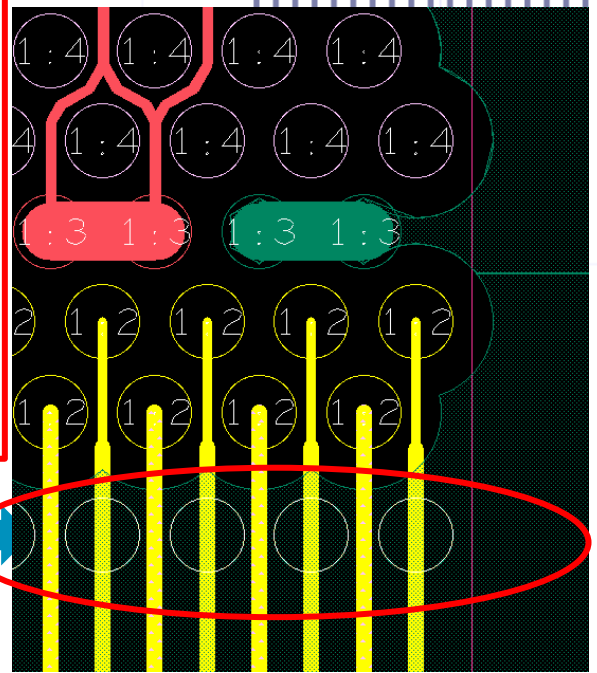
20mm wire length channel: S parameter results

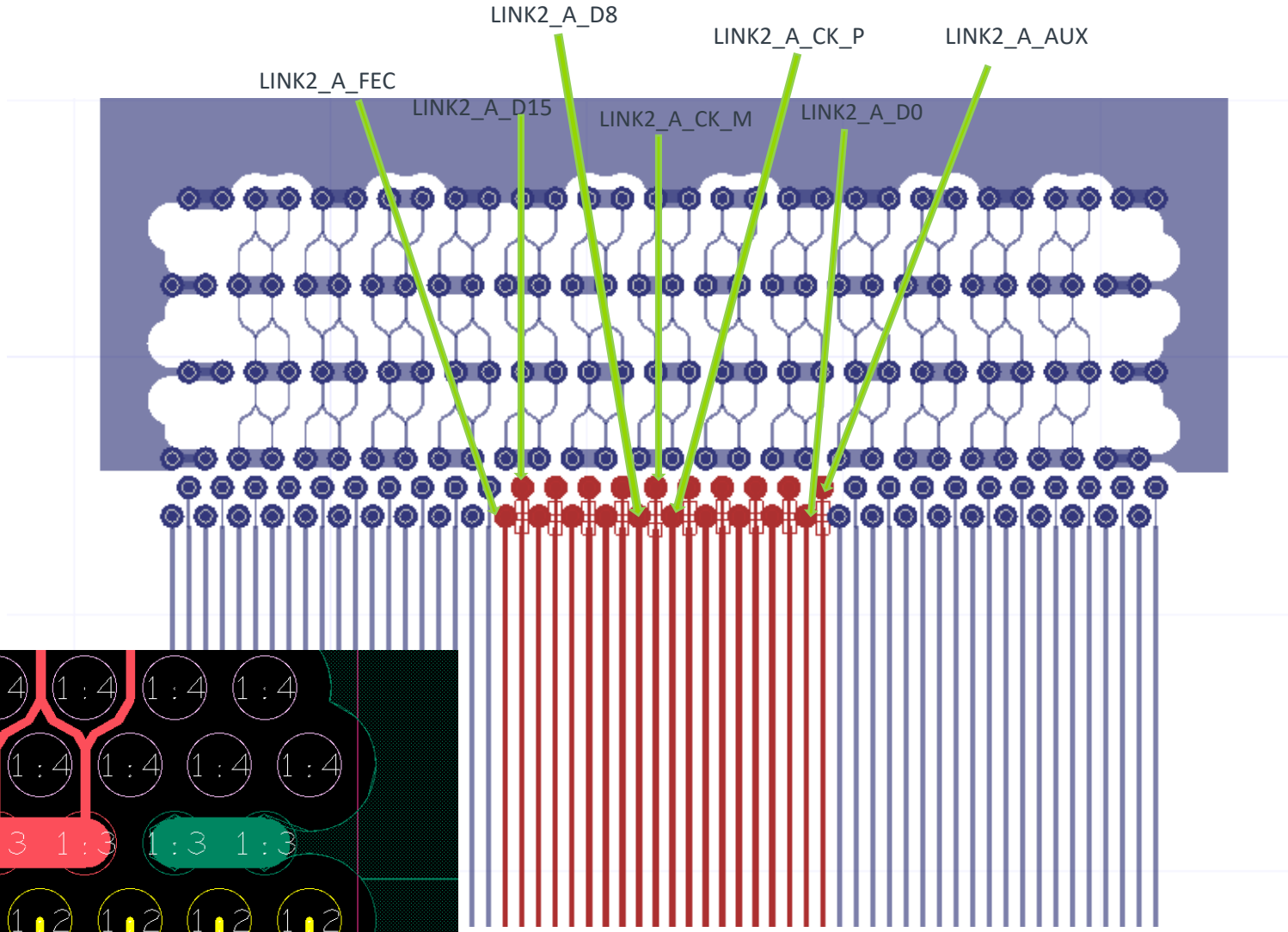
Slice A layout (layer 2)

- 3 stacks layout.
- Models created for the middle stack (40 ports model)

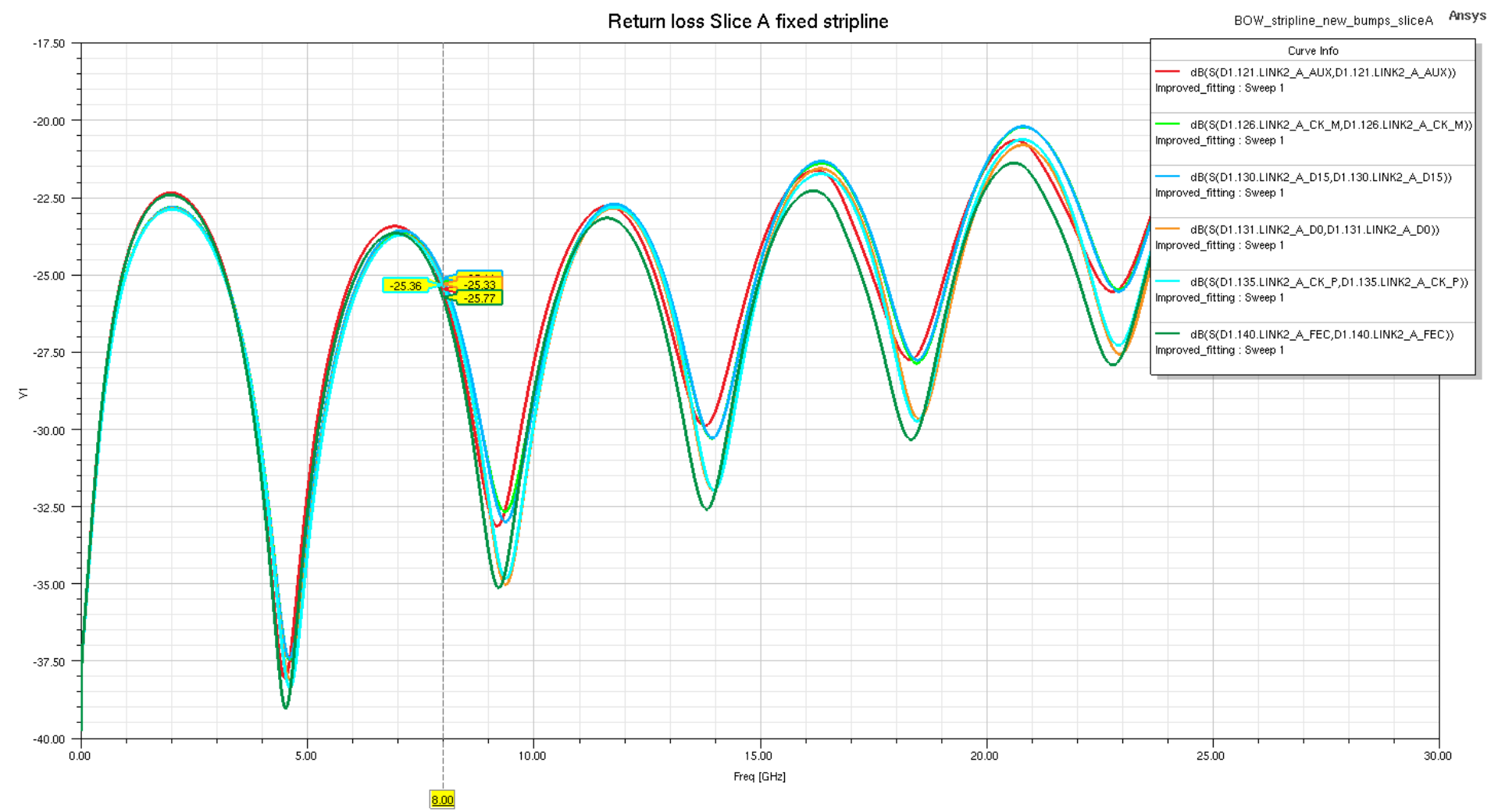
- **Important notice:** To have a good return path, it is important to have extra VSS bumps on layer 1, close to Slice A signal pads.
  If not, it will have a big impact on Slice A performances (see picture on the right)
  - Extra GND bumps on Layer 1 are highlighted in red.
  - This is just an example, other configurations to add GND bumps can be considered



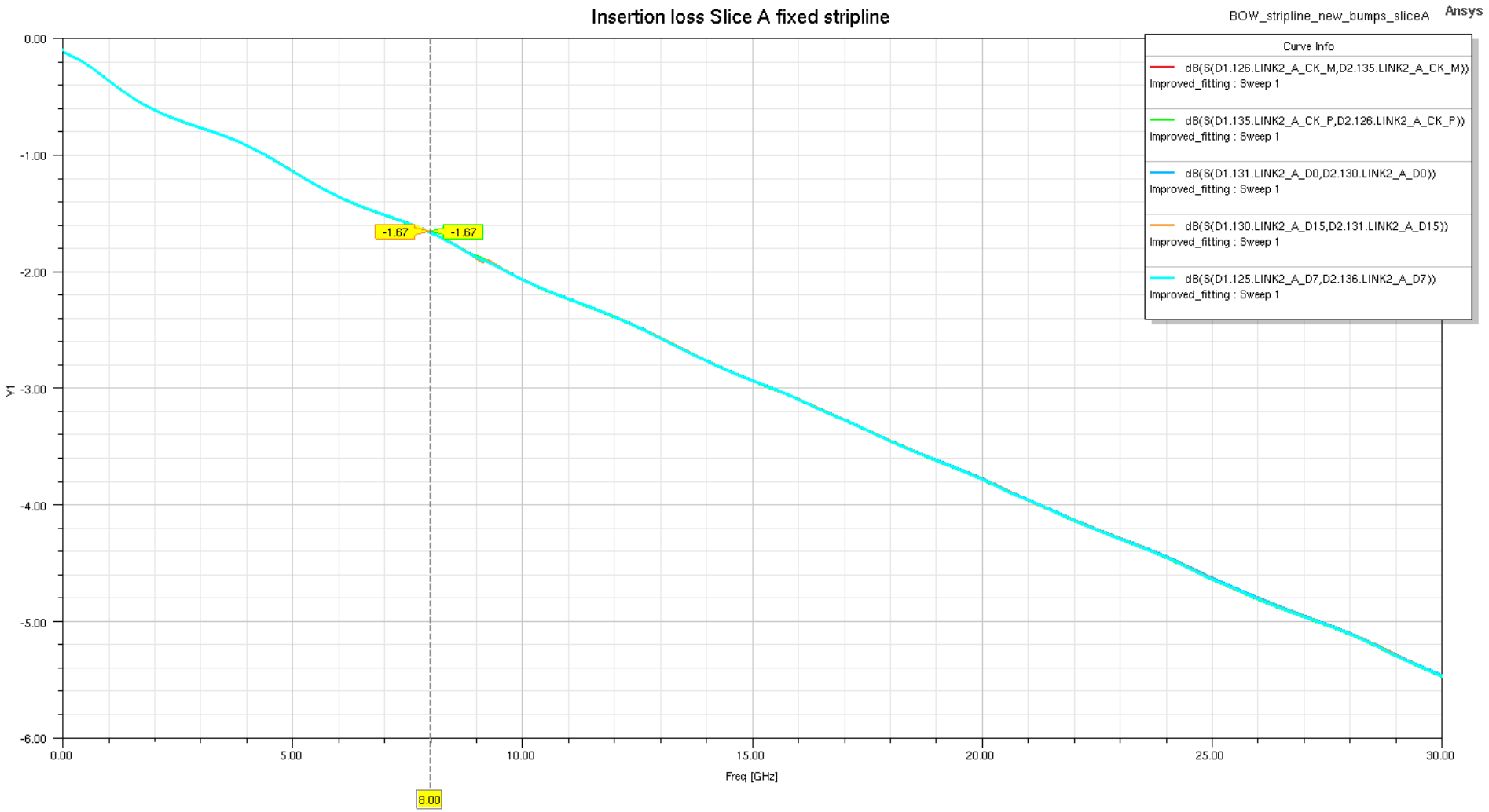
Extra GND bumps



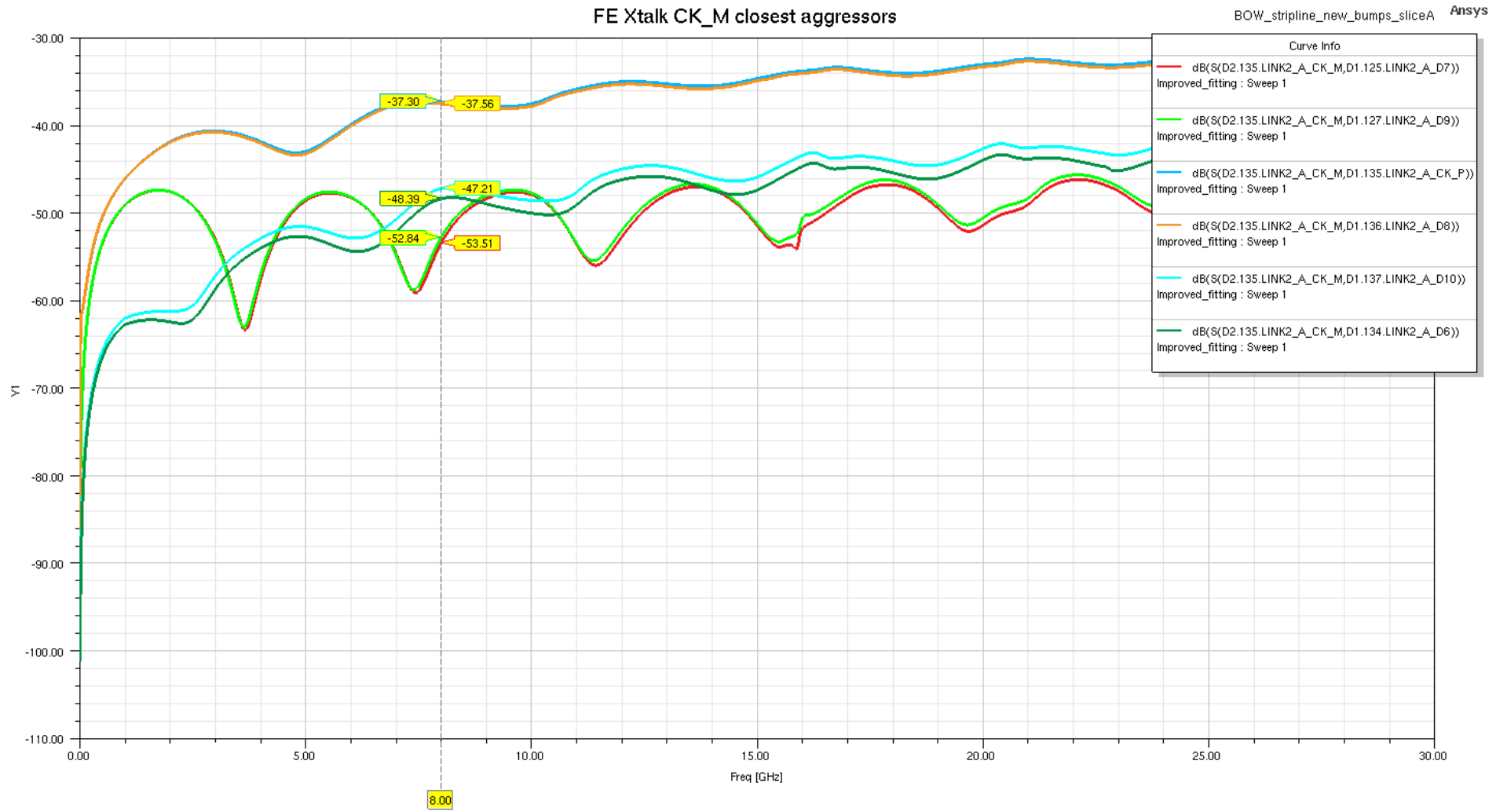
Return Loss Slice A stripline(layer2) -19/01 models



Insertion Loss Slice A stripline (layer2) -19/01 models

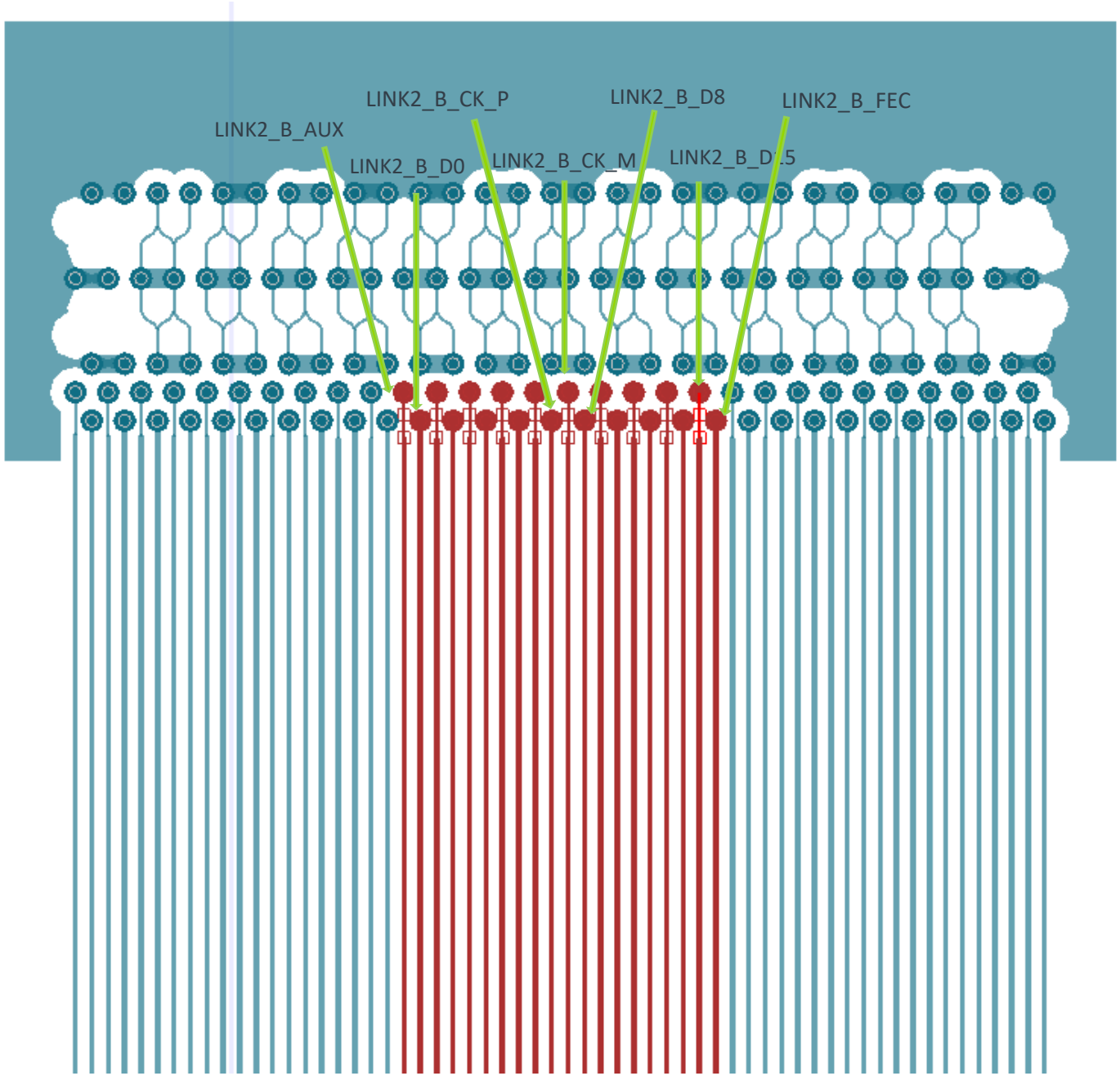


Far end Xtalk with A_CK_M victim (Stripline -layer2) – Only close aggressors -19/01 models

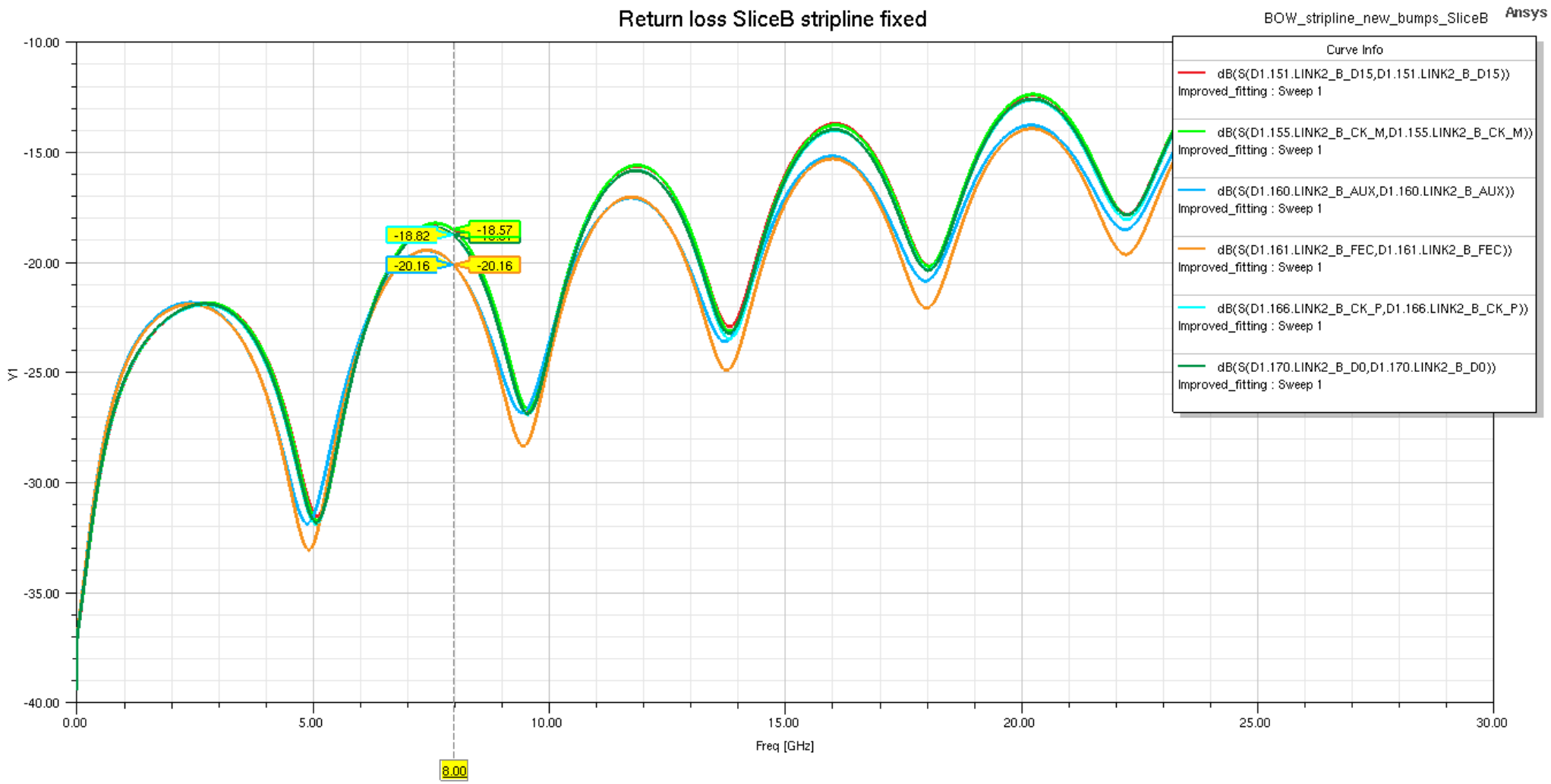


Slice B layout (layer 4)

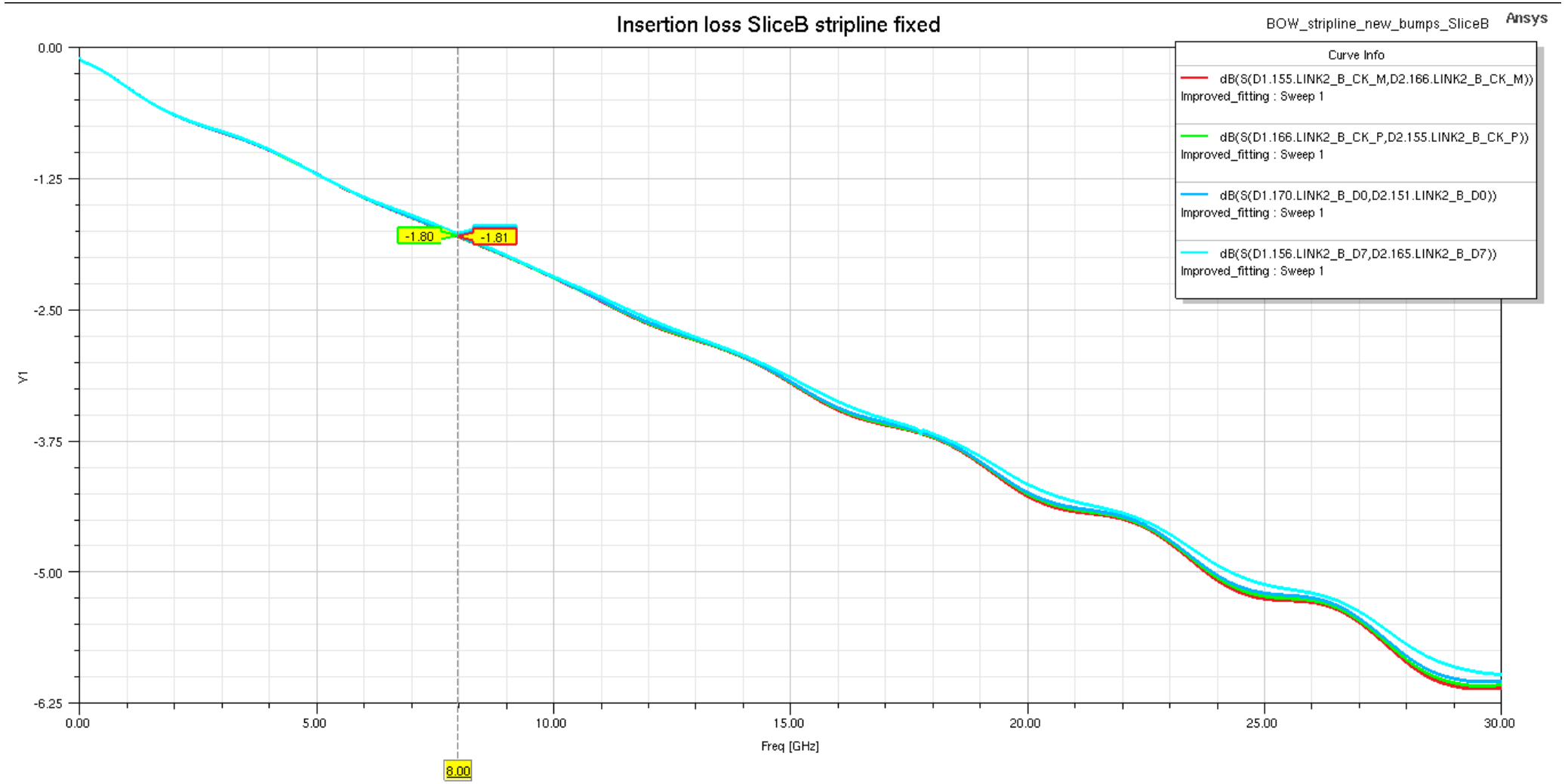
- 3 stacks layout.
- Models created for the middle stack (40 ports model)



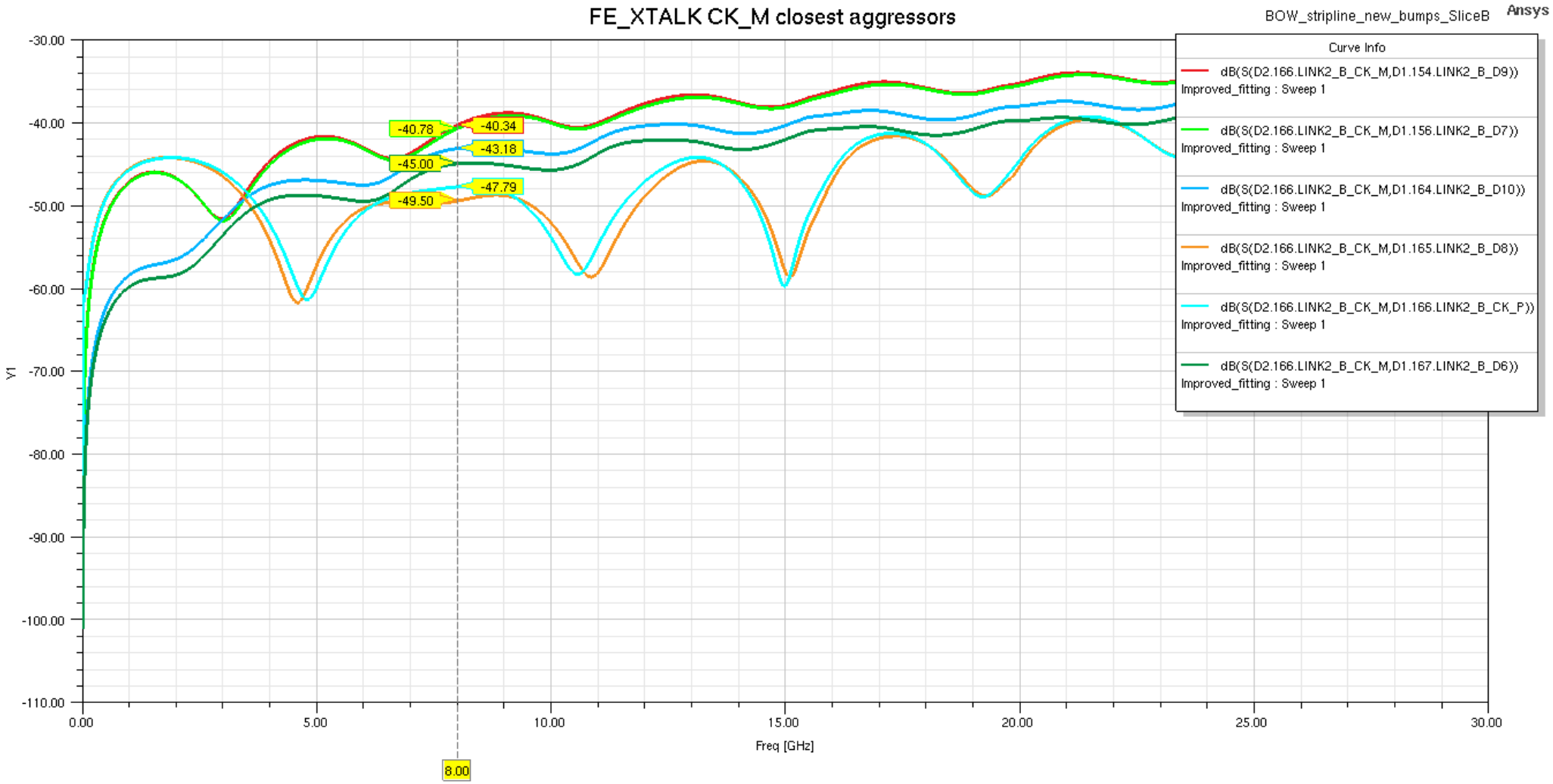
Return Loss Slice B stripline (layer4) -19/01 models



Insertion Loss Slice B stripline (layer4) -19/01 models

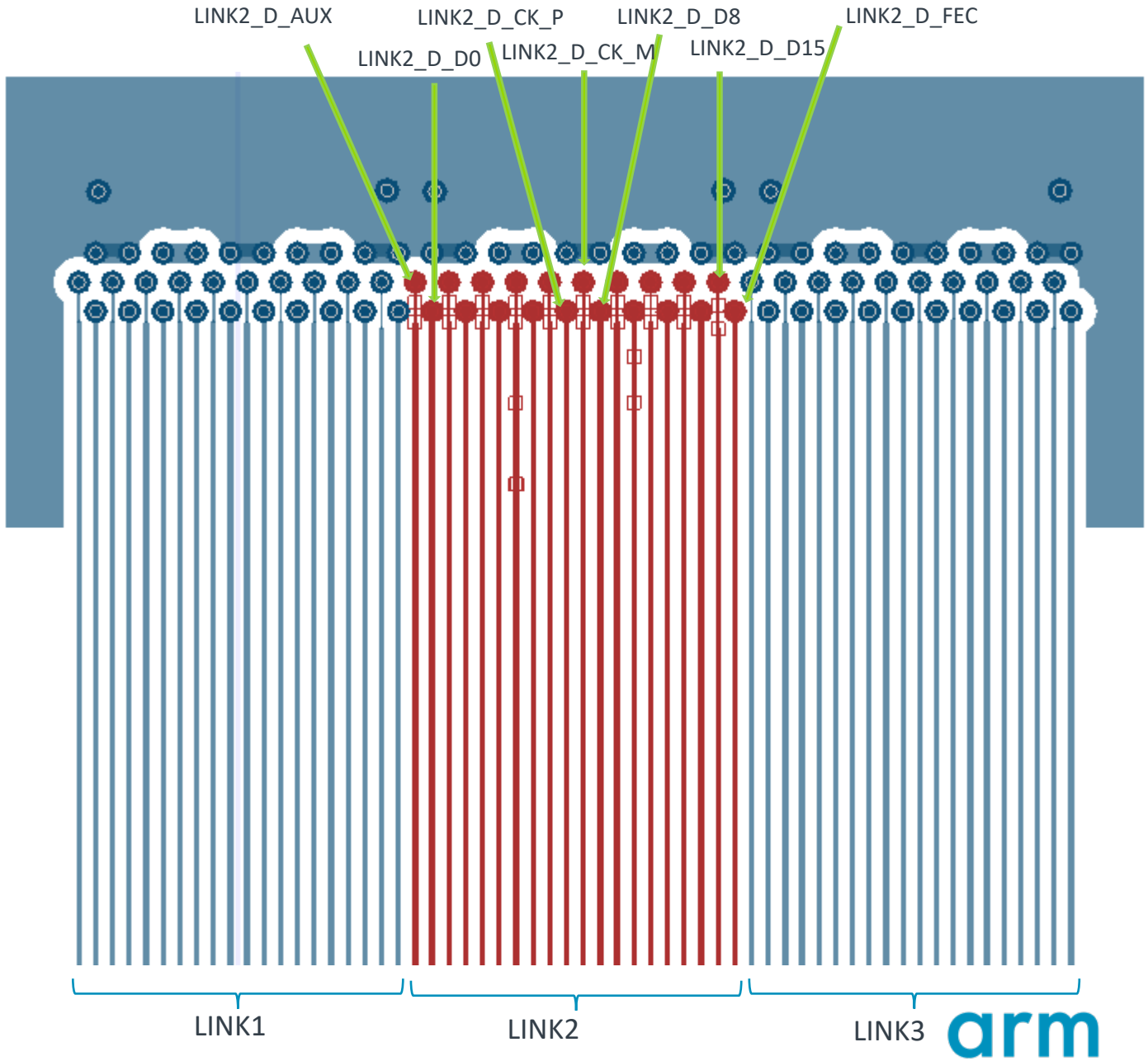


Far end Xtalk with B_CK_M victim (Stripline – layer4) – Only close aggressors -19/01 models

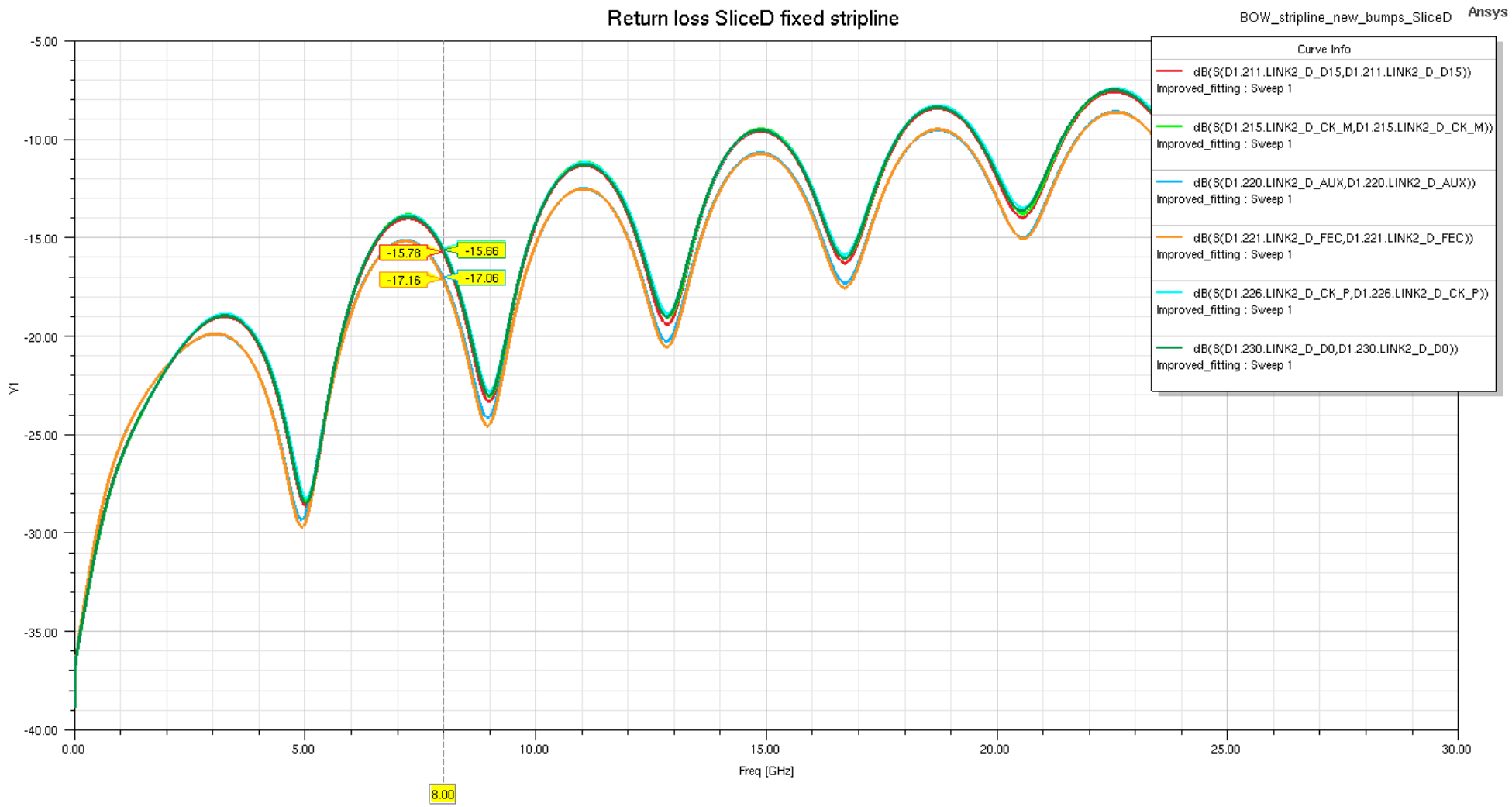


Slice D layout (layer 8)

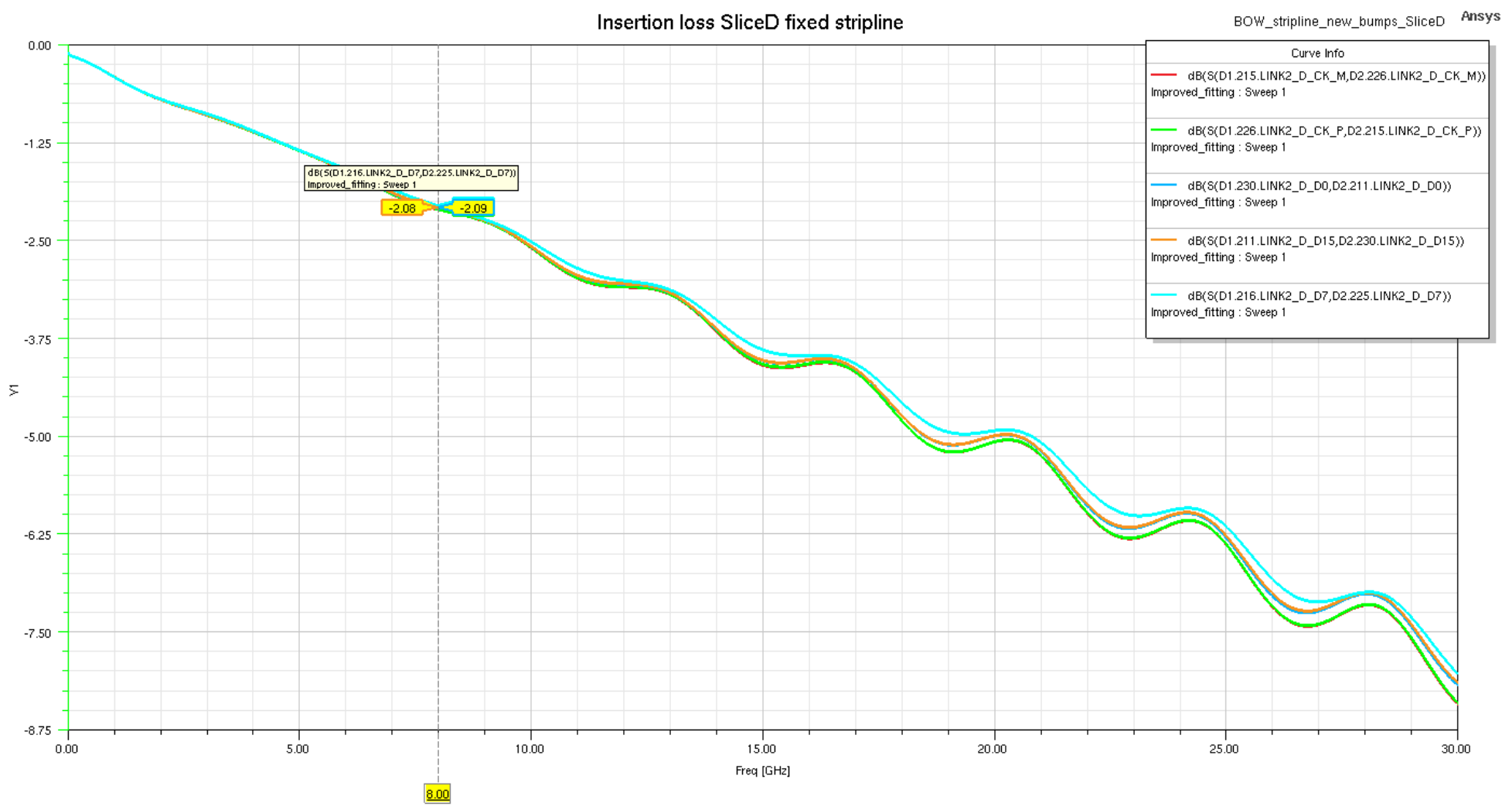
- 3 stacks layout.
- Models created for the middle stack (40 ports model)



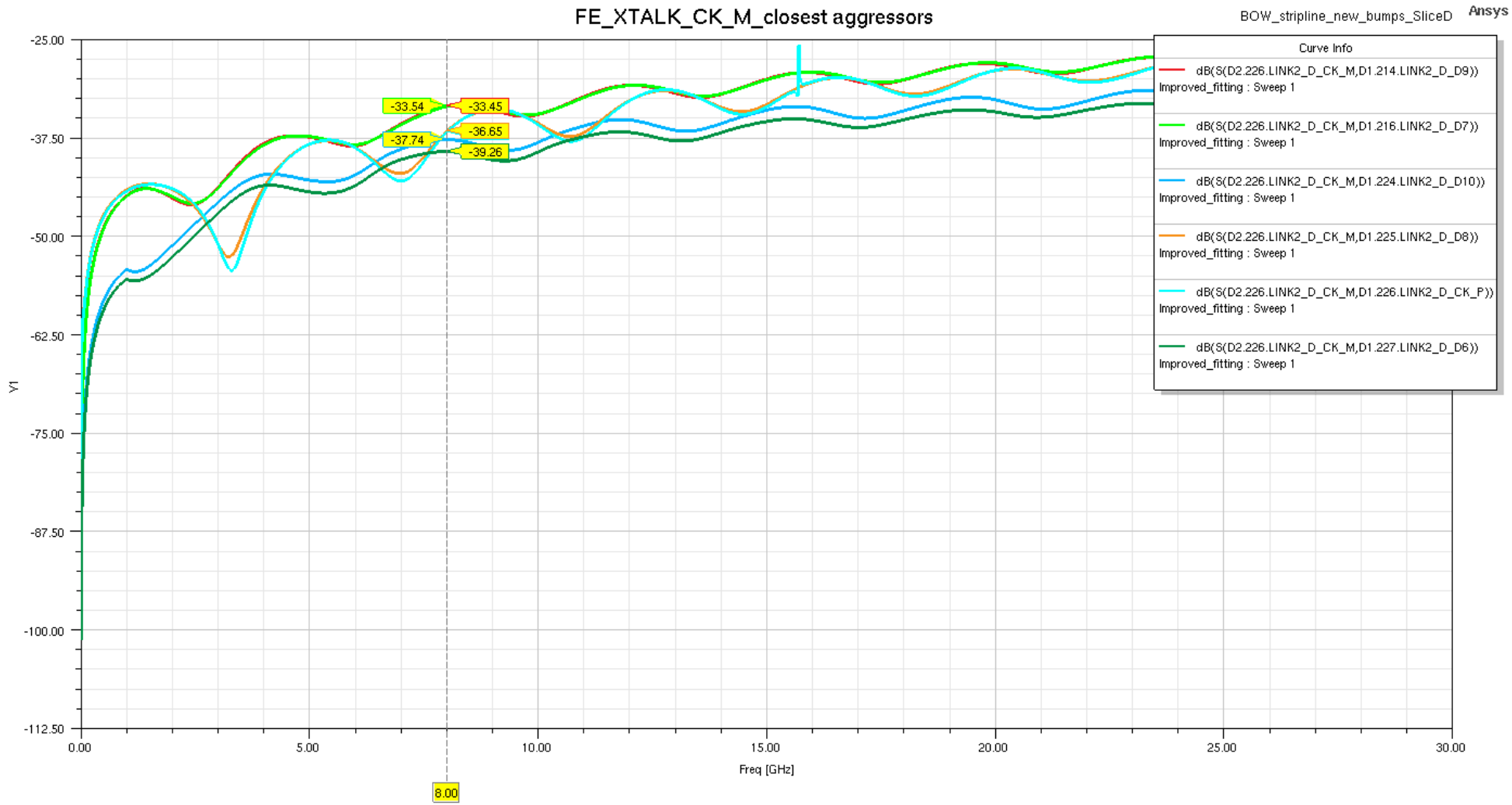
Return Loss Slice D stripline (layer8) -19/01 models



Insertion Loss Slice D stripline (layer8) -19/01 models



Far end Xtalk with D_CK_M victim (Stripline – layer8) – Only close aggressors -19/01 models



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Eye Diagram 20mm channel: Transient simulations

Simulation Setup

The number of aggressors can vary from 1 to 20

The worst case channel is monitored.

CK_P and CK_M (in the centre of the stack) are also considered as signal in this analysis.

The following conditions are applied (worst case from the BOW current spec):

- 16GBPs
- VDD= 0.75V
- 20% - 80% rise time: 0.32*UI
- 50 Ohms RX/Tx termination
- 300fF capacitance on TX/RX

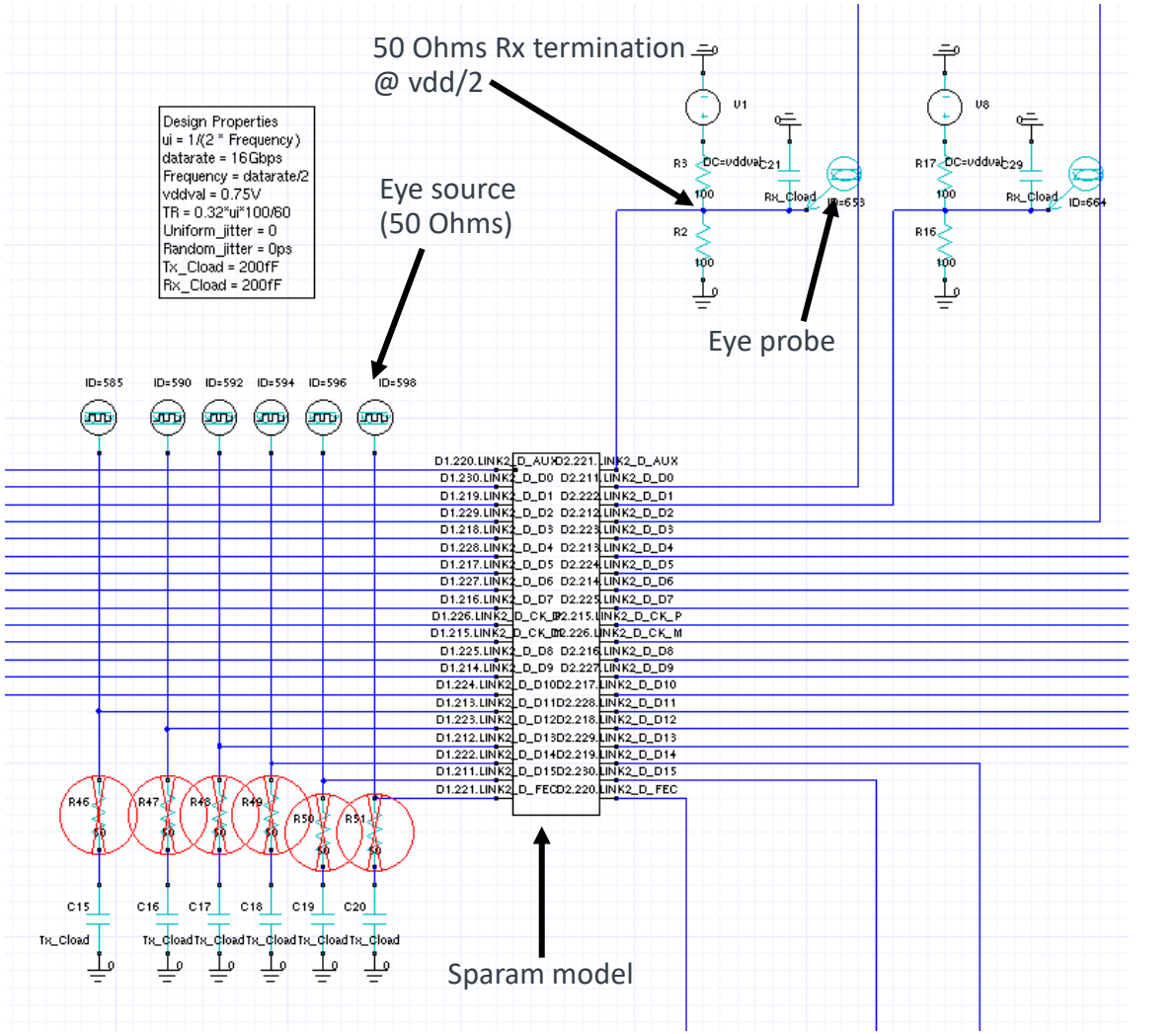
Additional simulation have been done with 200fF load cap

Target is to reach 68% eye opening:

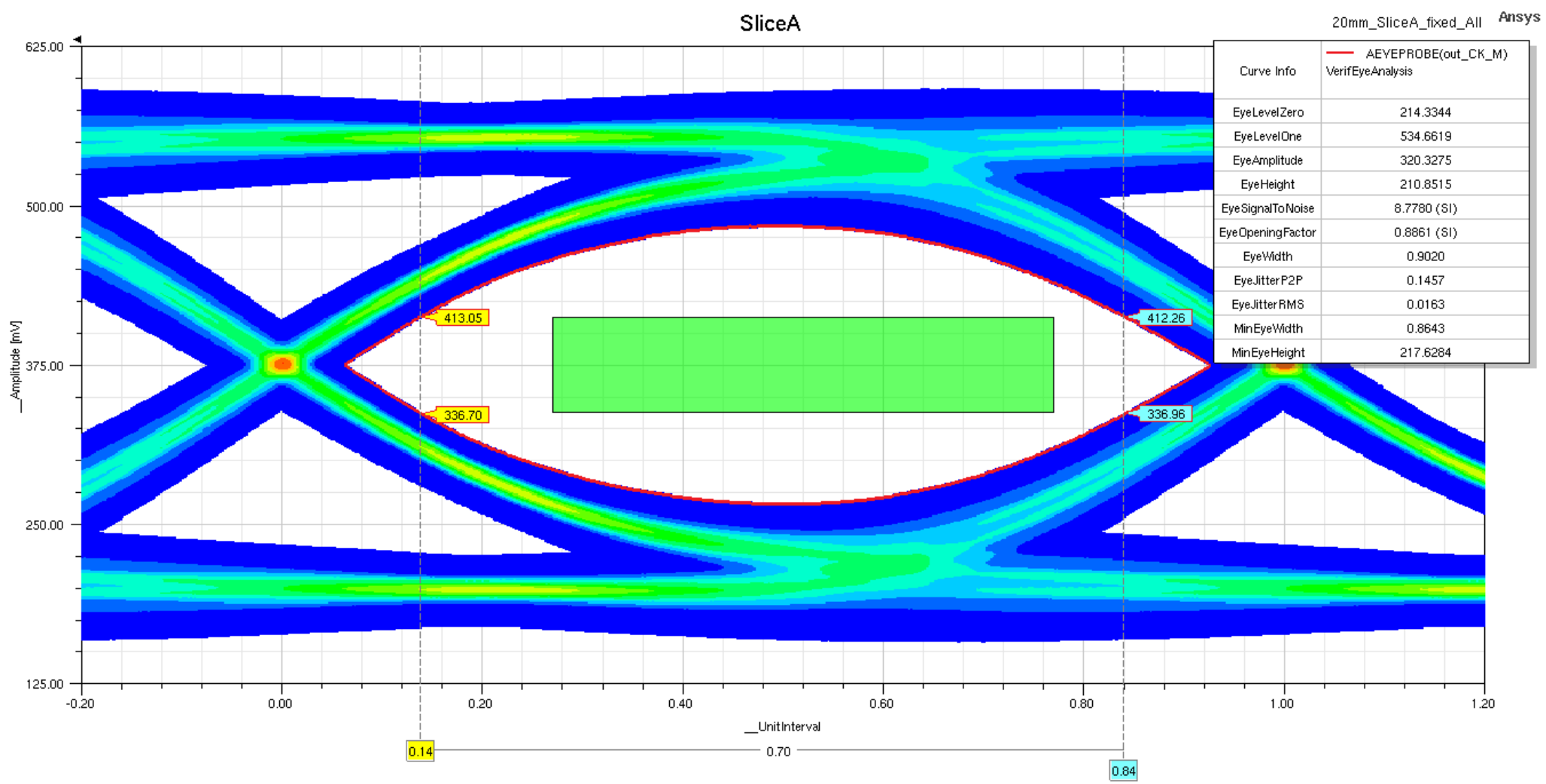
50% BOW spec +18% worst case jitter

The Picture below shows a portion of the schematic

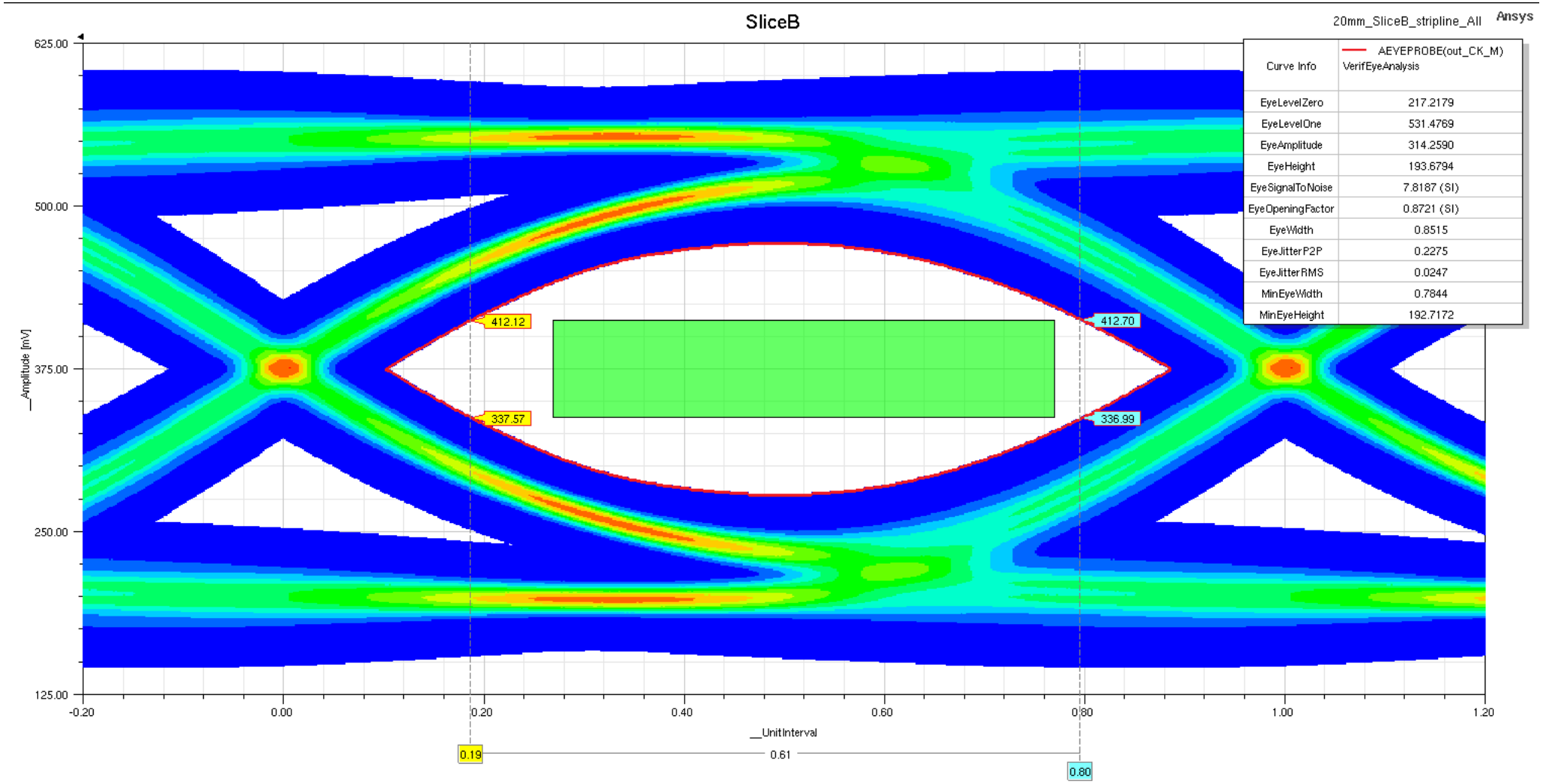
The BOW channel is simulated using a Statistical method (VerifEYE from ANSYS)



Slice A (L02) 300fF- 20 aggressors-Rise Time 0.32% UI (20/80%)
19/01 models

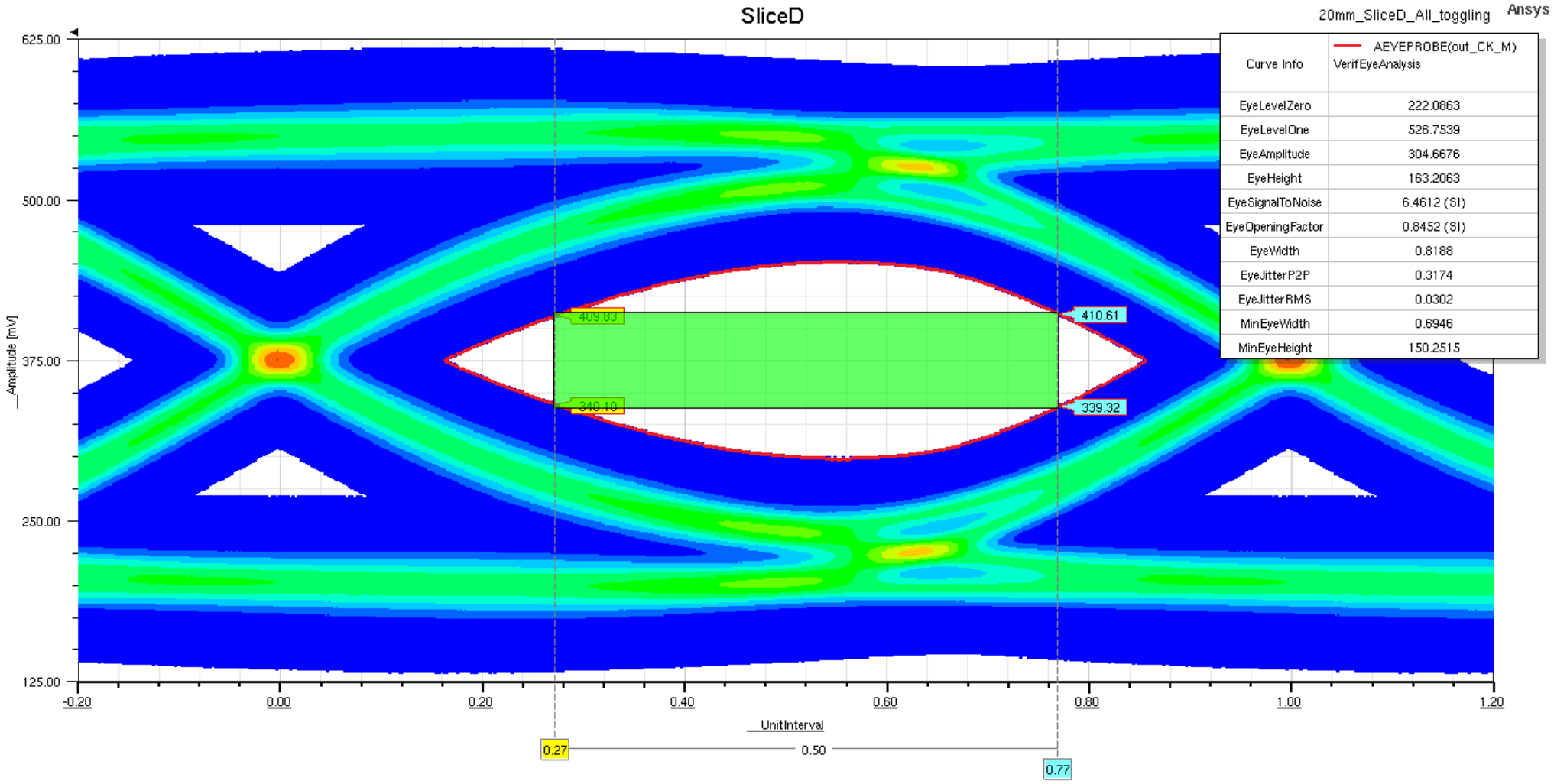


Slice B(L04) 300fF - 20 aggressors-Rise Time 0.32% UI (20/80%)
19/01 models

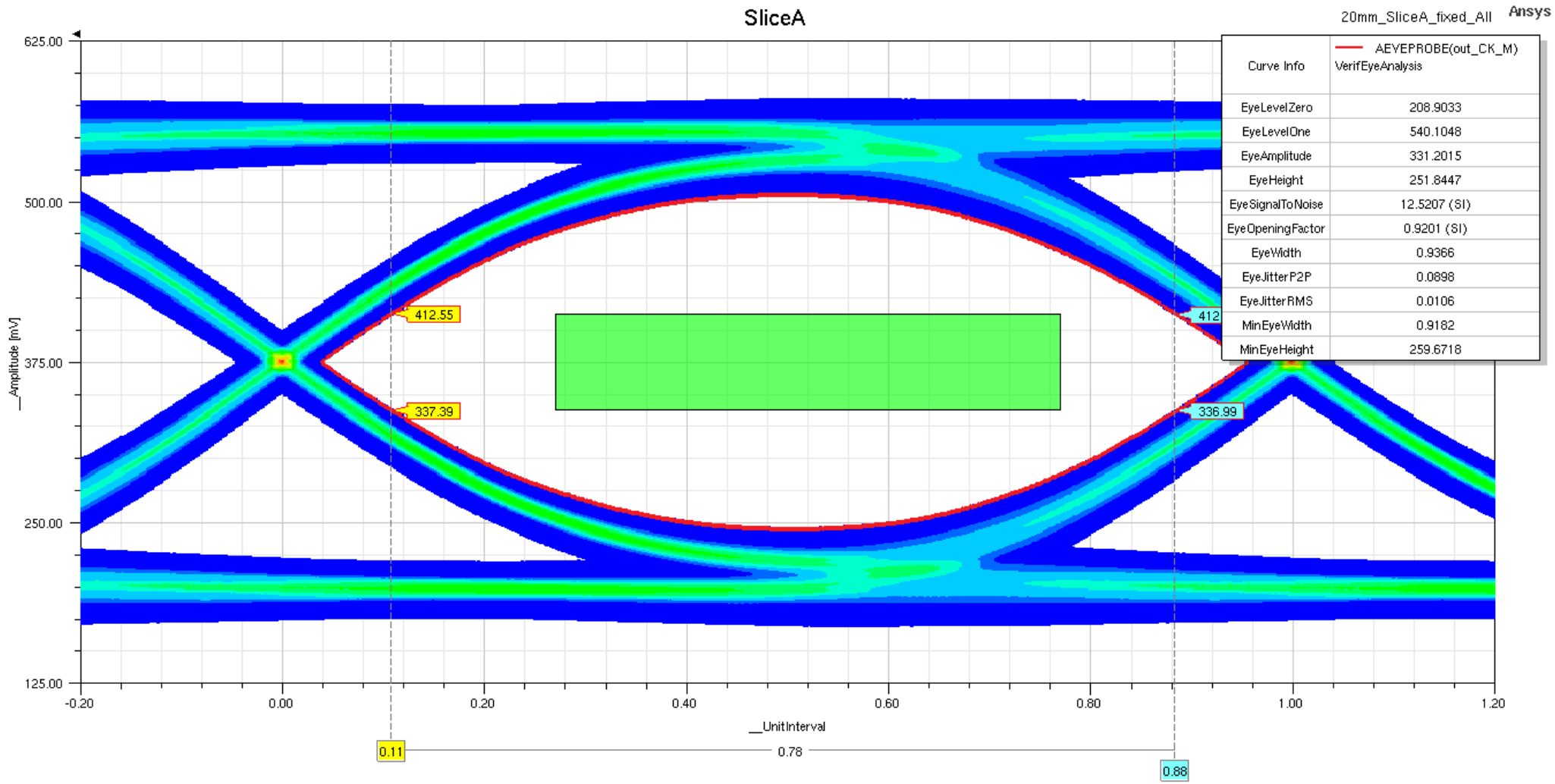


Slice D(L08) 300fF - 20 aggressors-Rise Time 0.32% UI (20/80%)

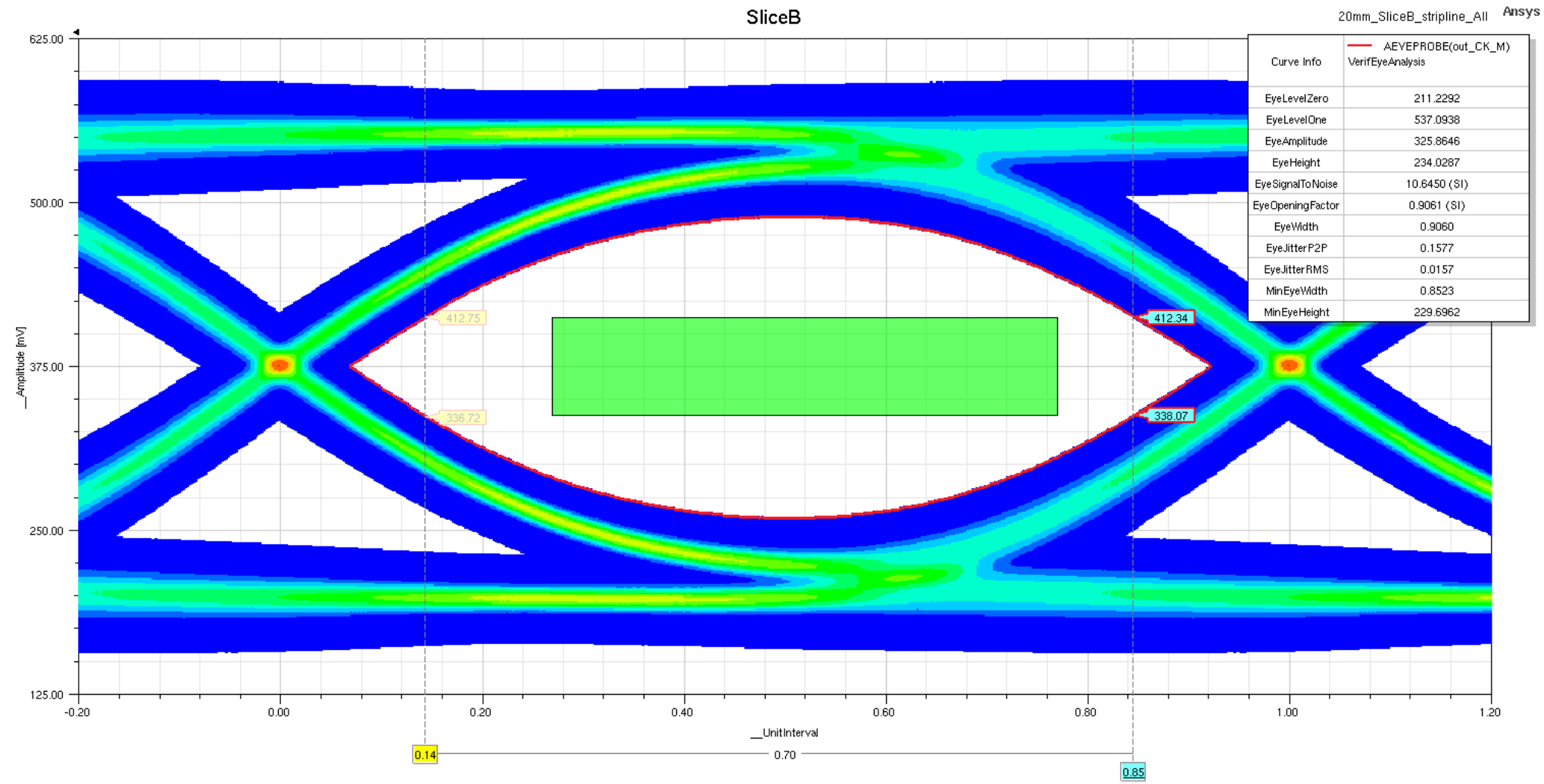
19/01 models



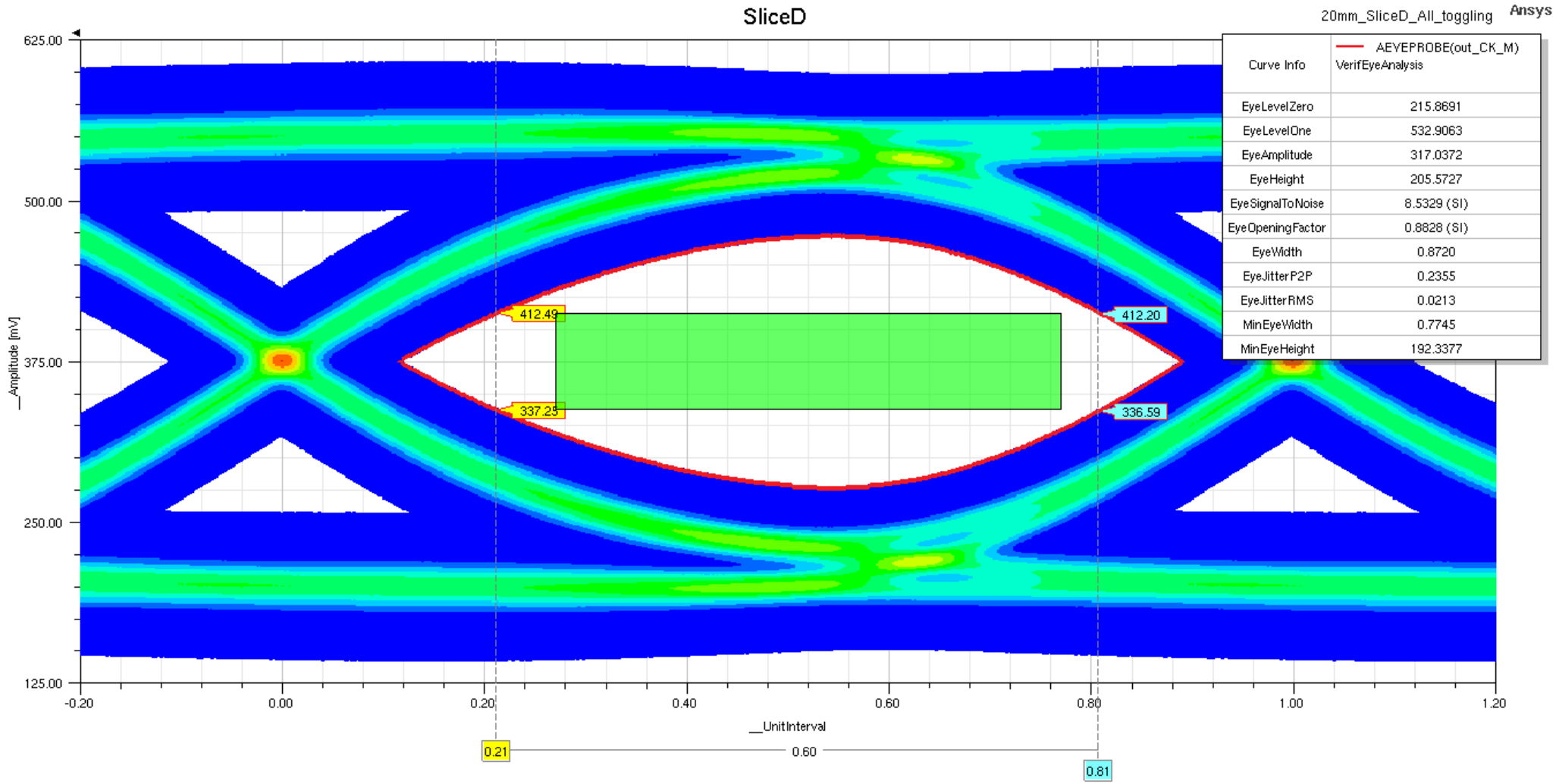
Slice A 200fF- 20mm – 20 aggressors -32%UI- 19/01 models



Slice B 200fF- 20mm – 20 aggressors -32%UI- 19/01 models



Slice D 200fF- 20mm – 20 aggressors -32%UI- 19/01 models



Eye diagram Summary table for the different slices- 01/02 models

Eye opening measurements done under the following conditions:

- CK_M/CK_P treated as signals
- Measurements done on the net in the centre of the channel (CK_M in this case)
- Clock Jitter not taken into account
- Rx sensitivity (Vrx_eye) =75mV (latest proposals on Tx/Rx Jitter not taken into account in this analysis)
- No Low-Pass_filter at Rx side

Fully Stripline (latest Design)	**Slice D**		**Slice C**		**Slice B**		**Slice A**	
C_{load} (Tx/Rx)	300fF *Tr=32% UI*	200fF *Tr=23% UI*	300fF *Tr=32% UI*	200fF *Tr=23% UI*	300fF *Tr=32% UI*	200fF *Tr=23% UI*	300fF *Tr=32% UI*	200fF *Tr=23% UI*
20 aggressors	53%	65%	57%	69%	63%	74%	71%	80%

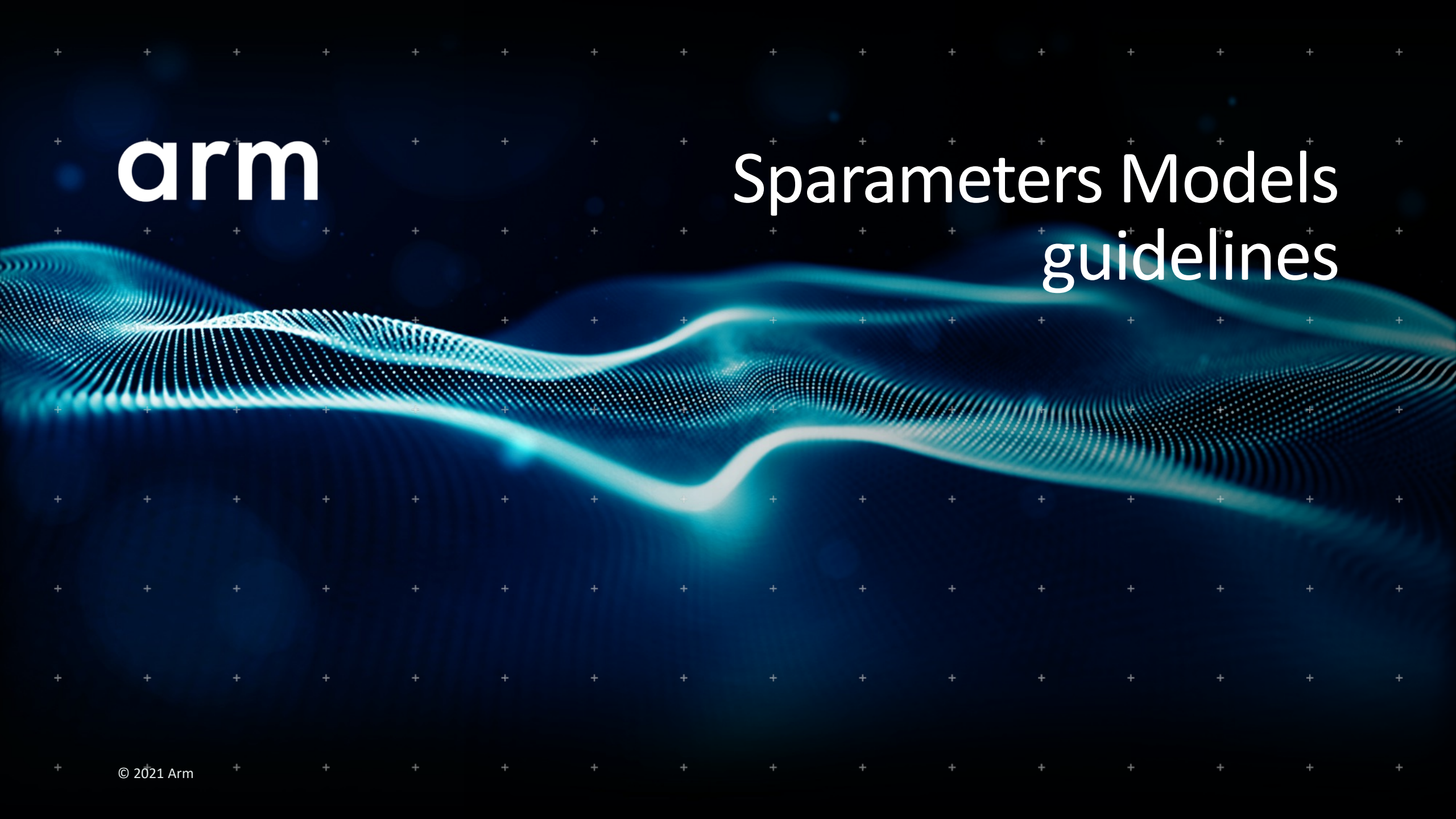
SliceC & SliceD: Main degradation is due to coupling in the vias

Further optimization is possible, but these numbers can only be improved by few %:

- Updating the material (gain <2%)
- Improving the GND connections around the signal vias (few %)

Conclusion

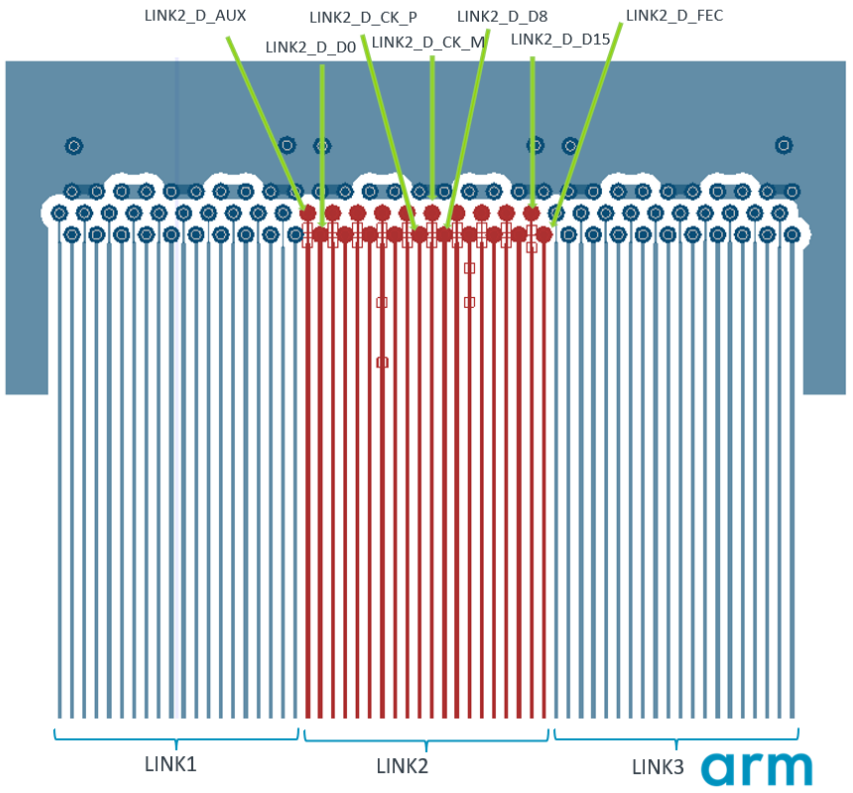
- These latest results seems fine for all Slices, considering the updated specifications from ODSA.



Sparameters Models guidelines

S parameters models guidelines

- *Current models are 40 ports models: 20 ports on each DIE (16 signals, 2 clocks, FEC and AUX optional signals).*
- *The naming convention is pretty simple, for example: D1.211.LINK2_D_D15 or D2.230.LINK2_D_D15*
  - *D1 is for die1 and D2 is for die 2.*
  - *D_D15 is for slice D signal D15.*
  - *I added a "LINK2" prefix because there are 3 stacks in the design, and I only extracted the "middle" stack (in RED in below picture)*



This Snapshot illustrates how to use the model for eye diagram simulations

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Thank You
Danke
Gracias
谢谢
ありがとう
Asante
Merci
감사합니다
धन्यवाद
Kiitos
شكرًا
ধন্যবাদ
תודה