Bunch of Wires PHY Specification

The Open Domain-Specific Architecture BoW Workstream

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Bunch of Wires PHY Specification

The Open Domain-Specific Architecture BoW Workstream

1. Introduction

The Bunch of Wires (BoW) is a simple, open and interoperable physical interface between two chiplets or chip-scale-packages (CSP) in a common package. This document specifies the BoW interface PHY layer.

1.1. Objectives

The BoW interface is a set of die-to-die parallel interfaces that provides the flexibility to trade off throughput/chipedge for design complexity, cost, and packaging technology.

The use of BoW is expected to be confined to connect die placed close to one another within the same package. In this environment, signal attenuation is small and the interface can be simple.

The definition of the BoW interface aims to meet the following design objectives:

- Inexpensive to implement
- Portable across IC process nodes ranging from 65 nm to 5 nm and beyond
- Flexible to support both laminate and advancing packaging technologies
- Portable across multiple bump pitches
- Unencumbered by technology license costs

- Very low power (< 1 pJ/bit) as defined by TX IO Pad, wire and RX IO Pad.
- Very low latency (<5 ns without FEC, <15 ns with FEC from logic interface to logic interface)
- High throughput density (100-1000+ Gbps/mm-chip-edge)
- Backwards compatible (across at least two major specification versions)

1.2. Advantages

The Bunch of Wires interface provides several key advantages for chiplet-based systems:

- Can operate at higher data rates per pin than existing parallel standards
  - or at lower data rates for compatibility with existing parallel standards
- Can be implemented in legacy technologies (process nodes) with generally available IP
- Can be implemented in low-cost laminates or higher-density silicon-based interconnect
- Can be implemented with much less design effort than a traditional SerDes
- Is not constrained to a specific bump pitch
  - interfaces with somewhat different bump pitches can be connected

Compared to SerDes, BoW uses a lower data rate/wire so it requires more wires. However the lower data rates allow use of single-ended signaling and denser wire packing. In addition, in laminates, BoW can take advantage of multiple wiring layers and in advanced packaging it can take advantage of the much-increased wire density.

1.3. Scope

The scope of this document has several levels.

1. The specification of the BoW interface includes these requirements:
   a. Operating modes
   b. Chip-to-chip wire signals
   c. Wire ordering
   d. Timing and electrical specifications on the chip-to-chip interface
   e. Signals at the logic (Link Layer) interface
   f. Configuration, initialization, calibration
   g. Functions that must be supported at the Link Layer or above
2. The specification includes recommendations for these elements:
   a. Bump patterns
   b. Arrangement of multiple slices in a link
   c. Arrangement of wires in laminate and advanced packaging
   d. signal integrity of the wire channel
   e. Configuration and management programming
   f. Design for test and test methods
   g. Performance estimates
   h. Compliance verification

3. The following activities are outside the scope of this document:

    a. Specific implementations of the interface
    b. Integration of the interface with system-level data flow e.g. interface to a PHY-layer abstraction such as PIPE/PCIe interface to the BoW
    c. The use of this interface outside of a package or entirely inside a chip
    d. Definition of protocols for logical data transfer

4. The following aspects may be addressed in subsequent versions of this specification:

    a. Simultaneous bidirectional data (full duplex on each wire)
    b. Security

1.4. Language

- "Shall" or "must" indicates a requirement. Failure to meet the requirement results in non-compliance
- "Should" indicates a recommendation, but not a requirement. Failure to implement the recommendation does not result in non-compliance.
- "May" indicates an implementation option.
- The lack of one of the above verbs indicates the material is informative.
- "Reference" indicates a reference design that is provided as example for explanation, but is not a requirement.

1.5. Compliance Summary

The specifications must be met over process variation, supply voltage range and temperature range (PVT). Each implementation must document its supported I/O voltage range, supply voltage range and temperature range.

Table 1 summarize the compliance points that shall be met in order to comply with the BoW specification. Each of the compliance points is discussed in the specification.

2. BoW Overview

This section provides an overview of the BoW physical interface (PHY) and its use in a multi-chiplet design.

2.1. BoW Slice

BoW is an energy-efficient, easy-to-use PHY interface between a pair of die inside a single package as shown in Figure 1. The BoW PHY is defined as a single unidirectional slice. Multiple slices are combined to create links of the desired throughput. A link may be symmetric, asymmetric or unidirectional. The BoW PHYs between two die are physically connected through wires on a substrate or interposer. A BoW PHY does not have enough drive strength for off-package interfaces, nor is it designed for buses that are entirely on die.

This document specifies the protocol for a BoW PHY slice. The aggregation of multiple PHYs into a link is beyond the scope of this document.

Description	Section	Detail
BoW Modes	2.3	
Die-to-die Signals (Wires)	3.1	
Slice Logic Interface	3.2	
BoW Modes and Reach	4	Table 6
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Channel Skew	8.1	
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Table 1. BoW Compliance Summary

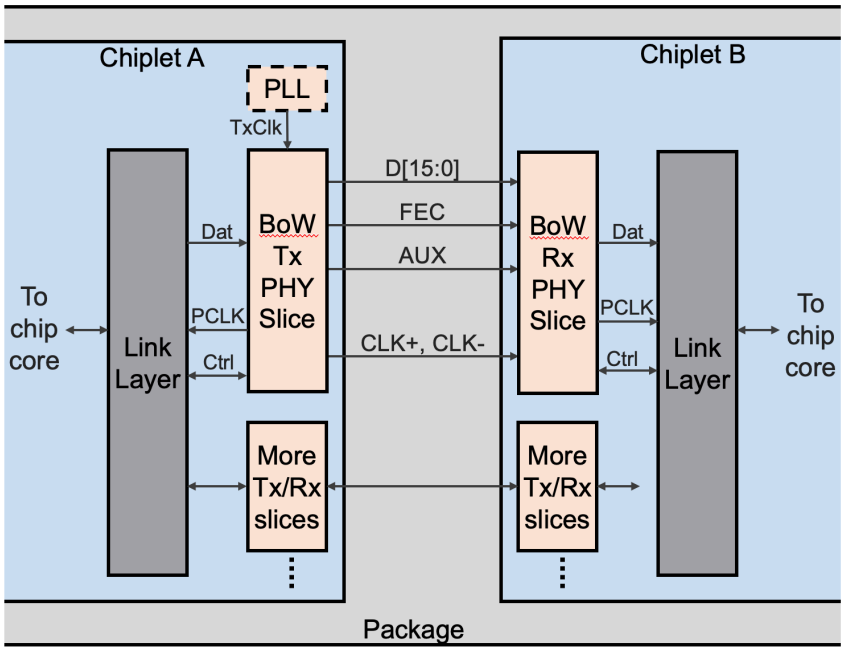

Figure 1. BoW Overview

BoW Mode	Slice Data Rate Gbps	Wire Bit Rate Gbps/wire	TxClk GHz
BoW-32	32	2	1
BoW-64	64	4	2
BoW-128	128	8	4
BoW-256	256	16	8

Table 2. BoW Modes

A BoW PHY slice either transmits or receives 16 bits of data between die. The BoW is a source-synchronous PHY and each transmitting PHY slice transmits a complementary clock signal CLK+ and CLK- with the data. A BoW PHY optionally has two additional wires designated FEC (for Forward Error Correction) and AUX, for other optional functions such as Data Bus Inversion (DBI).

2.2. BoW Wires

Within the package, the BoW datapath is transported on physical passive wires between the pair of connected die. The specifics of the wires, such as their density, maximum length, impedence characteristics and how they are realized vary with the packaging technology. In order to minimize power, unterminated and source-terminated links will have short reaches requiring chips to be adjacent.

2.3. BoW Modes

A BoW PHY must be operable in one of the BoW Modes listed in ascending order in Table 2. A BoW Mode defines the speed of clock and data of the PHY on the die-to-die wires. In all modes, the data must be clocked DDR: the chip-to-chip data wire bit rate is double the clock wire frequency. All BoW interfaces faster than BoW-64 should also be able to support BoW-64. Supporting rates other than the defined four modes is an implementation choice. There is more detail on BoW Modes in section 4.

Figure 2 shows the tradeoff between package, data rate, termination, and reach. Source-terminated BoW on laminate allows a longer reach than advanced packaging, but the wider design rules in laminate means that both of these cases are barely able to reach 8 Gbps/wire. A doubly-terminated link offers longer distances and higher rates, but requires a more complicated receiver design.

2.4. Logic Interface

Figure 3 shows the logic interface between a BoW slice and the digital Link Layer logic in a chip. The speed at the logic interface (Figure 1) is implementation-dependent. Typically, PCLK will be the TxClk frequency divided by a power of 2, so 250, 500 and 1000 MHz are common rates. The data at the logic interface is SDR (bit rate equal to PCLK frequency).

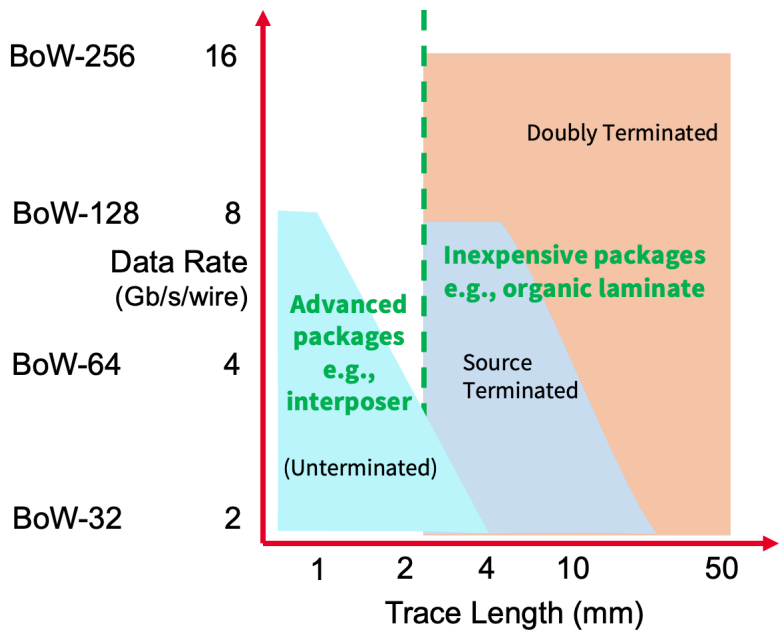

Figure 2. BoW Data Rate vs. Reach tradeoff

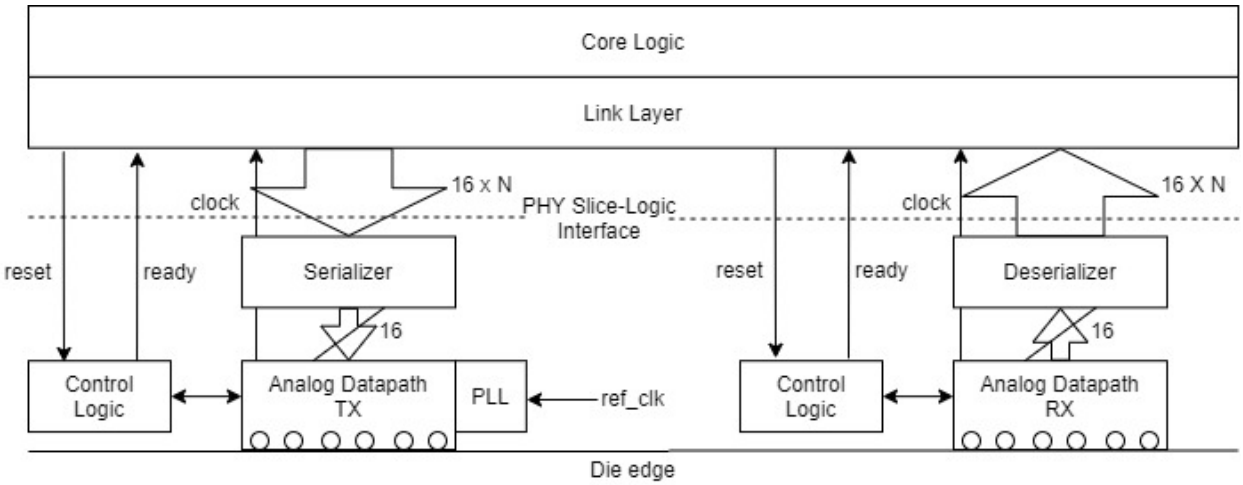

Figure 3. BoW slice logic interface

Function	# Wires	Signal Name	Notes
Clock	2	CLK+, CLK-	Differential
Data	16	D0-15	
Forward Error Correction	0/1	FEC	Optional
Auxiliary	0/1	AUX	Optional

Table 3. BoW Signals at the Die To Die Interface

3. Signal Definitions

This section specifies the control data signals into and out of device logic and package for BoW RX and TX slices.

3.1. Die-to-die Signals (Wires)

As shown in Figure 1, each BoW slice consists of a differential clock pair, 16 single-ended data wires, and an optional pair of wires FEC and AUX.

Each BoW slice is unidirectional when in operation. A chiplet may be designed with RX-only and TX-only slices, or each slice may have both TX and RX capability which is configured at runtime. A bidirectional link is composed of some number of slices configured for RX and some for TX.

FEC (Forward Error Correction) is an optional signal that allows using FEC to improve the bit error rate (BER). By using an additional wire when FEC is enabled, the payload data rate is not affected and the wire data rate is unaffected. This allows F(PCLK) = F(TxClk) / 2^n with FEC off or on, which simplifies the clock generation and serialization functions. If used, FEC is implemented in the Link Layer, and the PHY treats the FEC bit the same as the other data bits.

AUX is an optional signal that can be used for purposes such as Data Bus Inversion (DBI), flow control, redundancy for defect repair, etc.

The Link Layers of Chiplets A and B will need to agree on the details on FEC and AUX usage. An implementation may choose to support the FEC and AUX wires, or to omit both of them. If FEC and AUX are included in a PHY implementation, the PHY carries them in the same way as the data bits without acting on the content.

Table 3 summarizes these signals.

3.1.1. DBI on the AUX wire

Data Bus Inversion (DBI) can be used to mitigate simultaneous switching output (SSO) noise or to optimize energy of a BoW PHY by reducing the number of BoW data wires that switch between adjacent data transfer cycles. DBI functionality is optional; it one of several possible uses of the AUX wire. If implemented, DBI is in the Link Layer and must be implemented on both RX and TX.

3.2. Slice Logic Interface

Figure 3 shows the data and control signals in the interfaces to the logic in the die in each BoW transmit and receive slice. The data at the slice logic interface must be SDR (Single Data Rate -

Signal	# Bits	TX Slice	RX Slice	Description
Data	16*N	In	Out	Data
FEC	N or 0	In	Out	Forward Error Correction (optional)
AUX	N or 0	In	Out	Auxiliary uses (optional)
PCLK	1	Out	Out	
TxClk	1	In	NA	Comes from a PLL or other clock source, not the Link Layer. The TxClk source is usually shared among many TX slices. May be differential
RxClk	1 or 0	NA	Out	May be differential

Table 4. Logic Interface Signals

Signal	# Bits	TX Slice	RX Slice	Description
PHYResetB	1	In	In	Resets the BoW slice. 0 causes a reset
PHYReady	1	Out	Out	Indicates that the PHY is ready to transmit/receive mission mode data. 1 indicates ready

Table 5. Logic Interface Control Signals

bit rate equal to the PCLK frequency).

3.2.1. Slice Logic Interface: Data Signals

The signals in Table 4 shall constitute the data and clocks in the logic interface of the PHY. N is the ratio of the chip-to-chip per-wire data rate to the logic interface per-wire data rate.

3.2.2. Slice Logic Interface: Control Signals

A BoW interface must provide the following control and status signals:

- PHY Ready
- PHY Reset

The signals in Table 5 shall constitute the control portion of the logic interface of the PHY.

3.2.2.1. PHYResetB TX and RX The PHYResetB pin shall be asserted by the link controller to initialize the PHY. While the PHYResetB signal is asserted, the PHY shall stay in its reset state. When the PHYResetB signal is de-asserted, the PHY shall perform any necessary self-alignment. The reset states are otherwise implementation-dependent and shall be documented in the datasheet of a particular implementation.

3.2.2.2. PHYReady TX On a TX slice, the PHY shall assert PHYReady to indicate it is transmitting appropriate CLK and PCLK signals, and that it is ready to transmit data.

3.2.2.3. PHYReady RX On an RX slice, when PHYResetB is deasserted, the PHY assumes that the corresponding TX slice is sending CLK and that the TX Link Layer is sending training data on the data wires.

After the RX slice clock self-alignments are complete, each RX PHY slice shall assert its PHYReady pin. How an RX PHY slice determines completion of the self-alignment is implementation-dependent. For instance, it can be determined by observing the settling of the DLL or by a simple timer. PHYReady asserted indicates that any data received will be captured correctly.

3.2.3. Programming

There shall be an AMBA APB programming interface to control internal registers for control and status readout of the PHY.

The internal registers are implementation-dependent. The internal registers shall be fully documented in the PHY datasheet.

3.2.4. Link Controller

There shall be a Link Controller (LC) outside the PHY. This will manage initialization of the Link. It may reside on one of the chiplets of the link, in a third chiplet in the package or outside the package.

Communication from the Link Controller across chiplets shall be by a transport mechanism outside the BoW link. This could be a serial link like SPI or I2C, but this is not specified at this time.

Link initialization is described in Section 9. Clocks are described in 7.2.

4. BoW Modes and Reach

A BoW PHY slice must conform to at least one of the BoW Modes seen in Table 2. The recommended maximum wire reach for different packaging types and terminations is seen in Table 6. Exceeding these reach values may degrade the voltage margins at the receiver. See section 8 for how TX, RX and channels are qualified.

"Laminate" is intended to include organic laminate packages (a.k.a. "buildup"") and similar technologies with approximately 25 μm line and space rules. The minimum wire length for closely spaced chips in these technologies is around 3 mm for the slice closest to the chip edge.

"Advanced" is intended to include silicon interposer and similar technologies. These have much finer line and space dimensions, but traces are usually much more resistive than in organic laminate packages and will be limited to much shorter trace lengths. Due to these short traces, termination is not expected to be useful for implementations targeting Advanced packaging. The minimum wire length in these technologies may be less than 1 mm.

Adding termination increases the speed and/or reach, at the expense of greater design complexity and power.

Package			**Laminate**	**Laminate**	**Laminate**	**Advanced**
Termination			None	Source	Double	None
BoW Mode	**Wire Bit Rate**	**TxClk**	**Reach**	**Reach**	**Reach**	**Reach**
	(Gbps/wire)	(GHz)	(mm)	(mm)	(mm)	(mm)
BoW-32	2	1	10	20	25+	4
BoW-64	4	2	NA	10	25+	2
BoW-128	8	4	NA	5	25+	1
BoW-256	16	8	NA	NA	25+	NA

Table 6. Recommended BoW Wire Reaches

5. BoW Physical Configuration

5.1. Dead-Bug Views

The physical diagrams and descriptions in this document must be interpreted as looking down at the top layer of the unpackaged chiplets. Since these are flip-chip packages, these views are equivalent to looking through the bottom of the package with the balls up (dead bug view). For the view as seen looking down on a package as mounted on a PCB (live bug view), these views must be mirrored.

5.2. BoW Components

A BoW link between two chiplets is made up of wires, slices, and stacks as seen in Figure 4.

- The signal traces in the package between chiplets are called **wires**.
- A **slice** is the the basic unit of a BoW PHY. It must have 18 or 20 signal bumps. It must have 2 bumps for the differential clock and 16 single-ended data bumps. It may also have the optional single-ended signals AUX and FEC. The long edge of a slice must be parallel to the chip edge.
- A **stack** is composed of one or more slices stacked from the chip edge towards the center. The slice positions are designated A, B, C, etc, starting with the slice closest to the edge of the chip.
- A **link** from one chiplet to another is composed of one or more stacks placed along the chip edge. A link may be configured with equal numbers of RX and TX slices, or it may be asymmetric or one-way.

5.3. Example Link

The minimal bidirectional reference link is shown in Figure 5.
In this example, each chiplet has one TX slice and one RX slice, arranged in two one-slice stacks on each chiplet. This is a dead-bug view.

5.4. Die-to-Die Signals

Each BoW slice consists of a differential clock pair, 16 single-ended data wires, and optional wires FEC and AUX. Each BoW slice is unidirectional when in operation. A PHY may be designed as

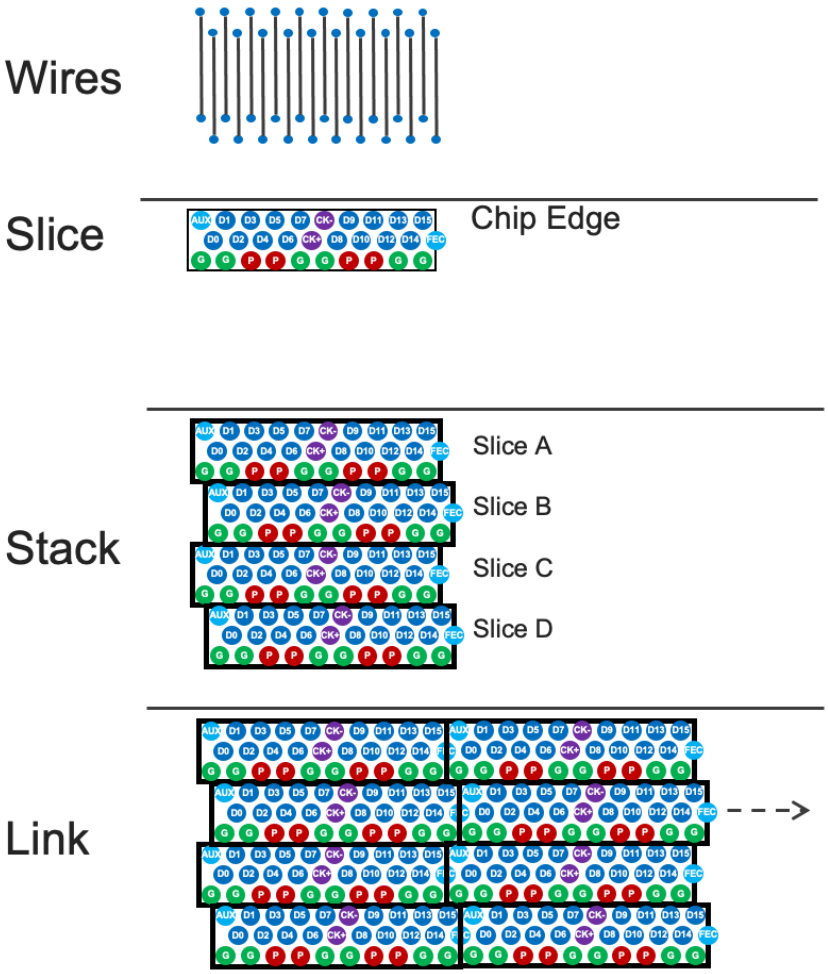

Figure 4. BoW Link Components

Function	# Signals	Signal Name	Notes
Clock	2	CLK+, CLK-	Differential
Data	16	D[15:0]	
Forward Error Correction	0/1	FEC	Optional
Auxiliary	0/1	AUX	Optional

Table 7. BoW Die-to-Die Signals

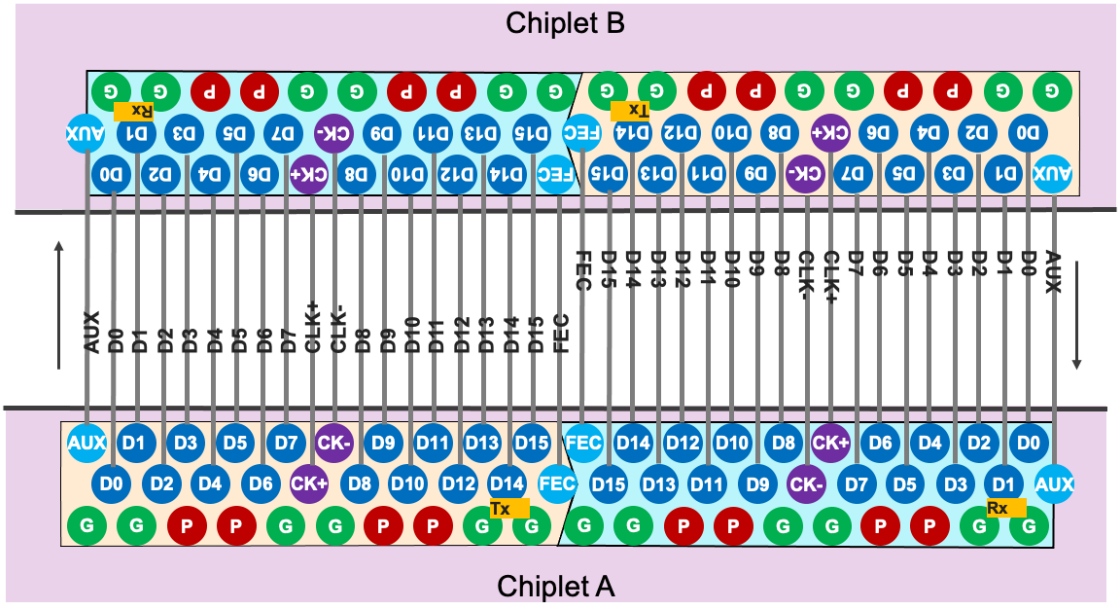

Figure 5. BoW Minimal Bidirectional Reference Link

RX-only and TX-only slices, or each slice may have both TX and RX capability, one of which is selected at configuration time. A bidirectional link is composed of some whole number of slices configured for RX and some whole number of slices for TX.

FEC (Forward Error Correction) is an optional signal that allows using error correction to improve the bit error rate (BER). AUX is an optional signal that can be used for purposes such as DBI, flow control, redundancy, etc. Chiplets A and B will need to agree on the details on FEC and AUX usage, which is defined in the Link Layer.

5.5. Signal Ordering

A BoW interface must conform to these wire order rules at the edge of the chip:

- The signals for a TX slice are in the following order at the chip edge, going clockwise around the chiplet in a dead-bug view: AUX, D0, D1, D2, D3, D4, D5, D6, D7, CLK+, CLK-, D8, D9, D10, D11, D12, D13, D14, D15, FEC
- The signals for an RX slice are in the reversed order (ascending goes counter-clockwise)
- The same clockwise/counter-clockwise ordering is used on all four sides of a chiplet
- The AUX and FEC signals may be omitted

5.6. Bump Arrangements

Note that bump patterns are not specified by BoW; only the signal *ordering* at the chip edge is specified for interoperability.

The reference example in Figure 5 uses hexagonal closest packing for the bumps: two rows for signal bumps and one row for power and ground bumps. In this pattern, the wire pitch is half the bump pitch.

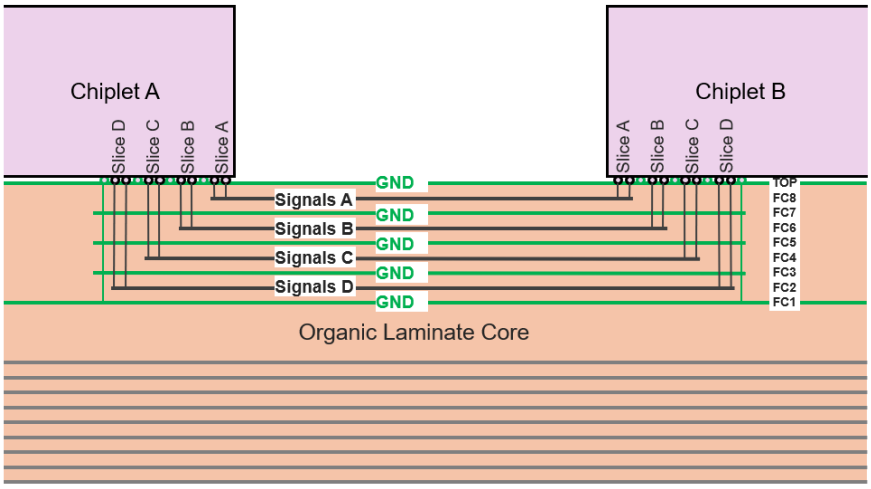

Figure 6. Cross section of a BoW Link in an Organic Laminate Package

5.6.1. Alternate Bump Arrangements

Alternate bump arrangements may include:

- 90-degree rotation of the hexagonal packing direction (to decrease the wire pitch 14%)
- square bump arrays instead of hexagonal (for regularity of layout)
- more than two rows of signal bumps (to decrease the wire pitch without changing the bump pitch)
- different ordering of power and ground bumps
- multiple power and ground rows

Somewhat different wire pitches between two chiplets can be accommodated with fan-out in the chip-to-chip wires. This is limited by the maximum skew due to different wire lengths - see section 8.1.

5.7. Cross Section

An example cross section for an organic laminate (a.k.a. "buildup") package is shown in Figure 6.

In an organic laminate package, signal layers should be alternated with ground layers in order to maintain a controlled impedance of 50 Ω. Each slice position (A, B, C, D) should be associated with one signal layer and there should be no mixing of signals from multiple slices.

In any technology, the position-A slice on chiplet A must be connected to the position-A slice on chiplet B (one must be configured for TX and one for RX). The position-B slices are connected together, and so on.

There is no specified limit to the number of slices in a stack. In organic laminate, the practical limit in 2020 is an 8-2-8 laminate which supports 4 slices as shown in Figure 6. A 7-2-7 laminate can support 4 slices by omitting the top GND layer, but with reduced signal integrity. Layers on the bottom side of the package typically cannot be used for BoW signals due to low via density passing through the thick central core layer.

In advanced packaging technologies, the shorter wire lengths and higher wire resistance suggests the use of non-controlled-impedance wires and unterminated transmitters and receivers. The smaller wire and space dimensions may allow the wires for multiple slices to be interleaved on a single wiring layer. The wire order within each slice must be maintained, even if interleaving with other slices is used.

5.8. Staggered Slices

To optimize the density of hexagonal bump arrays, slices in positions B and D may be offset horizontally by one half the bump pitch as seen in Figure 7. This necessitates a one-bump-pitch horizontal jog in the wires for slices B and D. The practical effect of this 130-um jog across a 2.5+ mm wire between chiplets is very small.

An alternative arrangement is to keep the slices aligned vertically. This requires adding a small extra vertical space between the slices, for an overall increase of 4% of the slice area.

5.9. Slice Numbering

A BoW interface must conform to these slice numbering rules:

- The TX slices in a link are numbered from 0 at the upper left edge of the link (facing from the chip center to the edge in a dead-bug view) and ascending through the TX slices in a stack, then from stack to stack clockwise.
- The RX slices in a link are numbered from 0 at the upper right, through the RX slices in a stack, then stack to stack counterclockwise.

An example of this numbering is shown in Figure 8.

The signal ordering and slice numbering rules allow BoW chiplets to be connected without signal reordering regardless of chiplet rotations.

5.10. Slice Stacking Pattern for Symmetric Links

For bidirectional links, a pattern of alternating TX and RX stacks should be used. Figure 8 shows an example bidirectional link with 4 stacks of 4 slices each, for 8 TX and 8 RX slices on each chiplet. The first TX stack should be at the left edge of the link.

Asymmetric and unidirectional links may use any slice pattern, but the slice numbering rules must be observed.

An alternate approach with more flexibility is to design every slice to operate as either RX or TX, to be configured after assembly or upon powerup. This allows complete flexibility in link configuration and interoperability and also provides an opportunity for wafer-level loopback testing. In this case, number the slices as if they are all TX slices.

In BoW-256 at 16 Gbps/wire, the link in Figure 8 provides a total of 2.0 Tb/s in each direction. In an organic substrate using the hexagonal bump pattern of Figure 5 with a bump pitch is 130 um, the total edge width is 5.2 mm (4.16 mm without AUX and FEC); the depth from the edge is 1.35 mm. In an interposer, if the bump pitch is 40 um, the edge width is 1.60 mm (or 1.28 mm) and the depth is 0.42 mm.

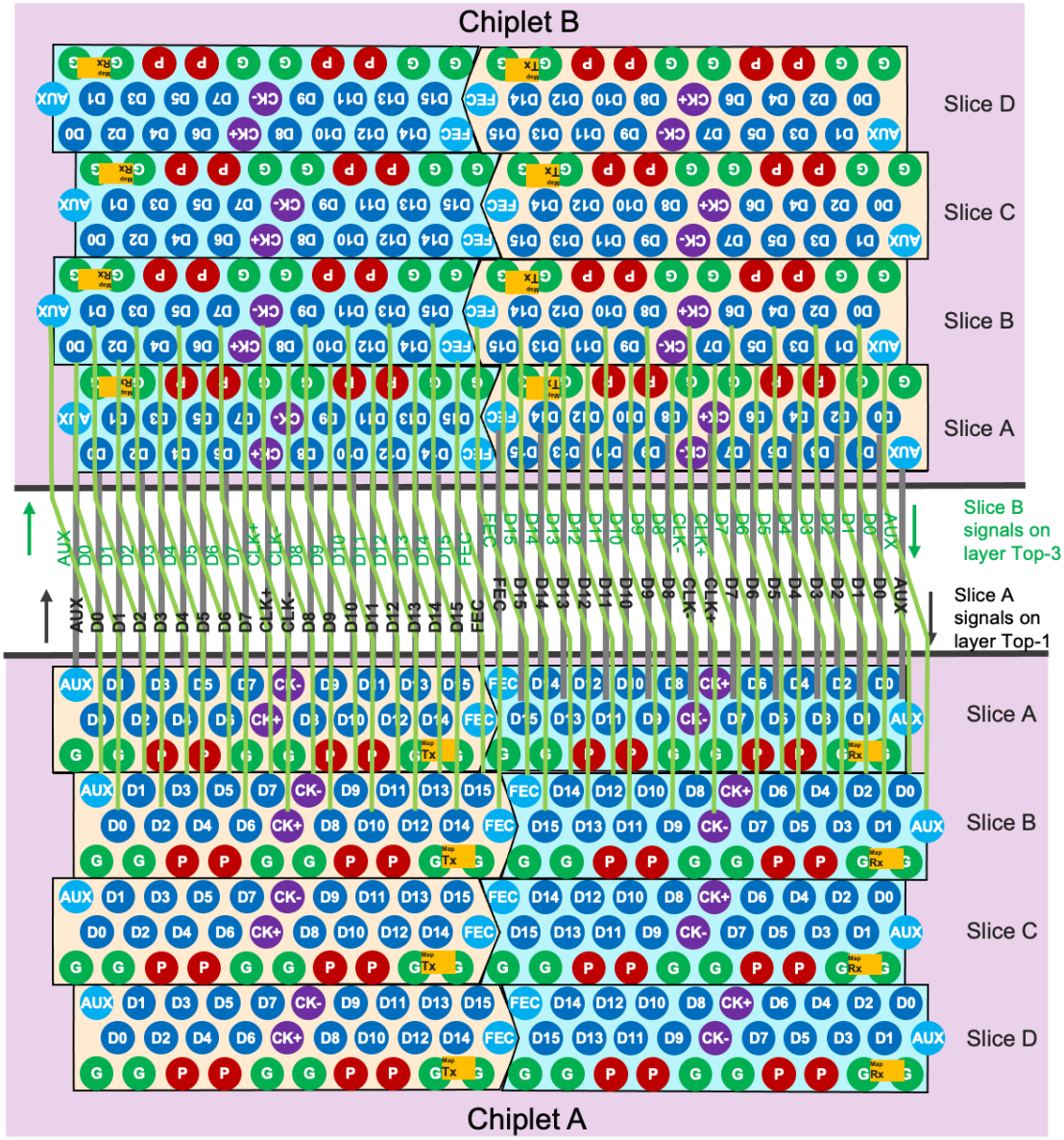

Figure 7. Staggered slices for the densest bump packing

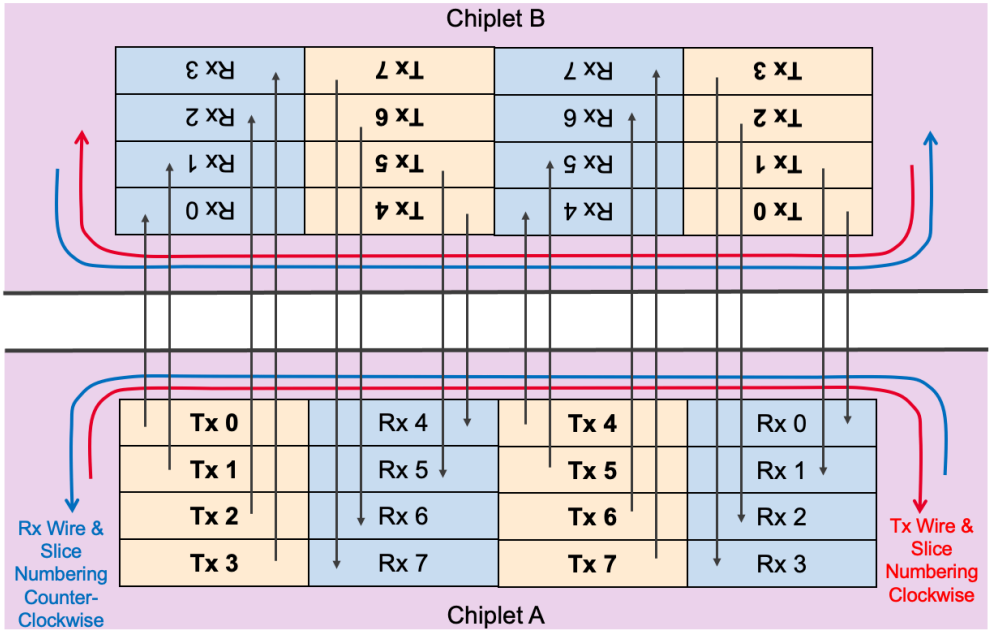

Figure 8. Alternating-Stacks Pattern of TX and RX Slices in a Link

6. BoW PHY Electrical Specifications

In order to ensure interoperability between differing BoW PHY implementations, this chapter provides a set of electrical specifications that all such BoW PHY implementations must meet.

6.1. Voltages and Termination Resistance

All BoW implementations must support signaling based on a 0.75 V "I/O voltage". BoW PHYs may also support higher or lower signaling voltages, but must support 0.75 V based signaling for interoperability.

Note that the simplest implementation is to provide a 0.75 supply voltage to the BoW VDD bumps, but the supply voltage may be different from the I/O voltage as long as the signal voltages meet the specification.

Independently of the I/O voltage, BoW transmitters and receivers must meet the DC termination resistance requirements defined in Table 8. Note that TX/RX termination (output/input) resistance values are skewed low/high compared to the channel impedance in order to ensure that the DC single-ended voltage swing at the RX is never reduced to less than half of the I/O voltage (i.e., 375 mV for a 0.75 V I/O voltage). Note that these termination resistance values must be met with logical 0, logical 1, and mid-scale between logic 0 and logic 1 voltages on the wire between the TX and the RX.

Especially in doubly terminated modes, within-slice variations of termination resistance would directly result in varying swing levels at each pin. Thus, in order to reduce or eliminate the need for per-pin voltage reference adjustment at the RX, Table 8 also specifies requirements on DC termination resistance matching across all I/O's within a given BoW slice. The σ for this variation in the table must be interpreted as capturing within-slice manufacturing variability across worst-

	Unterminated	**Source-Terminated**	**Doubly Terminated**
TX DC Term.	As required to meet TX rise-time	**36 Ω - 50 Ω** (0.72 - 1.0 Z_{chan})	**36 Ω - 50 Ω** (0.72 - 1.0 Z_{chan})
RX DC Term.	-	-	**50 Ω - 69 Ω** (1.0 - 1.38 Z_{chan})
Within-Slice DC Term. Matching	-	σ **= 1.333%** (8% over 6 σ)	σ **= 0.667%** (4% over 6 σ)

Table 8. Transmit and Receive Termination Resistance Requirements vs. Mode

	BoW–32 or BoW-64	**BoW-128**	**BoW-256**
Maximum Equivalent Capacitance (TX or RX)	**1.2pF**	**600fF**	**300fF**

Table 9. Maximum Parasitic Capacitance at a BoW I/O vs. Mode

case voltage/temperature operating conditions, and is expected to be primarily influenced by some combination of transistor and explicit resistor matching (with the mix depending on the circuit implementation).

In doubly terminated modes of operation, the RX termination resistance must be connected to 0V, the I/O voltage, or mid-rail of the I/O voltage (e.g., 375 mV with a 0.75 V I/O voltage). The selection of termination voltage is expected to be static (hardwired) in the RX, and must be specified in the receiver's datasheet. It is expected that Source-Series-Terminated (SST) Transmitters will be largely agnostic to the choice of termination voltage on the receiver.

6.2. ESD

BoW I/O shall be designed to withstand **50 V CDM** (Charged Device Model) and **250 V HBM** (Human Body Model). This requirement is deemed sufficient for intra-package signaling, similar to other die-to-die interface standards.

6.3. Return Loss and Parasitic Capacitance

Since BoW PHYs are targeted for relatively dense and simple realizations, it is expected that the primary frequency-dependent parasitics seen at a PHY's I/Os will be capacitive in nature. Table 9 provides limits on the maximum "equivalent" capacitance allowed on each side of each BoW I/O pin. (E.g., a BoW-128 TX is allowed to have up to 600fF of equivalent capacitance.) Note that while the maximum capacitance specification does increase at lower data-rates, it is recommended that BoW PHY implementations retain as low of a capacitance as practical in order to reduce power consumption and improve signal integrity.

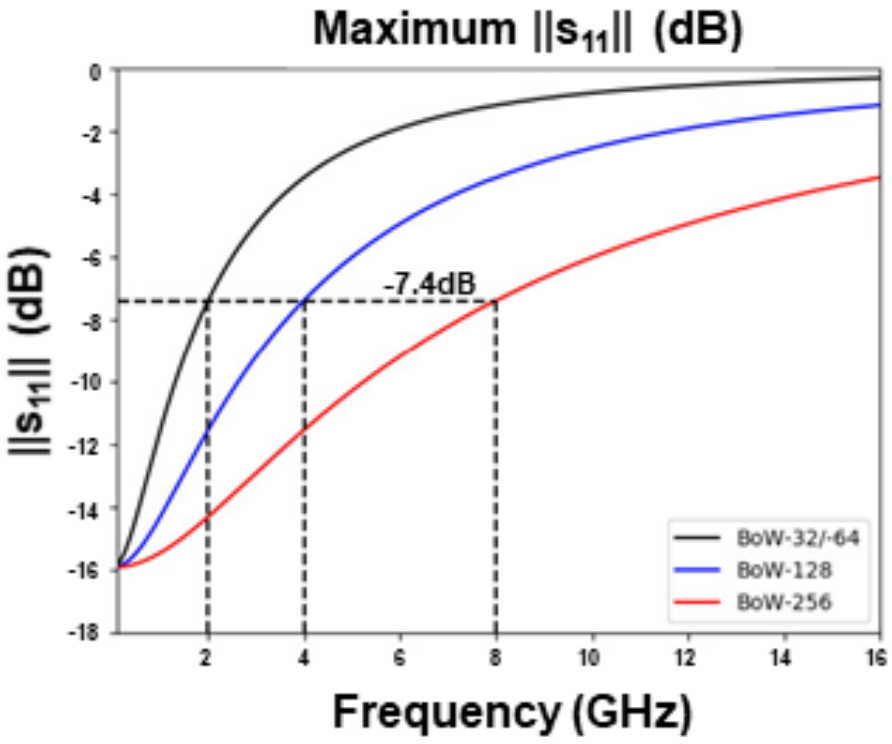

Figure 9. BoW Termination Maximum Return Loss

Since the actual frequency-dependent impedance profile of any given implementation may be comprised of a complex electrical network, compliance with the "equivalent" capacitance metric is formally defined by requiring that the magnitude of the return loss of any BoW I/O must be lower than the maximum limits shown in Figure 9 below. Similarly to DC termination resistance, the maximum s_{11} magnitude in the figure must be met with logical 0, logical 1, and mid-scale between logic 0 and logic 1 voltages on the wire between the TX and RX.

Nov 2021: simulation with example channels show that we either need to reduce the capacitance from 300 to 200 fF (9.8 dB S11) or reduce the Rx eye opening from 50% UI to 30-40% to reach 1e-15 BER. This is unresolved.

6.4. Receiver Bandwidth

While this specification does not place a direct requirement on the bandwidth of a BoW receiver implementation, such receivers should maintain an effective bandwidth of at least $\mathbf{(0.667/T_{bit})}$ **Hz**. For example, for a BoW-256 PHY, the receiver bandwidth is recommended to be at least 10.667 GHz.

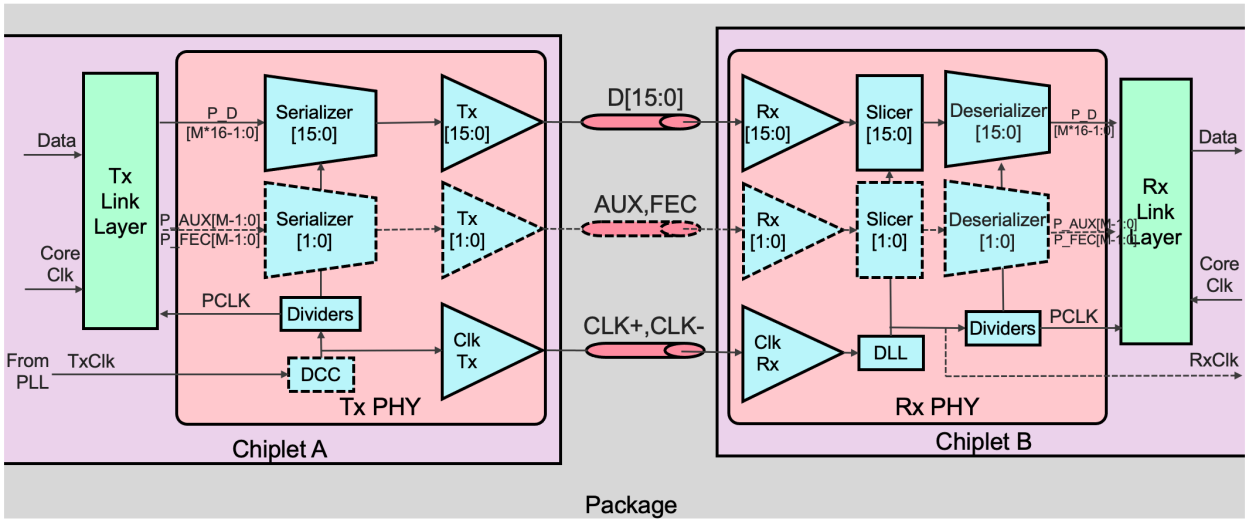

Figure 10. BoW Clock and Data Block Diagram - One TX Slice, One RX Slice

7. BoW PHY Timing Specifications

7.1. Bit Ordering

The PHY TX serializer shall order data this way (referring to Figure 10):

- On the first CLK edge (CLK+ rising) bits P_D[0:15] are sent on wires D[0:15]
- On the second CLK edge (CLK+ falling) bits P_D[16:31] are sent on wires D[0:15]
- and so on to bits P_D[M*16-16:M*16-1].
- Then the cycle repeats.

The RX PHY shall order bits in the same fashion. However, the bits at the RX PHY logic interface P_D[*] may be offset by a multiple of 16 bits from the TX order if the TX and RX PCLK dividers are not aligned. A PHY implementation may provide a way to align the TX and RX dividers, or it may rely on the Link Layer to rotate the RX P_D[*] bits to provide that alignment as part of the training of the Link Layer.

7.2. Clocking

Figure 10 shows the clock and data flow for a single TX slice and a single RX slice. On the TX side, data bits (and optional FEC and AUX bits) come in a wide word from the Link Layer, and are serialized to the line rate. At the RX side, they are sampled with a common slicer clock in most BoW implementations. BoW PHYs may optionally implement per-bit delay adjust or per-bit slicer clock adjust.

BoW PHYs shall be DDR (Double Data Rate) at the chip-to-chip interface: the data bit rate is twice the clock frequency, so data is clocked in on both edges of the clock in the RX slice. BoW PHYs shall be SDR (Single Data Rate) at the logic interface.

Table 10 provides recommended clock and data rates for each BoW mode. The ratio M should be limited to integers, preferably powers of two, and any other ratios should be implemented outside the PHY.

Mode	Data Rate (Gbps)	PCLK (MHz)	Mux Ratio M	Logic Data Width
BoW-32	2	250	8	8x18
		500	4	4x18
		1000	2	2x18
BoW-64	4	250	16	16x18
		500	8	8x18
		1000	4	4x18
		2000	2	2x18
BoW-128	8	500	16	16x18
		1000	8	8x18
		2000	4	4x18
BoW-256	16	500	32	32x18
		1000	16	16x18
		2000	8	8x18

Table 10. Recommended PCLK and Logic Data Rates for Figure 10

Signal	Rate	SDR/DDR
TxClk	2 GHz	
CLK+,CLK- D[15:0],AUX,FEC	2 GHz 4 Gbps	DDR
PCLK P_D[63:0],P_AUX[3:0],P_FEC[3:0]	1 GHz 1 Gbps	SDR

Table 11. Example Clock and Data Rates for Figure 10 with 4 Gbps, M=4

Note that higher PCLK rates (and lower M ratios) help reduce gate count and Link Layer latency, but lower rates are often more power efficient. The best PCLK rate(s) to implement for a particular chiplet will tend to be a function of its process node. For implementations in process nodes at 16 nm and below, supporting 1000 MHz is recommended.

Table 11 provides clock and data rates for an example with 4 Gbps wire data rate and M=4 to support a 1 Gbps data rate at the Link-PHY interface.

The DDR clock TxClk is provided to the TX PHY from elsewhere on Chiplet-A. This may come for example from an on-chip PLL (typically shared across multiple slices) or routed from the RxClk of an RX slice on Chiplet-A. In order to meet duty cycle requirements, a Duty Cycle Corrector (DCC) may be needed in the TX slice. TxClk is used to drive the serializers and provide the output CLK+, CLK- to Chiplet-B.

On the RX side, the PHY must align the slicer clock to sample the data correctly. This may be done with a DLL, adjustable delays, or other methods. If the PHY includes control logic to self-align the slicer clock for correct sampling of the data, the PHYReady signal must be asserted after the logic has determined that such alignment is complete. The RX PHY may output the received CLK as RxClk to the logic interface.

All BoW interfaces shall be source synchronous at the die-to-die interface within a slice. No modes of BoW require per-wire or per-slicer delay adjustments, but such capability may be optionally included.

Clock skew between the slices in each direction of a link likely depends on the implementation of the TxClk distribution to all the TX slices. That is, for the data flow from Chiplet A to Chiplet B, the TxClk distribution on Chiplet A probably dominates the the clock skew of the TX slices on Chiplet A and the clock skew of the RX slices on Chiplet B, and vice versa for flow from B to A. The skew between Tx CLK signals within one direction of a link should be no more than 150 ps/stack along the chip edge. There is no specification of the skew between TxClk on Chiplet A vs. TxClk on Chiplet B nor between different links.

Note that the dividers creating PCLK in each PHY slice are not required to be aligned. This implies that they will tend to have random starting states, leading to additional PCLK misalignment between slices of up to one PCLK period. PHY implementations may optionally include methods to align these dividers.

On both the TX and RX sides, the Link Layer will usually need to include a Clock Domain Crossing (CDC) to align the data between CoreClk and PCLK. The Link Layer must be able to absorb the slice-to-slice clock skew and core clock distribution skew across a whole BoW link. Word alignment across a link need not be supported by the PHY; if required, it should be done in the Link Layer.

7.3. Clock and Data Specifications

7.3.1. Transmitter Maximum Rise-Time

The maximum 20% - 80% rise-time simulated at the output of BoW TX shall not exceed **32% of a UI**. For example, for a BoW-128 Transmitter, the 20% - 80% rise-time shall not exceed 40 ps. This rise-time shall be simulated with the TX driving an ideal load of 50 Ω (Z_{chan}).

7.3.2. Transmitter Jitter

The total jitter simulated between the CLK and any data (D) line at the output of the TX shall not exceed **14% of a UI peak-to-peak at an error rate of 1e-15**. The evaluation of jitter must include all possible TX jitter contributors, including reference clock, clock distribution networks, duty cycle error, DCC jitter, PLL jitter, power-supply noise and switching noise. In order to retain TX design flexibility, this single total jitter specification includes both random and deterministic contributions to jitter. To account for the 1e-15 error rate and peak-to-peak requirement, the total jitter $t_{j,tot}$ must be computed as:

$$t_{j,tot} = t_{j,determinsitic} + 15.9\ \sigma_{tj,random}$$

This jitter must be evaluated for CLK edges that are up to **3 UI** earlier than the CLK edge that launched the data bit being captured at the receiver. This is because even though jitter on the data edges may be correlated with the CLK jitter, the slicer in the RX side is likely to use a different CLK edge due to delays in the RX-side clock alignment circuit (usually a DLL and clock distribution).

In order to properly account for the jitter filtering/peaking that will occur due to the difference in delay between the data launching edge at the TX and the data capturing edge at the RX, when evaluating the transmitter's jitter (and whether it meets the requirements described in this section),

the jitter at the TX output that is **correlated** between the CLK and D lines shall be filtered by the following frequency-dependent transfer function:

$$\mathbf{H_{tx\_jit}(j\omega) = 1\text{-}e^{(-j\omega t_{clk-d})}}$$

where t_{clk-d} is the delay between the CLK edge that launched the data bit and the CLK edge used to capture it. Note that jitter that is not correlated between the CLK and D signals shall **not** be filtered by this transfer function. (I.e., if the CLK signal and a given D signal have completely independent sources of jitter added to them such as non-shared portions of the clock distribution network, those jitter sources shall not be filtered by $H_{tx\_jit}(j\omega)$. Since the total TX jitter after filtering by this transfer function might not be monotonic with t_{clk-d}, and since receiver implementations may realize varying values of t_{clk-d}, a transmitter must meet the 14% of a UI peak-to-peak specification for $\mathbf{t_{clk-d} = T_{bit}}$, for $\mathbf{t_{clk-d} = 2T_{bit}}$, **and** for $\mathbf{t_{clk-d} = 3T_{bit}}$.

7.3.3. Transmitter CLK Edge to D Transition Skew + Jitter

In addition to jitter, BoW TX PHY implementations may introduce skew between the individual D signals and the CLK signals within a slice. The total amount of skew and jitter (as defined in Section 7.3.2) introduced by a BoW TX must be less than **18% of a UI peak-to-peak**. For example, a TX whose total jitter is 14% of a UI (and hence just meets the requirement) is allowed to introduce up to 4% of a UI peak-to-peak skew between CLK and D, while a TX with jitter better than required by this specification is allowed to introduced a larger amount of skew.

Note that this specification shall be simulated directly at the TX output while driving an ideal load of 50 Ω (Z_{chan}).

7.3.4. CLK Receiver Sensitivity to Common-Mode Variations

The timing of a BoW RX PHY's sampling clock edge at the slicer must be modulated by **less than 0.1% of a UI per mV of common-mode variation on CLK+/CLK-**. This sensitivity requirement must be met across any common-mode variation frequency less than or equal to $1/T_{bit}$. For example, the sampling clock edge of a compliant BoW RX would vary by less than 2% of a UI peak-to-peak for peak-to-peak common mode variation on CLK+/CLK- of 20mV.

7.3.5. Receiver Sensitivity and Timing Margin

As indicated in Figure 11 and Table 12, a BoW receiver must meet the required bit-error-rate of 1e-15 when receiving signals with a vertical opening (voltage margin) of at least V_{rx_eye} and horizontal opening (timing margin) of at least t_{rx_eye}. Both V_{rx_eye} and t_{rx_eye} shall include any random and/or statistical noise and error terms introduced by either the channel or the TX at a level that corresponds to 1e-15 probability. Similarly, the receiver's voltage sensitivity (which sets V_{rx_eye}) must also be evaluated at 1e-15 error rate, so the total voltage sensitvity $V_{s,RX}$ shall be computed as:

$$V_{s,RX} = V_{err,deterministic} + 15.9\ \sigma_{Verr,random}$$

Note that the receiver's voltage sensitivity shall take into account all voltage error sources at the receiver, including receiver thermal/flicker noise, supply noise, residual offset, and reference level errors.

Since swing and signal integrity are expected to vary with termination as well as data-rate, the RX voltage sensitivity requirements and minimum timing margin requirements are termination- and rate-dependent, as outlined in Table 12.

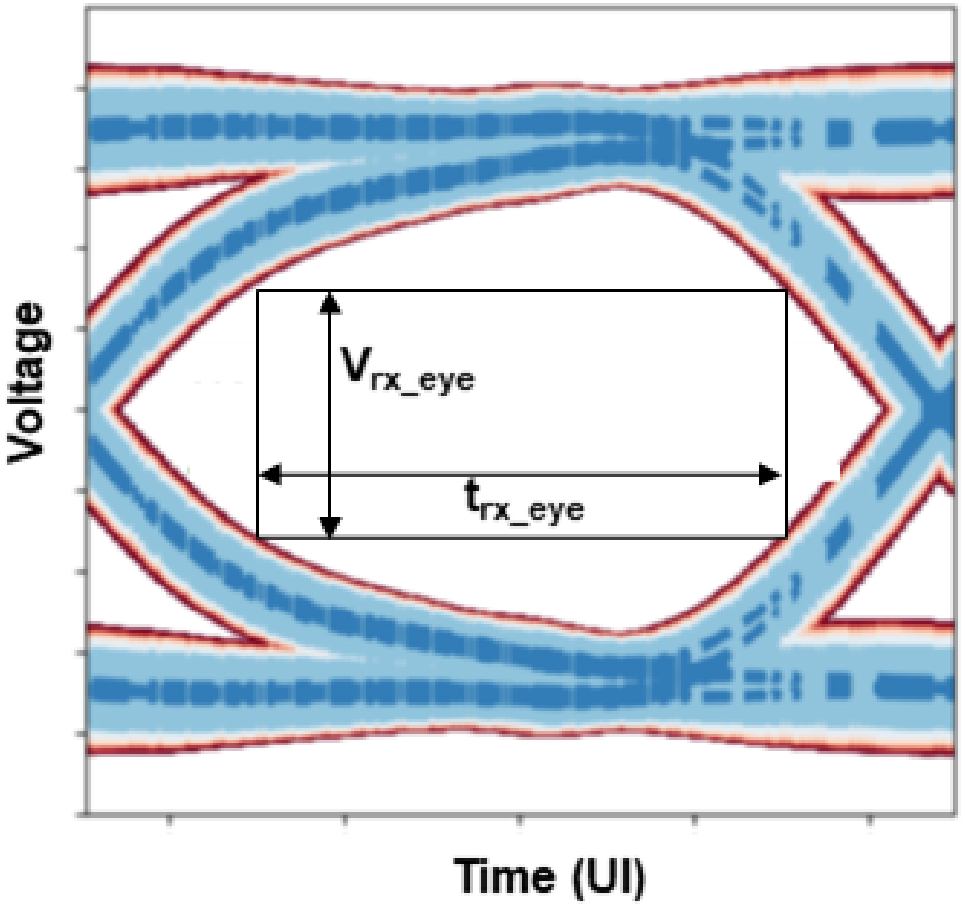

Figure 11. Eye Diagram Definitions

	Unterminated	**Source-Terminated**	**Doubly Terminated**
Maximum RX sensitivity BoW-128, BoW-256 (V_{rx_eye})	**150 mV**	**150 mV**	**75 mV**
Maximum RX sensitivity BoW-32, BoW-64 (V_{rx_eye})	**300 mV**	**300 mV**	**150 mV**
Minimum Timing Margin @ RX bump (t_{rx_eye})	**50% T_{bit}**	**50% T_{bit}**	**50% T_{bit}**

Table 12. Receiver Voltage Sensitivity and Minimum Timing Margin

7.3.6. Overshoot

CLK and data signals must not overshoot more than 25% of the I/O voltage at both the TX and RX ends. For a 0.75 V I/O voltage, they must stay within the range -0.188 V to 0.937 V.
Overshoot depends on Tx and Channel. Overshoot spec protects the Rx from damage. How to handle this?

7.3.7. Slice-to-Clice CLK Skew

The slice to slice clock skew t_{skew} across the width of a BoW link (along the chip edge) should be less than 150 ps/stack. (E.g., for a 4-stack interface, the skew from end to end must be less than 600 ps.) This skew includes only analog delays and specifically does not include any clock-related timing skew due to flip-flops/latches or varying reset states.
This skew is expected to be dominated by the TxClk distribution network.

8. Chip-to-Chip Channel Specifications

With the exception of the maximum skew requirement defined in Section 8.1, BoW does not place any direct requirements on characteristics such as channel loss or crosstalk. Instead, BoW channels are considered compliant if they are able to achieve the required V_{rx_eye} and t_{rx_eye} defined in Section 7.3.5 in conjunction with reference transmitters and receivers that meet all of the requirements provided in Section 6 and Section 7.3. To assist with evaluating compliance of a given channel, open-source software evaluating signal integrity and the overall link budgets with the reference transmitters and receivers will be provided at a future date.

8.1. Channel-Induced CLK Edge to D Transition Skew at RX

Within each slice, a BoW channel must not introduce more than **6.67 ps** of skew between CLK and D lines. This corresponds to 1 mm of length mismatch on a substrate with an ϵ_r of 4.

8.2. Channel Impedance

In laminate packages, the channel characteristic impedance should be between 45 and 55 Ω.

8.3. Example BoW Channel for Doubly-Terminated Links

To provide guidance on the types of channels that are expected to meet the requirements for compliance with the BoW reference receiver and transmitter, this section provides examples of typical loss and crosstalk profiles for doubly-terminated channels supporting 16 Gbps operation (which are most sensitive to channel signal integrity). Note that when operating at lower rates, the frequency axes in the figures below can be scaled with the data-rate relative to 16 Gbps.

8.3.1. Channel Loss

To avoid the need for equalization, a BoW-256 channel will typically need to have lower loss than shown in Figure 12.

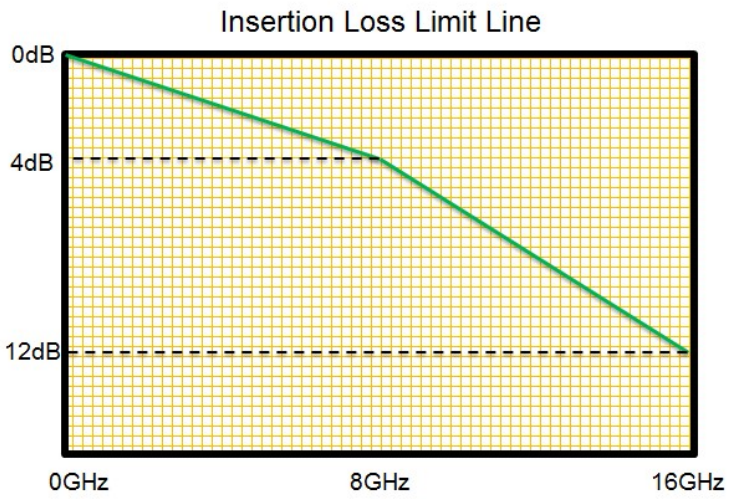

Figure 12. BoW Doubly-Terminated Wire Channel Loss Limit

8.3.2. Crosstalk

The crosstalk in a BoW-256 channel will typically need to be less than that shown in Figure 13. Power-sum crosstalk is the sum of crosstalk power of all aggressors on a target trace. The example limit depicted in Figure 13 corresponds to:

$$\text{XtalkLimit} = -37 * e^{-f/8\text{GHz}} - 10 \text{ dB}$$

9. Reset and Initialization

9.1. External Facilities

These facilities must be provided outside the PHY:

- a Link Controller (LC) which will manage initialization of the Link. It may reside on one of the chiplets of the Link, in a third chiplet in the package or outside the package.
- A communication path from the Link Controller to the PHY slices outside the BoW link. This could be a serial link like SPI or I2C, but this is not specified at this time.
- A source of training pattern data outside the PHY, assumed to be the Link Layer here. This must be able to repetitively transmit an arbitrary 16 bit per wire pattern (256 or 288 bits pattern depending on inclusion of FEC+AUX) required by the RX slice for clock alignment as specified in the datasheet for the RX PHY.
- The PHYReset input to each PHY shall be asserted upon powerup. It may also be asserted by commands from the LC.

An example topology is shown in Figure 14. The BoW interface communicates to interface and core logic (I&C) blocks.

Add another figure with the LC embedded rather than external

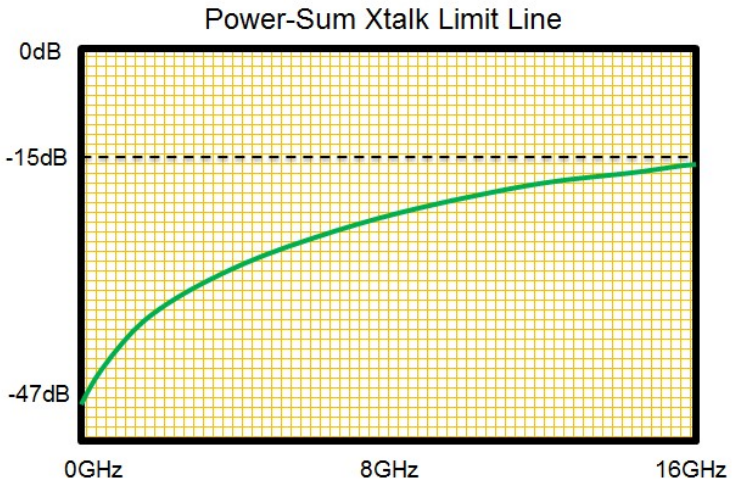

Figure 13. BoW Doubly-Terminated Wire Crosstalk Limit

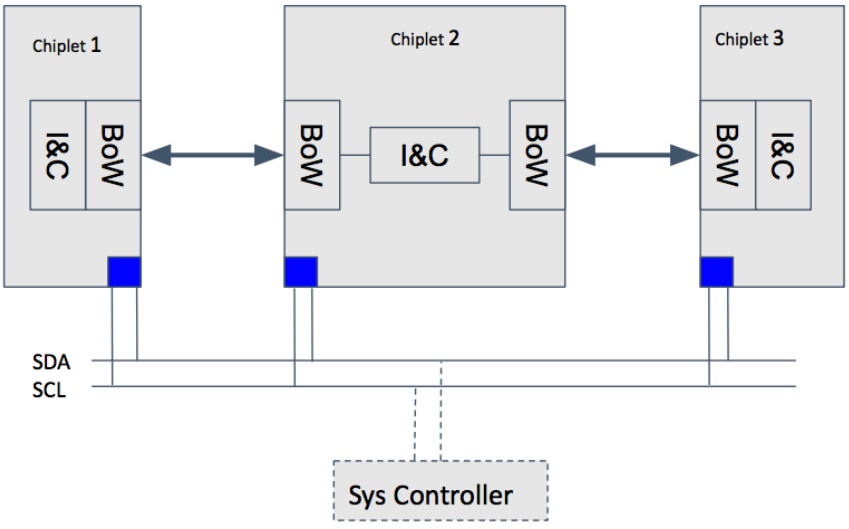

Figure 14. Example BoW System Configuration

9.2. Initialization Sequence

A TX-RX Link shall be brought up as follows:

1. The Link Controller (LC) performs any needed configuration of the PHY slices via the APB interface. This is implementation dependent
2. The LC de-asserts PHYReset to the TX PHY slices
3. Once its TX clock stabilizes, each TX PHY slice asserts PHYReady to the LC
4. When all TX PHY slices are ready, the LC signals the TX Link Layer to send the training pattern (repeating indefinitely) specified by the RX PHY
5. The LC de-asserts PHYReset to the RX PHY slices
6. Each RX PHY slice performs clock and data alignment and signals PHYReady to the LC when done
7. When all RX PHY slices are ready, the LC signals the TX and RX Link Layers that they can proceed with channel bonding

Implementation dependent:

- Whether the up and down links are initialized one at a time or in parallel
- How the signals from the the LC get from and to the PHYReady and PHYReset pins of the PHY
- How the Link Layer performs channel bonding or start of data transmission
- Any PHY registers required to implement this process - these are an implementation choice.

9.3. Unspecified Items

- There is no low-power standby mode defined.
- There is no specification for when a PHY should de-assert its PHYReady pin. PLL or DLL losing lock are possible causes.
- There is no definition of what occurs if the PHY does de-assert PHYReady
- There is no definition of what should be done with unused PHYs (that are on the chip but have no partner on another chiplet)
- There is no definition of logical addressing of chiplets, Links or slices
- Possible use of PRBS patterns for training

10. Configuration

PHY configuration is implementation dependent. It may include:

- TX vs RX for configurable slices
- PLL, DLL, DCC or similar circuit configuration

PHY configuration may be hardwired in the chiplet implementation, or it may be programmable.

10.1. Link Training

Link training will be addressed in a future revision of the spec

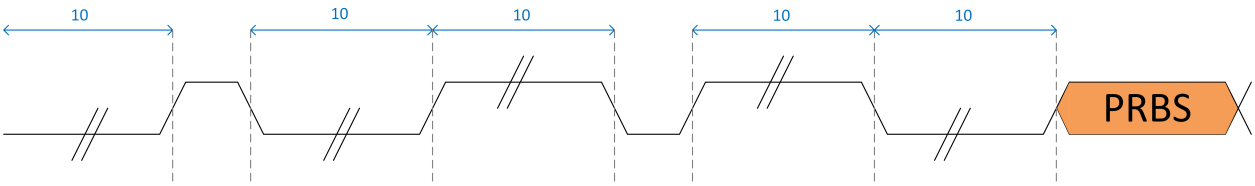

Figure 15. Stress Test Pattern

11. Control Register Mapping

The interface control registers are implementation dependent. The registers shall be fully documented in the PHY datasheet.

12. Testability

12.1. Test Patterns

- Should we make any or all of these test patterns mandatory to facilitate interoperability?
- Syncing a receiver to a PRBS-31 pattern is slow without an agreed start time. How do other specs do this?

Test patterns should be programmable to repeat indefinitely.

Suggested test patterns are:

- PRBS-9 Pattern, defined by polynomial of $X^9 + X^5 + 1$
- PRBS-31 Pattern, defined by polynomial of $X^{31} + X^{28} + 1$
- Isolated 1 and 0 pattern to test DC wander and single bit response:
  - [‘0’] X 10 + ‘1’ + [‘0’] X 10 + [‘1’] X 10 + ‘0’ + [‘1’] X 10 + [‘0’] X 10
  - This can be prepended to a PRBS pattern as seen in Figure 15

12.2. Loopback Test

A BoW interface may implement loopback testing for several use cases: at chiplet wafer-sort test, post-assembly package test, and debug/validation.

Wafer sort tests are currently only practical for the BoW interface with regular bump pitches (~130 μm), where ATE (automatic testing equipment) probe boards with matching pin pitches are available. Microbump probes will require additional effort.

Unidirectional links should support open-loop testing. In TX open loop testing, shown in Figure 16, Chiplet-A transmits a known test pattern (PRBS9 or PRBS31) to a golden reference receiver through the ATE load board. The received pattern should be verified in the ATE load board.

RX open loop testing, shown in Figure 17, is used for a link where the DUT is only a receiver. A golden reference TX transmits a known pattern (PRBS9 or PRBS31) through the channel to the chiplet. The received pattern should be analyzed for quality and functional tests.

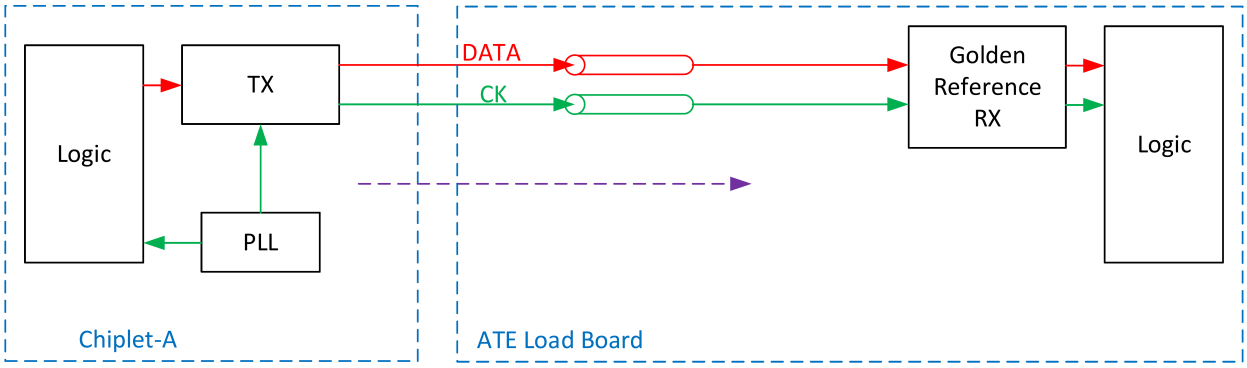

Figure 16. Open loop TX wafer test

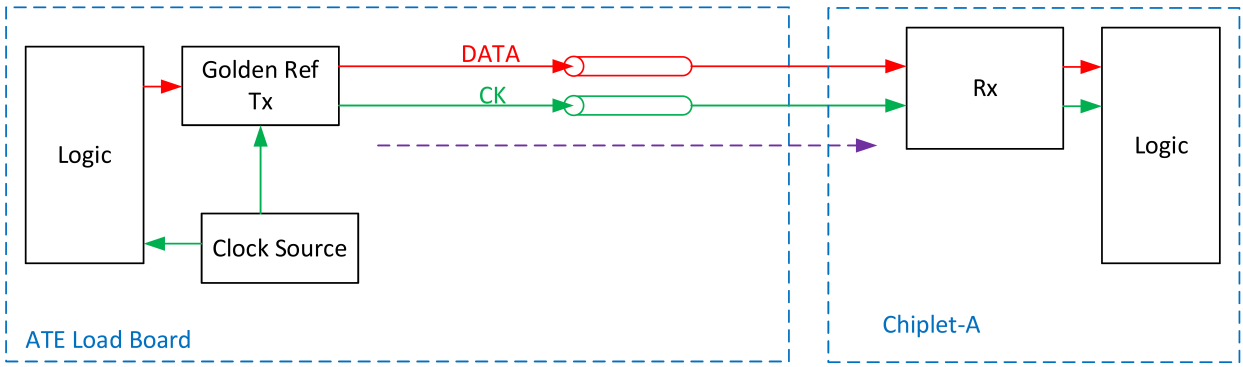

Figure 17. Open loop RX wafer test

The logic for generating and testing the PRBS sequences is outside the PHY, e.g., in the Link Layer.

In bidirectional links, loopback tests can be implemented in several modes:

- Slice-to-slice short loopback
  - Data is looped back within the chip from a TX slice to an RX slice using on-chip switching (shown in Figure 18). The short loopback path is configured by the ATE using implementation-dependent registers.
  - Loopback can be implemented before the PHY serializer, between the serializer and the output buffer, and/or at the bumps.
- Intra-slice short loopback
  - A single slice containing both RX and TX paths sharing the same bumps can perform on-chip loopback testing simply by turning on both the RX and TX paths at once. This has more on-chip circuitry, but allows loopback testing with no switches or extra lines connected to the bumps other than the TX driver tristate switches. Figure 18 applies, except there is only one shared set of bumps for a TX/RX slice.

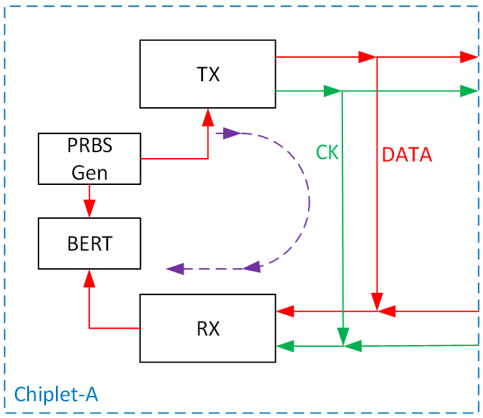

Figure 18. Short loopback testing

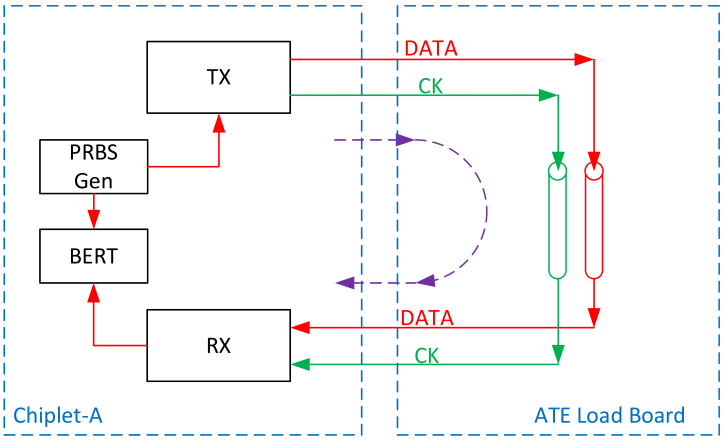

Figure 19. Long loopback testing

- Long loopback
  - The PRBS pattern is generated by chiplet-A, sent over the replica channel on the ATE load board which loops it back (shown in Figure 19). The received pattern should be passed to a bit error rate tester (BERT) to analyze the performance of the link with off-chip data and clock wires.

Both loopback modes can potentially be used for in-field validation bring-up and test. Cooperation across chiplets will be required to execute these tests in the field. Open-loop testing requires the use of a fixed test pattern recognized by both ends and is the only option for unidirectional links. Long loopback mode can be implemented on interposer or organic laminate for validation/verification purposes.

Figure 20 shows how a long loopback mode is executed across two chiplets for in-field validation and test where TX and RX are in different chiplets. Furthermore, this configuration can be expanded to loop back the data from the transmitter of chiplet-A to the receiver of chiplet-A.

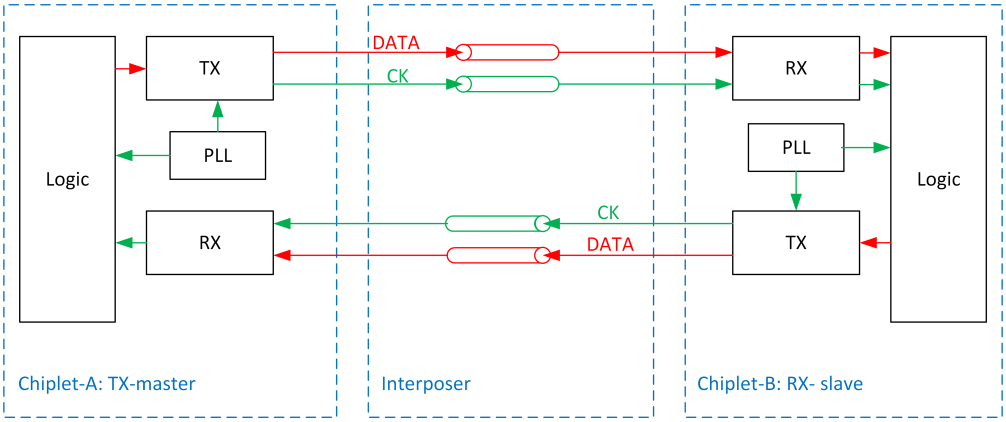

Figure 20. Chiplet-to-chiplet long loopback

13. BoW in an ODSA Design

Chiplet-based designs require logical connectivity between the die in a single package, in addition to physical connectivity. This section provides an overview of how the Open Domain-Specific Architecture stack can be used as an underlay for popular transaction protocols.

13.1. BoW for Common Transaction Protocols

Two connected die in a multi-chiplet device need to exchange logical information. The ODSA aims to define an open physical and logical interface for chiplets, as shown in Figure 21 to enable chiplets from multiple vendors to interoperate and be integrated in a multi-die package. The Bunch of Wires is an open D2D PHY option in the interface. The logical component of the ODSA interface aims to support protocols used for the two most common chiplet use cases, package aggregation and die disaggregation across a wide range of open and proprietary D2D PHYs such as PCIe, CXL, CCIX, AXI and proprietary streaming protocols.

The ODSA stack abstracts the PHY layer from the logical interface by using the well-defined abstraction interfaces PIPE and LPIF. Any logic transaction controller, such as a PCIe controller, that supports a PIPE or LPIF interface can use any D2D PHY that also supports that interface as its physical layer. As shown in Figure 21, the BoW interface may receive data through either the PIPE or LPIF interfaces to support common transaction protocols. For this use case, some BoW-specific adapter logic will be needed to support the requirements of PIPE or LPIF. The specifications for these adapters are outside the scope of this document. Figure 22 shows how the BoW with an PIPE adapter can be interfaced to a PCIe controller.

Need to remove “serializer” and “deserializer” from the labels in Figure 22 - these are part of the PHY, not the PIPE adaptor.j

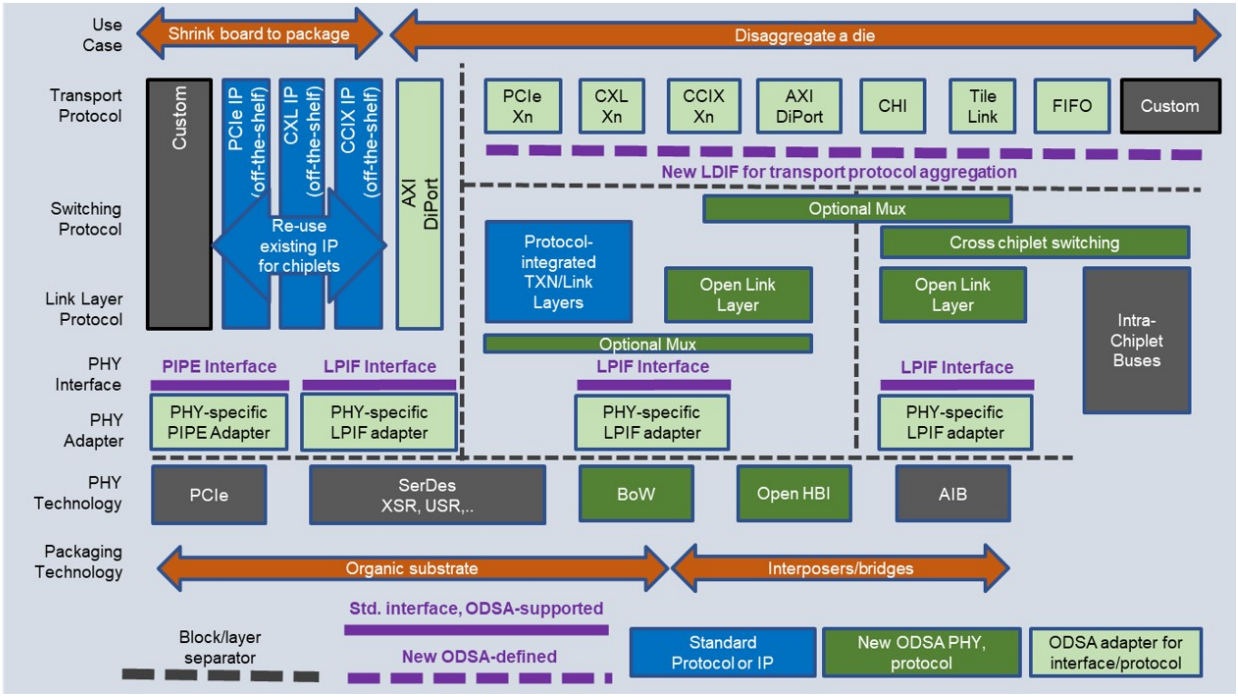

Figure 21. The BoW PHY in the ODSA Stack

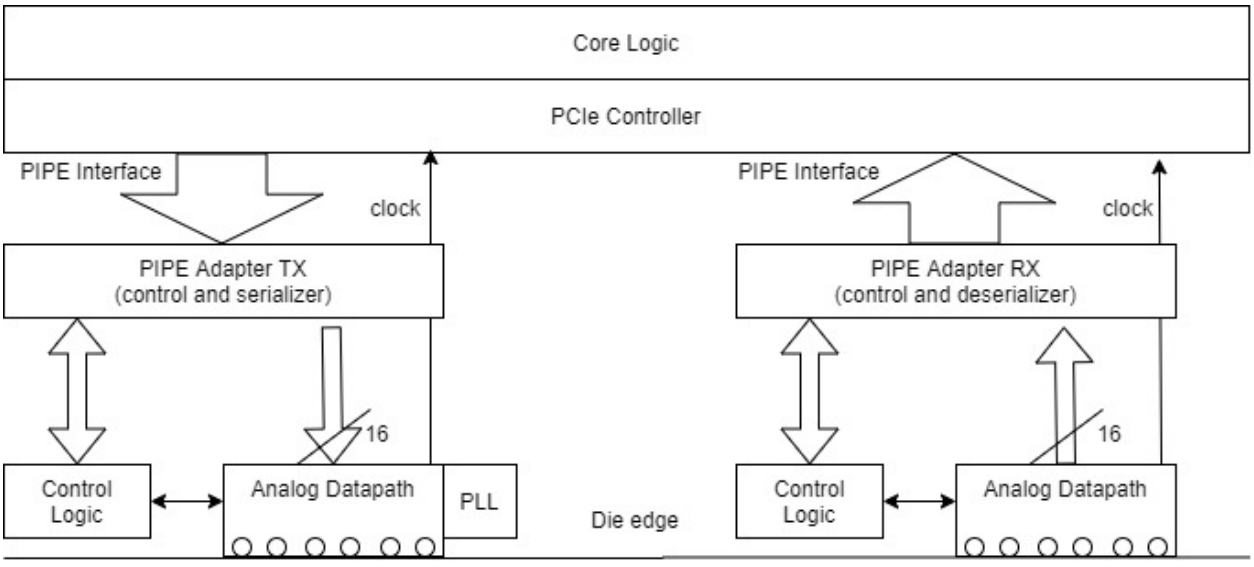

Figure 22. BoW with a PIPE adapter for PCIe transactions