ODSA AXI5-Lite D-32 Interface Profile

Revision A

Version 0.7.0

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Introduction

This specification describes Revision A (or Rev A) of the AXI5-Lite D-32 interface profile for the ODSA Transaction and Link Layer Specification for BoW Interfaces. Per that specification, the following are defined in this document:

- The inclusion or exclusion of optional fields on the interface protocol channels
- The width of each field on the interface protocol channels
- The bundling and mapping of fields into the payloads of various TLP types
- The use of the auxiliary field in the TLP header for each TLP type
- The definition of any additional TLP types for control information
- The assignment of TLP types into TLP streams
- The bundling of TLP streams into a TLP class
- The support for credit (CRD) and message (MSG) TLPs
- The number and assignment of virtual wires and the reset state of each virtual wire

Additional information about the interface profile is provided in the following sections.

Overview

The AXI5-Lite D-32 profile supports the AXI5-Lite interface protocol, as defined by AXI Issue G, with a 32b data width. The profile is classified into TLP classes, streams, and types as shown below:

TLP Class	TLP Stream	TLP Type	TlpHdr Type
AXI5-Lite D-32	A5LAWW	AWW32	0x08
	A5LB	B	0x09
	A5LAR	AR	0x0A
	A5LR	R32	0x0B
	None	A5LCRD	0x0C

AXI5-Lite D-32 Profile TLP Classes, Streams, and Types

The AXI5-Lite D-32 profile does *not* support CRD TLPs but does support MSG TLPs. In addition, the profile defines a number of virtual wires.

Implementations are characterized as either a *spoke controller* or a *hub controller*. The subsets of the profile supported by each are described in the remaining sections.

AXI5-Lite D-32 Class

AXI5-Lite D-32 transfers are encapsulated into TLPs based on the signals on the interface with the SoC on-die interconnect. The following constraints apply:

- AxID is 8b
- AxADDR is 52b

The AXI5-Lite D-32 profile classifies AXI5-Lite TLPs into one of four TLP streams: A5LAWW, A5LB, A5LAR, and A5LR.

For AXI5-Lite TLPs, the Aux field in the TLP header grants credits for the various TLP streams:

4	3	2	1	0
Reserved	A5LR[0]	A5LAR[0]	A5LB[0]	A5LAWW[0]

A one in bits 0 through 3 indicates that a credit has been granted for the corresponding stream, while a zero indicates that no credits have been granted. Bit 4 is *reserved* and *must* be zero.

An A5LCRD TLP is also defined to transmit additional credits for each of the TLP streams.

The AXI5-Lite class effectively connects a requester implemented on a hub with a responder implemented on a spoke. A hub controller transmits the following TLP streams:

- A5LAWW
- A5LAR

A spoke controller transmits the following TLP streams:

- A5LB
- A5LR

The streams transmitted by one type of controller are received by the other type. Both types transmit and receive A5LCRD TLPs (described below).

A5LAWW Stream

The A5LAWW stream consists of AWW32 packets, described below.

AWW32 TLP

AWW32 TLPs support 32b AXI5-Lite write data. The format for the AWW32 TLP is illustrated below:

AWW32		
Field	**Width**	**Bits**
AWID	8	[105:98]

AWADDR	52	[97:46]
AWPROT	3	[45:43]
AWSIZE	3	[42:40]
WDATA	32	[39:8]
WSTRB	8	[7:0]

Note: Fields highlighted in orange are reordered relative to the order of the signal lists in the AXI specification.

A5LB Stream

The A5LB stream consists of B packets, described below.

B TLP

The format for the B TLP is illustrated below:

B		
Field	**Width**	**Bits**
BID	8	[9:2]
BRESP	2	[1:0]

A5LAR Stream

The A5LAR stream consists of AR packets, described below.

AR TLP

The format for the AR TLP is illustrated below:

AR		
Field	**Width**	**Bits**
ARID	8	[65:58]
ARADDR	52	[57:6]
ARPROT	3	[5:3]
ARSIZE	3	[2:0]

Note: Fields highlighted in orange are reordered relative to the order of the signal lists in the AXI specification.

A5LR Stream

The A5LR stream consists of R32 packets, described below.

R32 TLP

The format for the R32 TLP is illustrated below:

R32		
Field	**Width**	**Bits**
RID	8	[41:34]
RDATA	32	[33:2]
RRESP	2	[1:0]

Miscellaneous TLPs

The AXI5-Lite TLP class defines an A5LCRD TLP that combines with the Aux field in the TLP header to grant large numbers of credits for each stream. The TLP payload for a A5LCRD TLP is defined as follows:

13 12	11 9	8 6	5 3	2 0
Reserved	A5LR[3:1]	A5LAR[3:1]	A5LB[3:1]	A5LAWW[3:1]

The TLP payload and the Aux field transfer up to 15 credits via a 4b value formed by concatenating a field in the TLP payload with the corresponding bits in the Aux field. For example, A5LR[3:0] represents 0 to 15 A5LR credits, where bits [3:1] are expressed in the TLP payload and bit [0] is expressed in the Aux field.

Virtual Wires

The AXI5-Lite D-32 profile supports 32 virtual wires between the spoke controller to the hub controller and 32 virtual wires between the hub controller to the spoke controller. The reset state for all virtual wires is 0.