EE3113 Homework Assignment-2

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EE18BTECH11014

Note: Mathematical Explanations for some of the questions are at the end.

1 1.MOSFET Resistance

Specifications:

$$\frac{W}{L} = 240/180 \tag{1}$$

$$W = 240nm, L = 180nm \tag{2}$$

$$V_{DD} = 1.8 \text{ Volts}, C = 1pF \tag{3}$$

$$\text{Voltage Drop across on Capacitor} = 1.8 \text{ Volts} \tag{4}$$

$$R = dV_{DS}/dI_D \tag{5}$$

1.1 1a

1.1.1 N-MOSFET

SPICE Netlist:

```
Question-1 for N-MOSFET

* Model
.include "TSMC180.lib"
.model nch_tt nmos

* Circuit
Vdd     G       0       DC      1.8
V       1       D       DC      0
M       D       G       0       0       nch_tt W=240n L=180n
C       1       0       1p

* Analysis
.tran   0.1p    50n

* Results
.ic     V(1) = 1.8
.control
run
let ID = V#branch
plot    ID vs V(D)
plot    V(D)/ID vs V(D)
.endc

.end
```

Results:

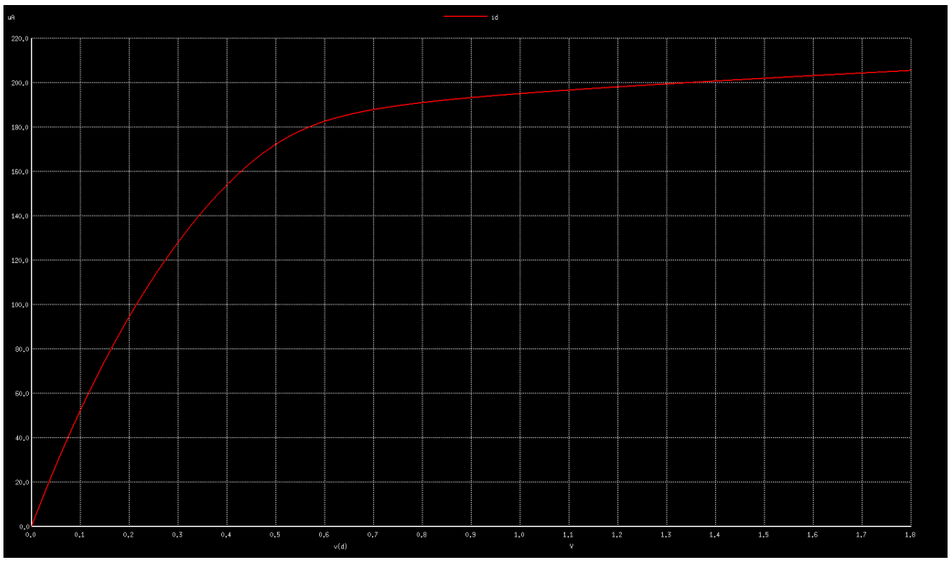


Figure 1: I_D vs V_{DS} Characteristics of N-MOSFET

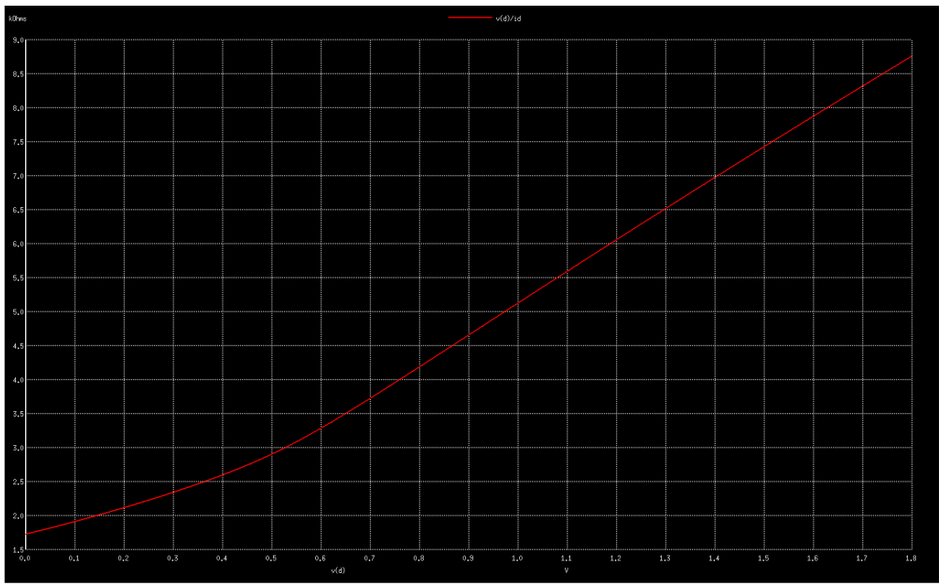


Figure 2: R vs V_{DS} Characteristics of N-MOSFET

1.1.2 P-MOSFET

SPICE Netlist:

```
Question-1 for P-MOSFET

* Model
.include "TSMC180.lib"
.model pch_tt pmos

* Circuit
Vdd     G       0       DC      -1.8
V       1       D       DC      0
M       D       G       0       0       pch_tt W=240n L=180n
C       1       0       1p

```

```
* Analysis
.tran  0.1p   50n

* Results
.ic    V(1) = -1.8
.control
run
let ID = V#branch
plot   ID vs V(D)
plot   V(D)/ID vs V(D)
.endc

.end
```

Results:

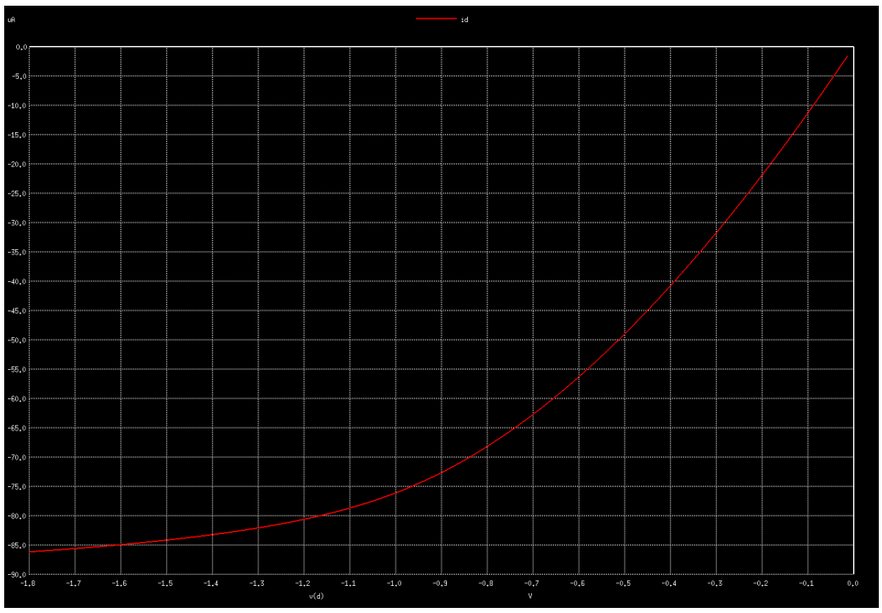


Figure 3: I_D vs V_{DS} Characteristics of P-MOSFET

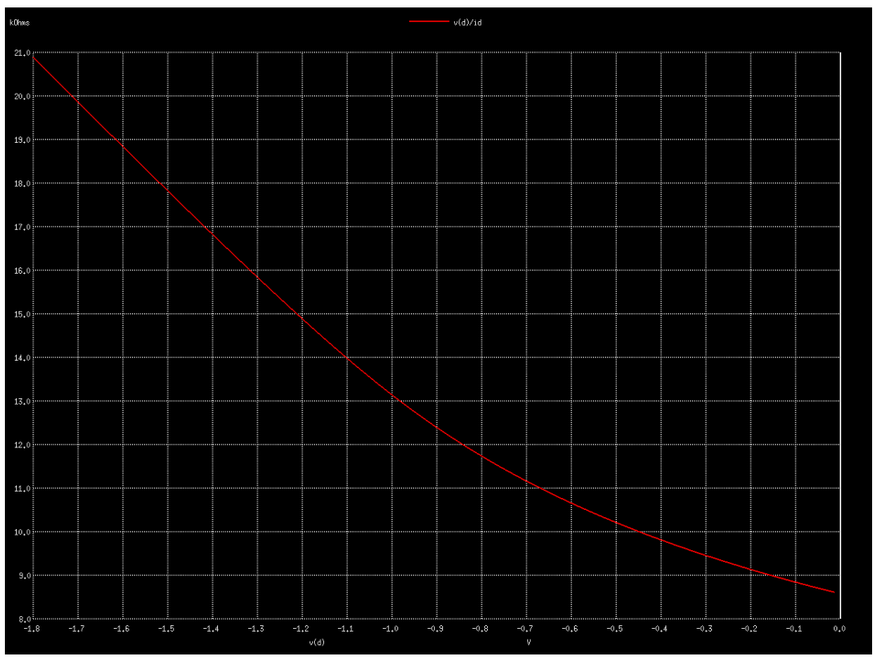


Figure 4: R vs V_{DS} Characteristics of P-MOSFET

1.2 1b

$$R_{eq} = 0.5 \times \left[R(V_{DS} = \frac{V_{DD}}{2}) + R(V_{DS} = V_{DD}) \right] \tag{6}$$

1.2.1 N-MOSFET

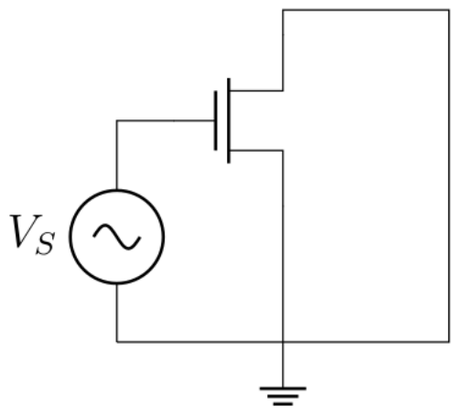
V_{GS} (in Volts)	$R\,(V_{DS} = 0.5V_{DD})$ (in Ω)	$R\,(V_{DS} = V_{DD})$ (in Ω)	R_{eq} (in Ω)
1.8	4660	8772.73	6616.4
1.5	5235.29	9803.92	7519.605
1.2	6463.67	12063.3	9263.485
0.9	10320	18620	14470
0.6	47070.7	80000	63535.35

1.2.2 P-MOSFET

V_{GS} (in Volts)	$R\,(V_{DS} = 0.5V_{DD})$ (in Ω)	$R\,(V_{DS} = V_{DD})$ (in Ω)	R_{eq} (in Ω)
-1.8	12393.9	20878.8	16636.35
-1.5	16062.5	27541.7	21802.1
-1.2	23762.7	41355.9	32559.3
-0.9	44793.8	79278.4	62036.1
-0.6	178958	321277	250117.5

There is a huge difference between values in **Table 3.3** of Reference Book and our Values, is because of the $\frac{W}{L}$ ratio between the MOSFETs.

2 2.MOSFET Capacitance



Specifications for Short Channel MOSFET:

$$L = 180 \text{ nm} \tag{7}$$

$$W = 450 \text{ nm} \tag{8}$$

Specifications for Long Channel MOSFET:

$$L = 10 \ \mu\text{m} \tag{9}$$

$$W = 25 \ \mu\text{m} \tag{10}$$

Calculations:

$$V_{applied} = V_{CM} + V_0 \sin(\omega t) \tag{11}$$

$$V_0 = \frac{1}{2\pi f} = \frac{1}{\omega} \tag{12}$$

$$I = CV_0\omega \cos(\omega t) = C\cos(\omega t) \tag{13}$$

$$C = I(t = \frac{2\pi}{\omega}) \tag{14}$$

For plotting Gate Capacitance vs V_{GS}, $V_{GS} = V_{CM}$ is varied from $[-1.8, 1.8]$ Volts.

2.1 2a

Assuming,

$$f = 100 \text{ Hz} \tag{15}$$

$$V_0 = \frac{1}{2\pi f} = 0.00159154943 \text{ Volts} \tag{16}$$

$$V_0 \approx 0.0016 \text{ Volts} \tag{17}$$

2.1.1 Long Channel N-MOSFET

SPICE Netlist:

```
Question-2a Long Channel N-MOSFET

* Model
.include "TSMC180.lib"
.model nch_tt nmos

* Circuit
Vs      G       1       AC      SIN(0 0.00159154943 100)
Vcm     1       0       DC      -1.8
M       0       G       0       0       nch_tt W=25u L=10u

* Results
.control
run

let Vg = -1.8
let X = vector(180)
let Y = vector(180)

while Vg < 1.81
        alter @Vcm Vg
        tran    10u     10m
        meas    tran    Capacitance    FIND    Vs#branch      AT = 10m
        let X[50*(Vg+1.8)] = Vg
        let Y[50*(Vg+1.8)] = -Capacitance

        let Vg = Vg + 0.02
end
plot    Y vs X

.endc
.end
```

2.1.2 Short Channel N-MOSFET

SPICE Netlist:

```
Question-2a Short Channel N-MOSFET

* Model
.include "TSMC180.lib"
.model nch_tt nmos

* Circuit
Vs      G       1       AC      SIN(0 0.00159154943 100)
Vcm     1       0       DC      -1.8
M       0       G       0       0       nch_tt W=450n L=180n

* Results
.control
run

let Vg = -1.8
let X = vector(180)
let Y = vector(180)
```

```
19
20 while Vg < 1.81
21        alter @Vcm Vg
22        tran    10u     10m
23        meas    tran    Capacitance    FIND    Vs#branch      AT = 10m
24        let X[50*(Vg+1.8)] = Vg
25        let Y[50*(Vg+1.8)] = -Capacitance
26
27        let Vg = Vg + 0.02
28 end
29 plot    Y vs X
30
31 .endc
32 .end
```

Results:

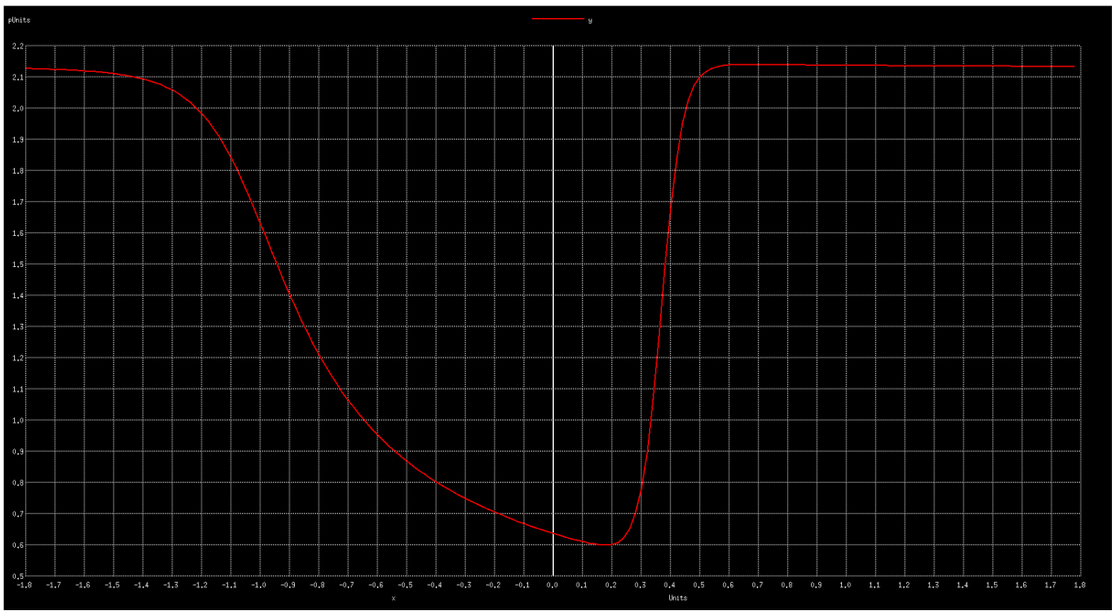


Figure 5: C vs V_G for Long Channel Device

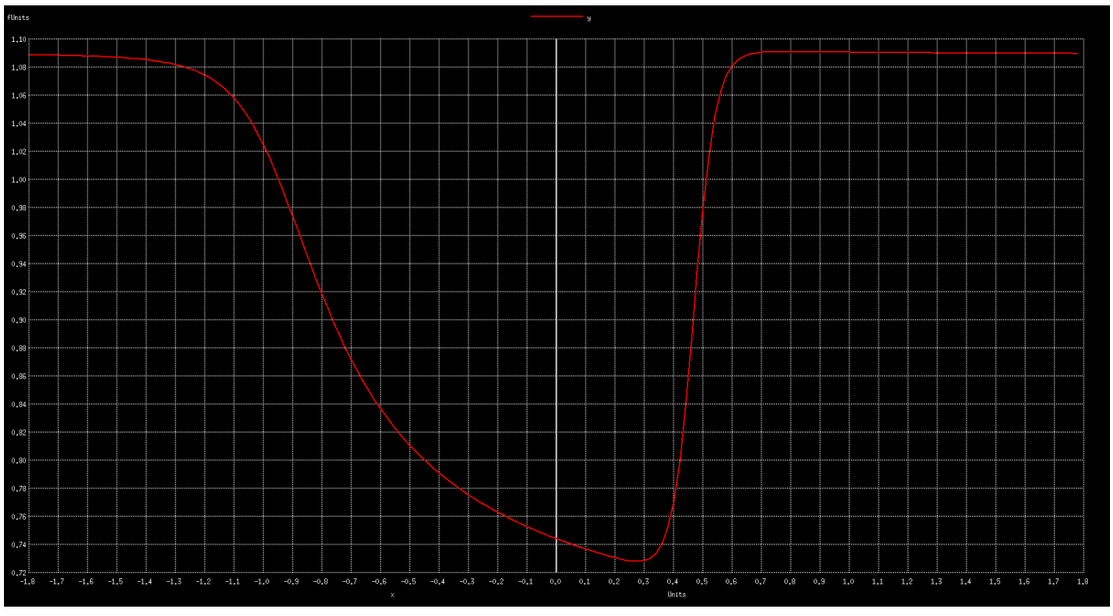


Figure 6: C vs V_G for Short Channel Device

2.2 2b

2.2.1 Long Channel N-MOSFET for f=10MHz

SPICE Netlist

```
Question-2b Long Channel N-MOSFET for f = 10MEG Hz

* Model
.include "TSMC180.lib"
.model nch_tt nmos

* Circuit
Vs      G       1       AC      SIN(0 0.000000015915 10MEG)
Vcm     1       0       DC      -1.8
M       0       G       0       0       nch_tt W=25u L=10u

* Results
.control
run

let Vg = -1.8
let X = vector(180)
let Y = vector(180)

while Vg < 1.81
        alter @Vcm Vg
        tran    1n      0.1u
        meas    tran    Capacitance    FIND    Vs#branch      AT = 0.1u
        let X[50*(Vg+1.8)] = Vg
        let Y[50*(Vg+1.8)] = -Capacitance

        let Vg = Vg + 0.02
end
plot    Y vs X

.endc
.end
```

Results:

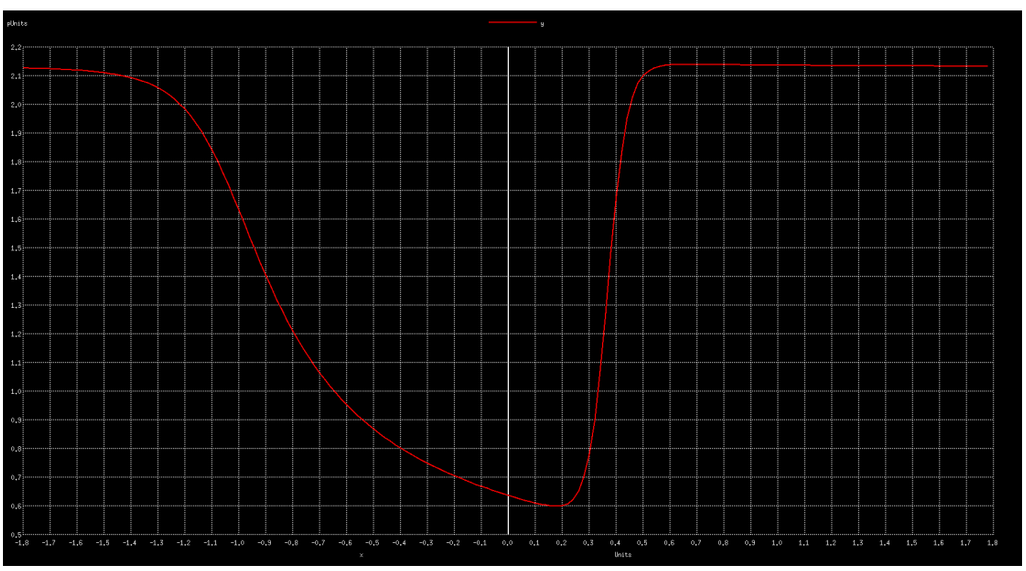


Figure 7: C vs V_G for Long Channel Device for $f = 10M$Hz

2.2.2 Short Channel N-MOSFET for f=10MHz

SPICE Netlist

```
Question-2b Short Channel N-MOSFET for f = 10MEG Hz

* Model
.include "TSMC180.lib"
.model nch_tt nmos

* Circuit
Vs      G       1       AC      SIN(0 0.000000015915 10MEG)
Vcm     1       0       DC      -1.8
M       0       G       0       0       nch_tt W=450n L=180n

* Results
.control
run

let Vg = -1.8
let X = vector(180)
let Y = vector(180)

while Vg < 1.81
        alter @Vcm Vg
        tran    1n      0.1u
        meas    tran    Capacitance    FIND    Vs#branch      AT = 0.1u
        let X[50*(Vg+1.8)] = Vg
        let Y[50*(Vg+1.8)] = -Capacitance

        let Vg = Vg + 0.02
end
plot    Y vs X

.endc
.end
```

Results:

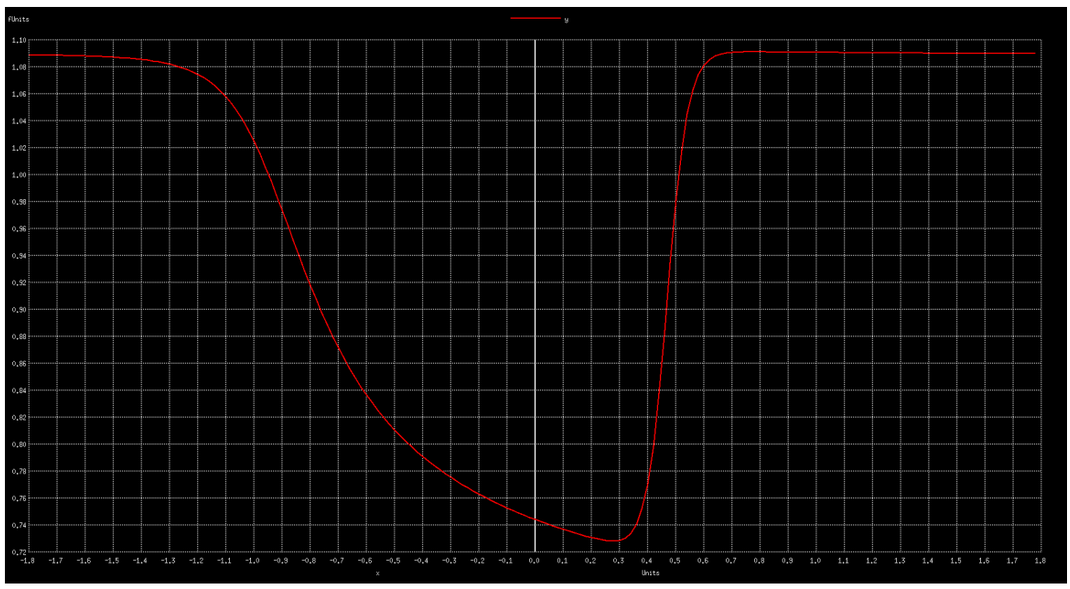


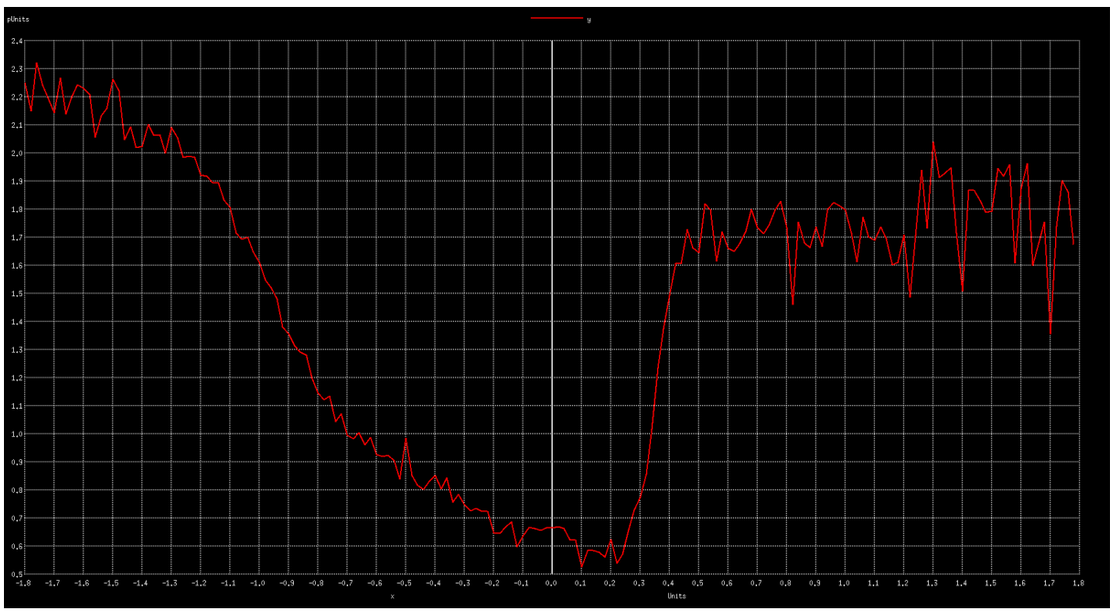
Figure 8: C vs V_G for Short Channel Device for $f = 10M$Hz

2.2.3 Long Channel N-MOSFET for f=10GHz

SPICE Netlist:

```
Question-2b Long Channel N-MOSFET for f = 10G Hz

* Model
.include "TSMC180.lib"
.model nch_tt nmos

* Circuit
Vs      G       1       AC      SIN(0 0.000000000015915 10G)
Vcm     1       0       DC      -1.8
M       0       G       0       0       nch_tt W=25u L=10u

* Results
.control
run

let Vg = -1.8
let X = vector(180)
let Y = vector(180)

while Vg < 1.81
        alter @Vcm Vg
        tran    5p      10.1n
        meas    tran    Capacitance    FIND    Vs#branch      AT = 10n
        let X[50*(Vg+1.8)] = Vg
        let Y[50*(Vg+1.8)] = -Capacitance

        let Vg = Vg + 0.02
end
plot    Y vs X

.endc
.end
```

Results:

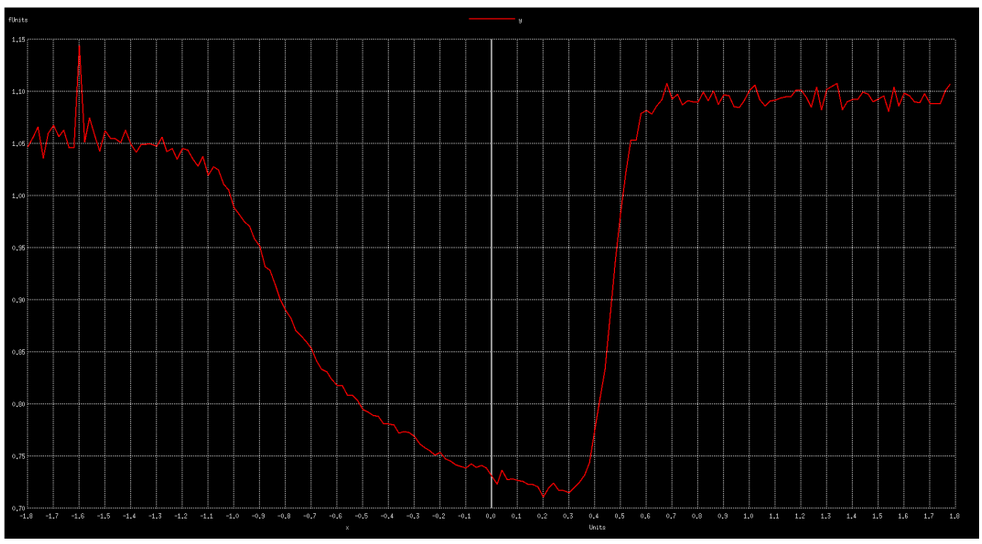


2.2.4 Short N-MOSFET for f=10GHz

SPICE Netlist:

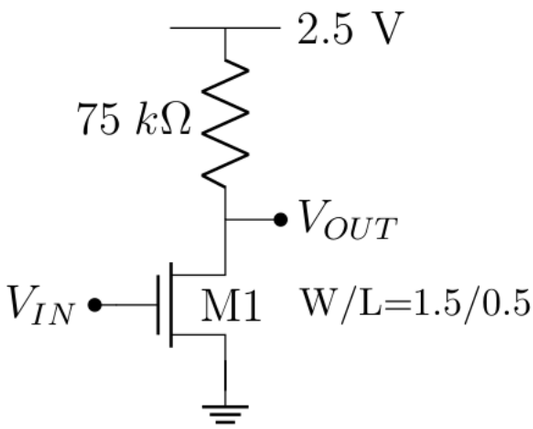
```
Question-2b Short Channel N-MOSFET for f = 10G Hz

* Model
.include "TSMC180.lib"
.model nch_tt nmos

* Circuit
Vs      G       1       AC      SIN(0 0.000000000015915 10G)
Vcm     1       0       DC      -1.8
M       0       G       0       0       nch_tt W=450n L=180n

* Results
.control
run

let Vg = -1.8
let X = vector(180)
let Y = vector(180)

while Vg < 1.81
        alter @Vcm Vg
        tran    1p      0.101n
        meas    tran    Capacitance    FIND    Vs#branch      AT = 0.1n
        let X[50*(Vg+1.8)] = Vg
        let Y[50*(Vg+1.8)] = -Capacitance

        let Vg = Vg + 0.02
end
plot    Y vs X

.endc
.end
```

Results:



The difference between HFCV and LFCV characteristics is due to the time required for electrons to settle down. When the Frequency is high, there won't be be anytime for electrons to reach Gate end of MOSFET. When Frequency is Low, Electrons reach the Gate end and Capacitance increases.

3 5.NMOS Inverter - SPICE simulations



Specifications

$$\frac{W}{L} = 1.5/0.5 \tag{18}$$

$$W = 540nm, L = 180nm \tag{19}$$

$$V_G = [0, 1.8] \text{ Volts} \tag{20}$$

$$R = dI_D/dV_{DS} \tag{21}$$

3.1 5a

SPICE Netlist

```
Question-5a

* Model
.include "TSMC180.lib"
.model nch_tt nmos

* Circuit
VG      G       0       1.8
M       D       G       0       0       nch_tt W=540n L=180n
R       D       2       75k
V       2       0       DC      2.5

* Analysis
.dc VG 0 1.8 1m

* Results
.control
run
let ID = -V#branch
let Vout = V(D)
let Vin = V(G)
plot    Vout
plot    deriv(Vout)
.endc

.end
```

Results:

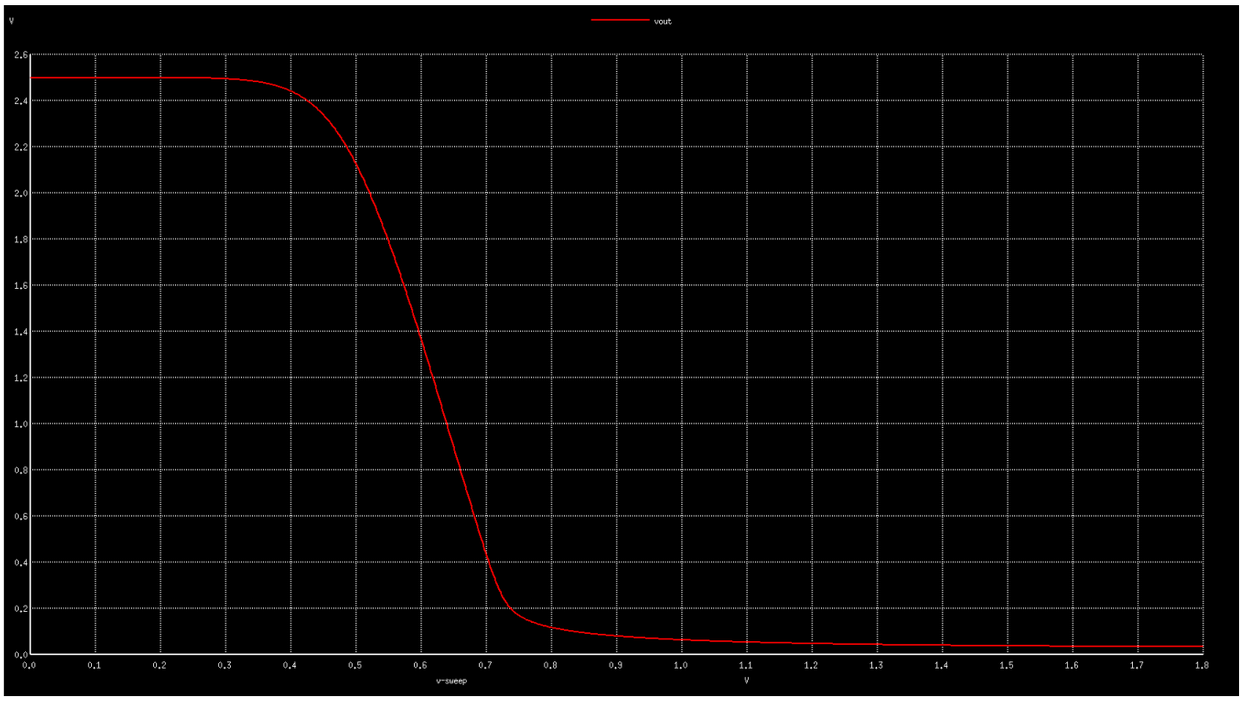


Figure 9: VT Characteristics

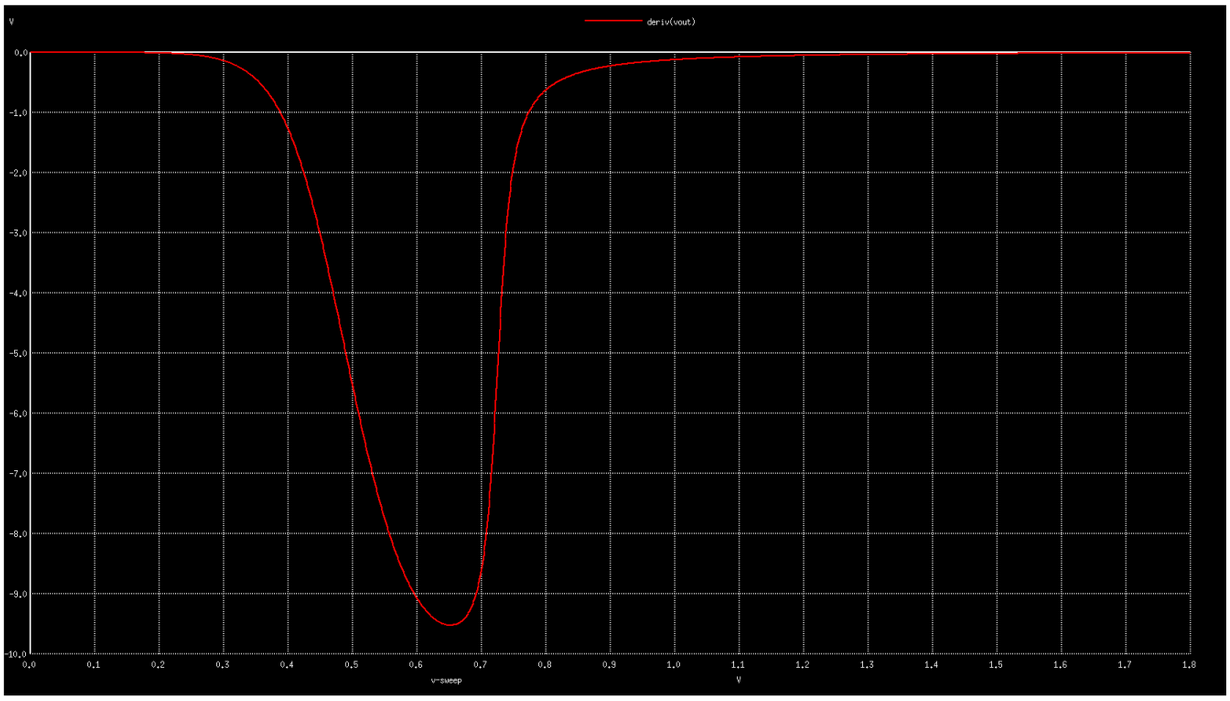


Figure 10: Gain of Inverter

3.2 5b

As Load Resistance increases Magnitude of Gain Increases. On solving Small Signal Model of MOSFET,

$$\frac{dV_{out}}{dV_{in}} = -g_m R_{load} \tag{22}$$

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{Th}) \tag{23}$$

SPICE Netlist:

```
Question-5b
*Load Resistance is varies from 10k to 100k as steps of 10k*

* Model
.include "TSMC180.lib"
.model nch_tt nmos

* Circuit
VG      G       0       1.8
M       D       G       0       0       nch_tt W=540n L=180n
R       D       2       100k
V       2       0       DC      2.5

* Analysis
.dc VG 0 1.8 1m

* Results
.control
run
let ID = -V#branch
let Vout = V(D)
let Vin = V(G)
*plot  Vout
plot   deriv(Vout) vs V(G)
wrdata ../Data/5b/10.dat            V(G)   deriv(Vout)
.endc

.end
```

Python Code for Plotting

```
import numpy as np
import matplotlib.pyplot as plt
import os
def File2Numpy(Path):
        Content = []
        for i in open(Path).readlines():
                Content.append(i.strip().split())
        Content = np.array(Content).astype(float)
        x = Content[:,1]
        y = Content[:,3]
        return np.array([x,y]).T

Path = "../Data/5b/"
DataFiles = len(os.listdir(Path))
# Load Resistance
R = np.arange(10,110,10) * 1000
# Gain
Gain, PeakGain, Vm = [], [], []
# Reading Files
for i in range(DataFiles):
        Gain.append(File2Numpy(Path+str(i+1)+".dat"))
Gain = np.array(Gain)
# Plotting Gain as function VG
plt.figure(figsize=(7,7))
for i in range(Gain.shape[0]):
        PeakGain.append(np.min(Gain[i,:,1]))
```

```
        ind = np.argmin(Gain[i,:,1])
        Vm.append(Gain[i,ind,0])
        plt.plot(Gain[i,:,0],Gain[i,:,1], label=str(int(R[i]/1000))+"K ohm")
plt.legend()
plt.grid()
plt.title(r"Gain vs $V_G$")
plt.xlabel(r"$V_G$")
plt.ylabel("Gain")
plt.savefig("5b_Gain.png")
# Plotting Peak Gain
plt.figure(figsize=(7,7))
plt.plot(R,PeakGain)
plt.grid()
plt.title(r"PeakGain vs R")
plt.xlabel("R")
plt.ylabel("PeakGain")
plt.savefig("5b_PeakGain.png")
# Plotting Vm
plt.figure(figsize=(7,7))
plt.plot(R,Vm)
plt.grid()
plt.title(r"Vm vs R")
plt.xlabel("R")
plt.ylabel("Vm")
plt.savefig("5b_Vm.png")
plt.show()
```

Results:

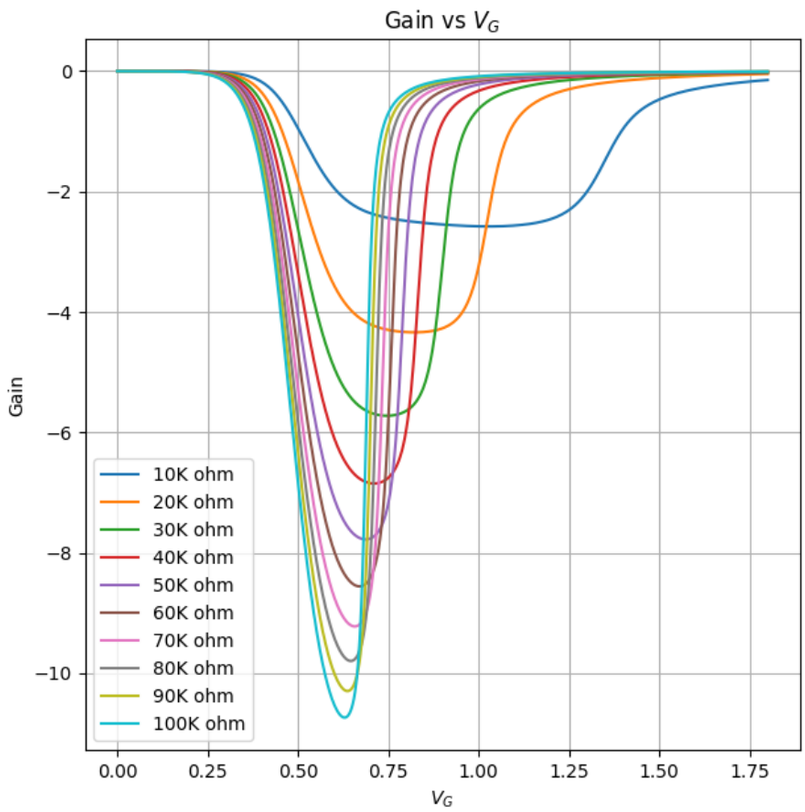


Figure 11: Gain vs V_G

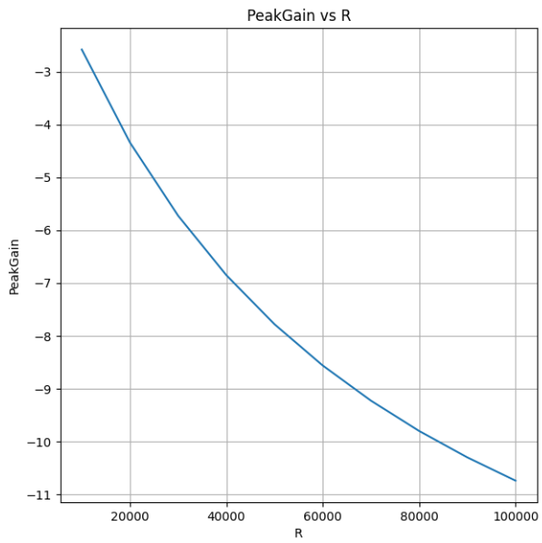


Figure 12: Peak Gain vs R_{load}

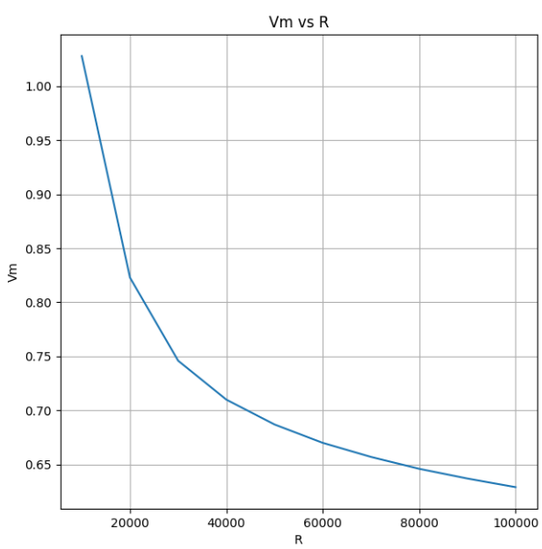


Figure 13: V_m vs R_{load}

3.3 5c

$$C = 3pF \tag{24}$$

SPICE Netlist

```
Question-5c

* Model
.include "TSMC180.lib"
.model nch_tt nmos

* Circuit
VG      G       0       PULSE(0 1 0 0 0 2u 4u)
M       D       G       0       0       nch_tt W=540n L=180n
R       D       2       75k
```

```
V       2       0       DC      2.5
C       D       0       3p

* Analysis
.tran   0.1n    10u

* Results
.control
run
let ID = -V#branch
let Vout = V(D)
let Vin = V(G)
plot    Vin
plot    Vout
.endc

.end
```

Results:

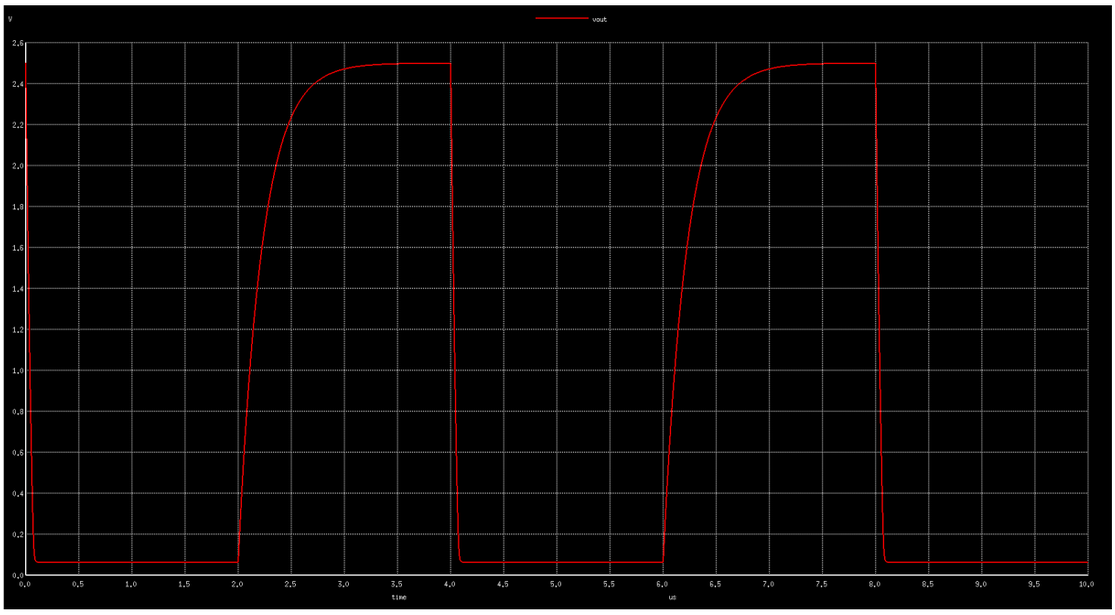


Figure 14: Output of the Circuit for an Ideal Clock Signal with $f = 250k$Hz and duty-cycle of 50%

$$t_r = 0.489\ \mu\text{s} \tag{25}$$

$$t_p = 32.0896\ \text{ns} \tag{26}$$

$$t_f = 63.134\ \text{ns} \tag{27}$$

Rise Time and Fall Time are difference is due to the Resistance of MOSFET. During Rise Time of V_{out}, $V_{in} = low$, which means MOSFET is turned off. So, Capacitor gets charged by drawing Power through Resistor(R_L) from V_{DD}. When discharging i.e during Fall of Output, Capacitors gets discharged through MOSFET and due to Low Resistance of MOSFET when compared to R_L, Fall-Time is less than Rise-Time of Output.