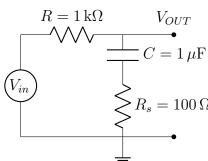
Deadline: Fri, 27th Oct 2020

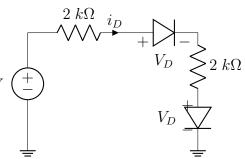
1. SPICE Analyses

- (a) Calculate the operating point of the circuit in Figure 1 using '.op' command given $V_{IN} = 2.5 V$.
- (b) Perform a transient simulation to calculate the phase lag introduced by the circuit if $V_{IN} = \sin \omega t$ with $\omega = 100~Hz$ and 1 MHz. Estimate the phase lag using analytical expression and compare.
- (c) Plot the amplitude and phase transfer characteristics of the filter using $V_{IN} = \sin \omega t$. Determine the 3 dB point and the corresponding phase lag. Compare with analytic expressions.



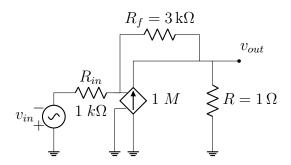
2. Analytic calculations vs SPICE simulations

- (a) Consider the adjacent circuit. Using a simple model, with $V_{Don} = 0.7 \text{ V}$, solve for I_D .
- (b) Find I_D and V_D using the ideal diode equation. Use $I_s=10^{-14}~A$ and T=2.5~V 300 K.
- (c) Run a SPICE simulation to validate your results in (a) and (b).



3. Controlled sources

A voltage controlled current source is driven by ac source, $v_{in} = 1 \ V_{p-p}$, $1 \ kHz$. Simulate the output response and calculate the gain in the circuit.



4. MOSFET Characteristics

Consider long and short channel MOSFETs with $L=10~\mu m$ and $L=0.18~\mu m$ respectively. Both devices have identical W/L of 1.5

(a) Simulate the IV characteristics of PMOS and NMOS devices using 180 nm Predictive Technology Model (PTM). Your results will be similar to Fig. 3.19 and

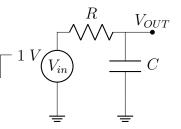
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- 3.21 of reference [1]. Remember the maximum supply voltage for regular devices is only 1.8 V in this technology.
- (b) Identify the transition between linear and saturation regions of operation of these MOSFETs. Annotate the regions of operation on the graphs obtained in part (a). Indicate the differences between short and long channel MOSFETs in your graphs.
- (c) Calculate the small signal output resistance of NMOS and PMOS devices.
- (d) Simulate the $I_d V_g$ characteristics of the NMOS and PMOS devices with $|V_{ds}| = 1.8 \ V$. Plot on a log-lin scale and calculate the sub-threshold slope of NMOS and PMOS devices. The subthreshold slope of MOSFET is given by S = n(kT/q)ln(10) where n is a geometry and technology dependent parameter. Calculate n from your simulations of 180 nm technology.

5. Propagation Delay

A first order RC circuit is frequently used to estimate the propagation delay in logic gates. In the class we have seen that the propagation delay for an ideal step input($t_{r,in} = 0$) is $t_p = 0.69RC$. Further, the output rise time $t_r = 2.2RC$.

- (a) Verify the expressions given above using SPICE simulations. Choose appropriate values for R and C components.
- (b) Now consider a non-ideal step input with 10 $ps < t_{r,in} < 10 ns$. Simulate the propagation delay, and plot t_p as a 0 V function of $t_{r,in}$.
- (c) Arrive at an analytical (or empirical!) expression for propagation delay in presence of *non-ideal* step input.



Submission

Please prepare a pdf of all your solutions, graphs and SPICE netlist (whereever necessary) and submit on Google Classroom.

Simulation setup in NGSPICE

We will use predictive technology models (PTM) for simulations of MOS devices. The instructions to setup the library are as follows:

- Download and install NGSPICE. Use this Installation and Tutorial Guide: https://drive.google.com/file/d/1H6shLV3BGI5wkpwhNbN-r0XI536x1_lC/view?usp=sharing.
- Download Technology File: Download the TSMC 180nm predictive technology file TSMC180.lib from this link: https://drive.google.com/file/d/1cTsloYSmTUf__21MMn0_j0gCI4T0TS80/view?usp=sharing.
- To link the technology file to your SPICE netlist use command .include "path to file".

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• The .model statements in the technology library file contain model name and type (e.g. .model nch_tt nmos). Make sure you use the correct model names in the SPICE netlist.

References

- [1] Rabaey, Jan M and Chandrakasan, Anantha P and Nikolic, Borivoje. *Digital Integrated Circuits*, Prentice Hall, 2002
- [2] Holger Vogt, Marcel Hendrix Paolo Nenzi, Ngspice User's Manual: Version 32, 2020

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