A Novel Fully Synthesizable All-Digital RF Transmitter for IoT Applications

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***Abstract*—In this paper, a fully synthesizable all-digital transmitter (ADTX) is first proposed. This transmitter (TX) uses Cartesian architecture and supports wide-band quadratic-amplitude modulation with wide carrier frequency range. Furthermore, the design methodology for ADTX and corresponding bandpass filter is discussed. This TX is synthesized with digital register transfer level-graphic database system flow, and can be easily implemented in any standard CMOS technology. An exemplary TX is synthesized by TSMC 28-nm standard cell library with extremely small area (0.0009 mm^2) and supports carrier frequency as high as 6 GHz with excellent error vector magnitude (<-30 dB). To the best of the authors' knowledge, this is the first work on a fully synthesizable design of RF transistors, allowing easy technology migration and portability.**

***Index Terms*—CMOS, design methodology, RF, synthesis.**

I. Introduction

IN EMERGING applications of Internet of Things (IoT), wireless connectivity capability of sensor nodes is necessary, as sensors need to talk with each other and with the central hub using wireless connectivity (Fig. 1). Those sensors cover a full spectrum of applications, including temperature sensors for smart furniture, traffic video sensor for smart city, human–machine interface for augmented-reality applications, and EEG/ECG sensors for health applications [1], [2]. In order for multiple sensors to work together without interfering with each other, time-domain multiplexing (TDM) or frequency-domain multiplexing (FDM) can be used. For TDM, different nodes transmit data only at the allocated time slot. However, this requires complicated protocol to coordinate multiple nodes, which in turn increases power consumption and cost.

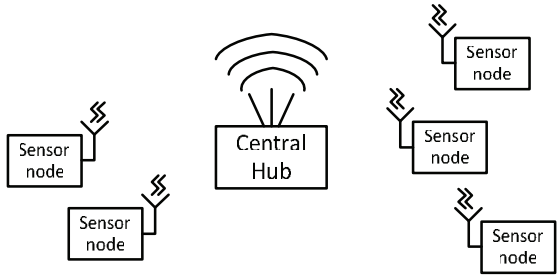

Fig. 1. Structure of IoT with multiple sensor nodes.

In addition, for applications, such as real-time video monitoring, high data bandwidth is required for wireless connectivity. For instance, a resolution of 480 $\times$ 272 with 16-bit color and 25 frames/s (for real-time security camera applications) needs around 50 Mb/s data bandwidth. If TDM is used, each sensor node needs to transfer huge amounts of data within its allocated time slot, and real-time video transfer is hard to achieve when many sensors are present. On the other hand, FDM enables multiple sensors to transfer data simultaneously by allocating different carrier frequencies to transmitters (TXs). This avoids the above issues of TDM. Currently, available frequency bands for FDM include 802.11ah and ISM bands (900 MHz and 2.4 and 5.8 GHz) for all applications and MedRadio (430 MHz) for medical applications, while more frequency bands may be available in the near future.

From a design perspective, it is desirable to have one TX IP for versatile IoT applications. This IP must:

1) be able to cover all frequency bands, which is desirable for IoT application scenarios where many sensors must work simultaneously; therefore the TX can be used universally, and can switch between different bands when necessary;
2) be able to transmit at high data rate within limited bandwidth resources, i.e., have high spectral efficiency, which is desirable for IoT applications, such as smart surveillance camera system;

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3) be easy to integrate into chips fabricated by various process technologies, which is needed for all cost-sensitive IoT applications, such as disposable body sensors.

For conventional analog TXs, since LC-tank is generally used as load to save voltage headroom [3], the transfer function of TX has band-pass characteristic. Therefore, those TXs can hardly cover wide band and meet the requirements (1). This makes conventional RF TXs not flexible enough to work under IoT application scenarios where many sensor nodes must work simultaneously. Digital TXs have also been proposed to use binary signal instead of analog signal within TX chain and avoid LC-tank load [4], [5]. However, these reported digital TXs are based either on phase-MUX or phase-locked-loop (PLL) architecture, and they cannot transmit spectral-efficient quadratic-amplitude modulation (QAM) signal, and therefore hard to meet the requirement of real-time video IoT applications where high data rate is necessary. Finally, design of both conventional analog and digital TXs is based on custom circuit methodology. Therefore, the conventional TX IP is hard IP, in the form of graphic database system (GDS) database. Retuning of circuits is required when one IP is to be used in another fabrication technology.

In this paper, an all-digital, fully synthesizable TX is proposed to meet the requirement of IoT applications. By taking advantage of fast-evolving digital gates, the proposed TX can cover a wide carrier range of dc ∼6 GHz, and therefore all ISM and MedRadio bands are covered. In addition, by using Cartesian architecture, the proposed TX can support M-ary modulation, and therefore high data rate transmission within limited bandwidth is possible with our TX. Finally, we used digital flow (register transfer level (RTL) to GDS) to implement our TX. The TX IP is a soft IP, and can be easily fabricated in various process technologies. In addition, this IP has small area consumption, and can be easily integrated into TX array.

The main contribution of this paper includes the following.

1) A Cartesian all-digital TX (ADTX), which can be synthesized with digital standard cells.
2) Circuit techniques (pseudo-differential output buffer and carrier delay calibration) for ADTX to improve signal quality.
3) Design methodology for ADTX which greatly reduces design cycle time.
4) Tunable bandpass filter (BPF) for out-of-band noise suppression.

The proposed synthesizable ADTX can fully take advantage of feature size scaling of technology, and therefore the performance of ADTX architecture can scale along with technology. In addition, the proposed TX can be easily programmed to work with various modulation schemes and carrier frequencies, and therefore our proposed TX is one step closer to ideal software defined radio. To the best of the authors' knowledge, this is the first work on a fully synthesizable design of RF transistors, allowing easy technology migration and portability.

This paper is organized as follows. The TX architecture and blocks are introduced in Section II. In Section III, the building blocks of the proposed TX are described, followed by design methodology discussion in Section IV. In order to eliminate out-of-band interference, a ring filter along with its synthesis algorithm is proposed in Section V, and the TX-BPF array for wide-band transmission is discussed in Section VI. We present measurement results of prototype TX with filter in Section VII, and the conclusion is drawn in Section VIII.

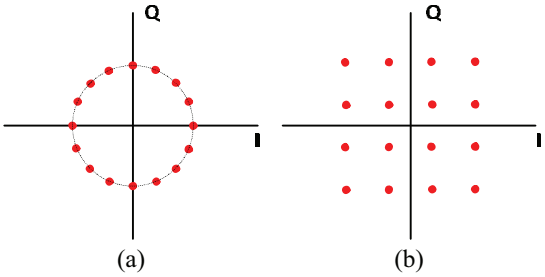


Fig. 2. Constellation of (a) n-PSK and (b) n-QAM, where n=16.

II. Modulation Scheme and ADTX Architecture

In IoT applications, the available spectrum is shared band between a large amount of wireless sensors. In order to accomplish high-speed data transfer within limited frequency bandwidth, spectrum efficiency of modulation scheme is extremely important as it limits the data rate that the transceiver can achieve. In addition, modulation scheme also decides the signal-to-noise ratio (SNR) specification of a transceiver for acceptable bit error rate (BER).

The most common digital modulation schemes for wireless transceiver include n-phase-shift keying (PSK) and n-QAM modulation, where n denotes the number of digital states (constellation points) of modulation. As shown in Fig. 2, n-PSK modulates only the phase of carrier while n-QAM modulation modulates both phase and amplitude of carrier. N-PSK and n-QAM have the same spectrum efficiency when they have the same number of constellation points. Also, with higher n, the spectrum efficiency of three modulation schemes is improved. However, the SNR requirements for three modulation schemes are quite different (Fig. 3). With given BER, n-QAM has lower SNR requirement. This is due to the fact that constellation points of n-QAM have the longest Euclid distance between each other [6].

Modulation of carrier can be accomplished by various architectures of TXs. PLL-based ADTX achieves carrier modulation by injecting data into PLL and modulating carrier phase [5]. Unfortunately, the PLL-based ADTX can only achieve n-PSK. Therefore, SNR requirement for both TX and receiver (RX) is stringent. In addition, the data bandwidth of PLL-based ADTX is limited by the loop bandwidth of PLL, which is generally smaller than 1 MHz.

Simultaneous modulation of amplitude and phase can be achieved by polar or outphasing architecture ADTX [7], [8]. However, the bandwidth of data signal is still limited by PLL loop bandwidth. In addition, the phase-amplitude mismatch is hard to control, which can degrade error vector magnitude (EVM) seriously.

Cartesian architecture ADTX [9]–[13] is the most common architecture to support n-QAM. In [9]–[12], ADTX is based

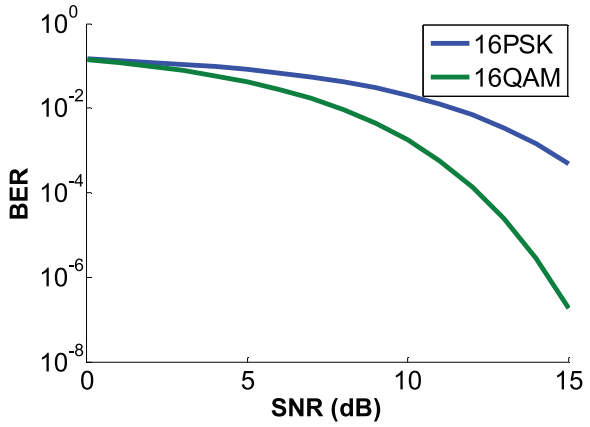


Fig. 3. BER-SNR plot of 16PSK and 16QAM.

on RF-digital-to-analog converter (DAC). The RF-DAC runs at high frequency ($> 4\times$ carrier frequency) and needs good resolution and effective number of bits. Therefore, RF-DAC requires careful manual design and layout. Another method to implement Cartesian architecture is by sigma-delta modulation (SDM) [13]. This method transforms multibit input signal into 1-bit stream by SDM, and then transmits 1-bit stream by digital power amplifier (PA). In [13], with carrier frequency of f_c, a clock signal running at $4f_c$ is required since MUX-based upconversion is used. This $4f_c$ clock restricts the highest carrier frequency that ADTX can achieve.

III. Fully Synthesizable All-Digital Transmitter

The architecture of the proposed TX is shown in Fig. 4. By using Cartesian architecture, the proposed TX can have much higher baseband data bandwidth than PLL-based TXs, and it can support QAM modulations. The multiple-bit input of each I/Q path is first oversampled by digital SDM and converted into a train of one-bit pulses. This train of 1-bit pulses conveys amplitude information of I/Q path. Then, the pulse train is fed into digital upconverter, which is virtually an XOR gate. Finally, the buffer chain works as driver amplifier and drives the 50-Ω load (which is the input impedance of off-chip PA or antenna). I/Q combination is also accomplished in the final stage: I/Q signal is added in current domain. The proposed ADTX has low-pass transfer function instead of band-pass transfer function as in conventional TX. Once the upper limit carrier frequency of the ADTX is identified (defined by speed of digital gates in given process technology), it can cover all carrier frequencies below that limit.

A. Digital Sigma-Delta Modulator

Digital SDM converts the multibit digital baseband input of I and Q path into a train of oversampled 1-bit pulses. The quantization noise of SDM is pushed out of band by oversampling and noise shaping [14]. SDM order and oversampling ratio (OSR) are determined by in-band signal SNR and out-of-band emission requirements. A higher order reduces in-band quantization noise (Fig. 5) while increasing out-of-band emission that can be attenuated by a filter in a following stage.

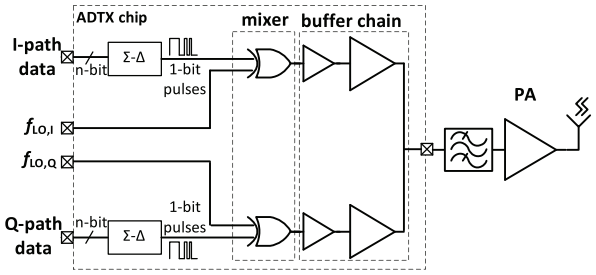


Fig. 4. Architecture of proposed ADTX.

OSR is a tradeoff between in-band SNR and power consumption. Order is a tradeoff between SNR and design complexity. With higher order, SDM has higher risk of instability. For a 1-bit pth order digital SDM, the signal to quantization noise ratio is [15]

$$\mathrm{SNR} = 10\log_{10}\left[\frac{(2p+1)(\mathrm{OSR})^{2p+1}P_S}{\pi^{2p}e_{\mathrm{rms}}^2}\right] \tag{1}$$

where P_S is the average power of I or Q signal of n-QAM signals

$$P_S = \frac{2}{\sqrt{n}}\sum_{i=1}^{\sqrt{n}/2}\left(\sqrt{n}-2i+1\right)^2 \tag{2}$$

and e_{rms}^2 is the mean square of quantization noise.

Compared with DAC in conventional implementation, SDM has similar in-band SNR but much compact silicon area [3]. Regarding out-of-band noise, conventional DAC needs a nonchip low-pass filter (LPF) to filter out out-of-band image, while SDM in our ADTX needs an RF filter to eliminate out-of-band quantization noise. We propose one tunable filter that can work over multiple frequency bands in Section V. The proposed filter is based on transmission line with only a few passive components. Modern package technology can implement this kind of filter within package using in-package routing, and thus it can be integrated together with RF frontend module (such as PA) in the same package with low cost overhead [15]. In addition, with evolution of CMOS technology, we expect faster devices and therefore SDM can work at higher sampling frequency, and this not only pushes out-of-band noise to higher frequency (and therefore eases filter specifications) but also enhances in-band SNR so that more complicated modulation scheme can be supported. On the other hand, in-band SNR of DAC is limited by mismatch between devices. In advance technology, mismatch of devices is becoming worse [16], so SDM has more potential than traditional DAC with technology evolving.

B. Upconversion

The upconversion is accomplished by XOR operation of SDM pulse train and local oscillator. The output of XOR upconversion can be expressed as

$$X_{\mathrm{RF}} = \mathrm{PT}\oplus\mathrm{LO} = \begin{cases}\overline{\mathrm{LO}}, & \text{when PT} = 1\\ \mathrm{LO}, & \text{when PT} = 0\end{cases} \tag{3}$$

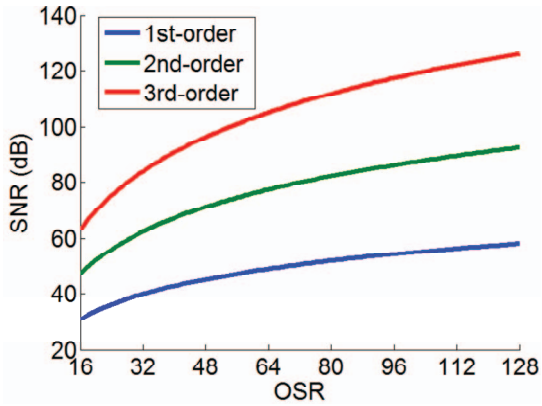


Fig. 5. Simulated SDM SNR versus OSR.

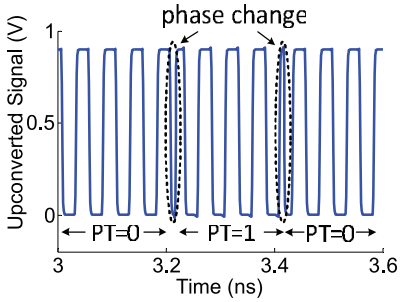


Fig. 6. Simulated upconverted waveform.

where X_{RF} is output of upconversion, PT is input pulse train, and LO is local oscillator input. The output of upconversion is either original LO (when PT = 0) or LO with 180° phase change (when PT = 1). By using XOR instead of AND/OR gate, the output of upconversion has constant envelope (Fig. 6). In addition, by using in-phase and quadrature carrier, the 4× oversampling carrier in [13] can be avoided. It should be noted that carrier frequency should be at least 3×–4× higher than SDM sampling frequency to meet time-bandwidth requirement for demodulation [18]. The XOR-based mixer is similar to switch-based passive mixer in conventional RF design in essence, but can be implemented by digital flow (Fig. 7). One issue with XOR-based mixer is that mismatch of XOR gate delay can induce EVM degradation, and this mismatch must be calibrated as discussed in Section III-D.

C. Output Buffer Chain

The output buffer chain uses pseudo-differential structure to enhance power supply rejection. It starts from a buffer with minimum size, and increases the size of each buffer stage until the final stage. The final stage outputs current into the load. The final outputs of I/Q buffer chain are connected together to the load, and thus signals from I/Q are added together in current domain. The circuit of inverter buffer is similar to push–pull power amplifier in conventional RF design, and therefore output buffer chain is similar to conventional RF design in essence but can be implemented by digital design flow.

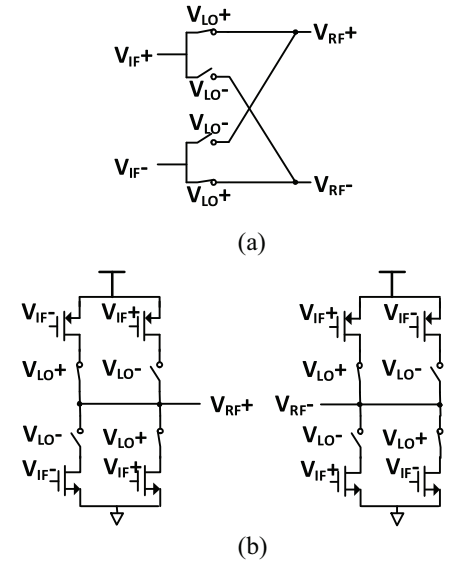


Fig. 7. (a) Conventional passive mixer. (b) Proposed XOR-based mixer.

There are several issues if we use single-ended structure in output buffer chain [Fig. 8(a)]. The output stage of the buffer chain is an inverter, simply composed of a pMOS and an nMOS. The first issue is dc bias problem. We need a proper dc bias point at the other end of load impedance. It would need extra effort to find the optimal bias point for each chip, and extra hardware overhead is required to implement this bias point. The second issue is output signal asymmetry. When input of the inverter is low, the nMOS is turned off and the pMOS is turned on to pump out current I_p onto load impedance. When input of the inverter is high, the pMOS is turned off and the nMOS is turned on to pump in current I_n from load impedance. However, I_p and I_n can be different due to different characteristics of pMOS and nMOS. Therefore, the output current across load impedance is not symmetric [Fig. 8(b)], and the dc component of output waveform is not zero. On the other hand, the antenna [19] has a bandpass characteristic and cannot pass dc signal. When the input signal has dc component, the envelope of antenna output signal needs time to settle. Before envelope settles, the EVM of output signal is not acceptable as the constellation is distorted. This makes single-ended buffer chain unable to meet the fast on–off requirement of IoT applications. Finally, the single-ended structure is also vulnerable to power supply noise.

In order to solve the issues, we use (pseudo) differential structure for output, as shown in Fig. 8(c). In differential structure, the load impedance is connected across positive output and negative output. By using differential structure, dc bias point for output impedance is no longer needed. In addition, output waveform is symmetric [Fig. 8(d)]. When the positive input for buffer is low, the pMOS in inverter INV_P is turned on, and pumps out current I_p upon load impedance. Meanwhile, the negative input for buffer is high, and the nMOS is INV_N is turned on and pumps in current from load impedance. When the positive input is 1 and the negative input is 0, the pMOS in INV_N pumps out current I_n and the

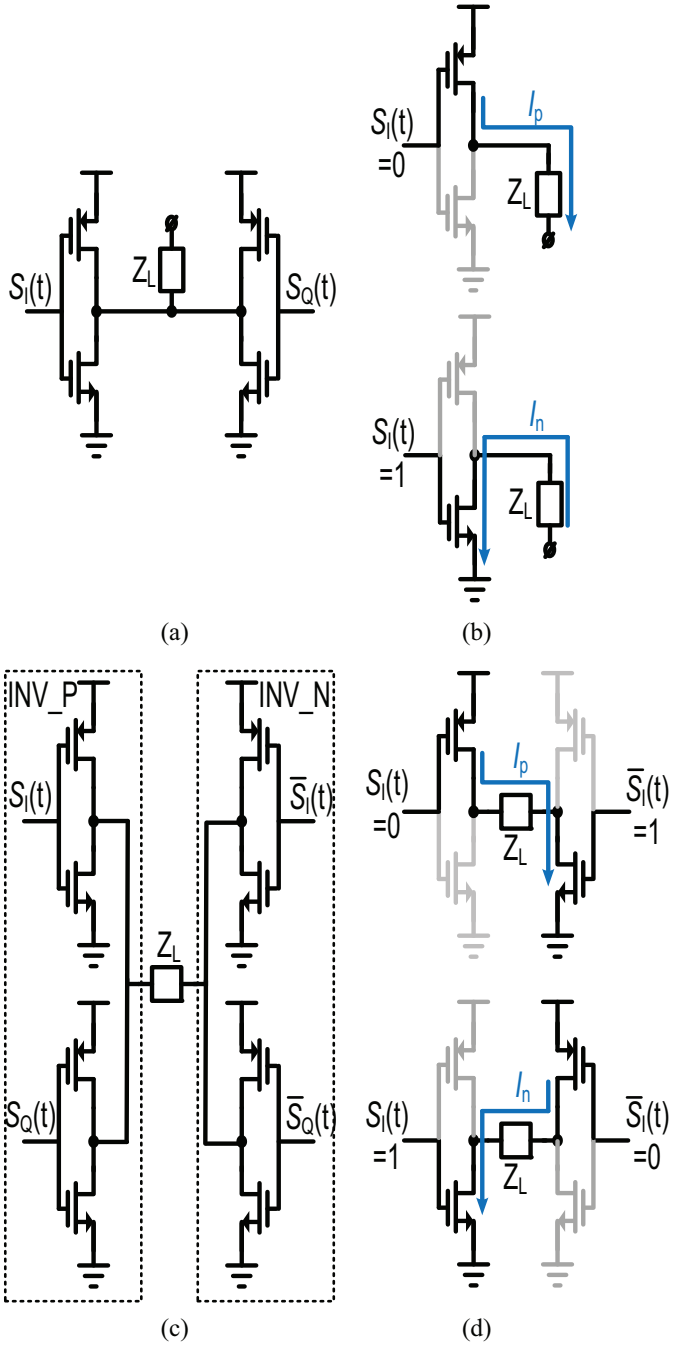


Fig. 8. Pseudo-differential output stage. (a) Single-ended structure (b) Current load of single-ended structure. (c) Differential structure. (d) Current load of differential structure.

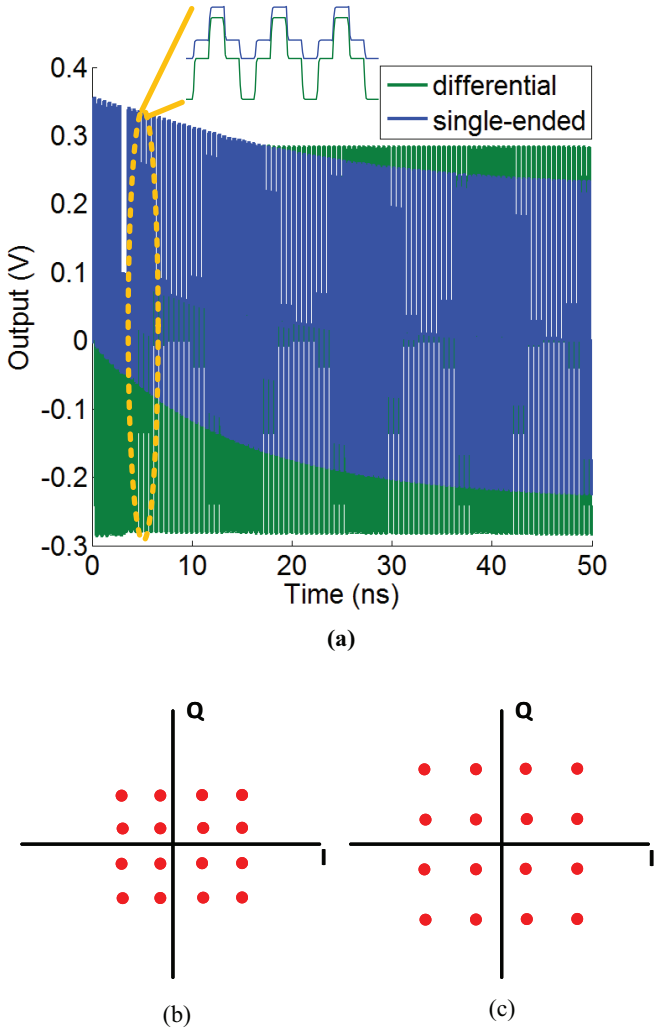


Fig. 9. (a) Waveform of differential and single-ended buffer chain output. Constellation of (b) single-ended output before settling and (c) both single-ended and differential output after settling.

nMOS in INV_P pumps in the current. As long as the pMOS in INV_P matches the pMOS in INV_N and the nMOS in INV_P matched the nMOS in INV_N, I_p and I_n are identical, and symmetric signal waveform with zero dc component is obtained. Therefore, fast settling of both antenna output envelope and constellation is achieved.

The comparison of single-ended and differential output waveforms are shown in Fig. 9(a). It can be seen that waveform envelope of single-ended output takes a lot of time to settle. In addition, the constellations of single-ended output before and after settling are shown in Fig. 9(b). It is clear that before settling, the constellation cannot be demodulated properly, as it is distorted and shifted compared with constellation after settling.

D. Carrier Delay Calibration

In order to have differential output, we need two paths (positive and negative paths) for one signal. However, the carrier delay between positive and negative paths can be different due to mismatch of digital gates. This induces IQ phase error and degrades EVM. Suppose there is positive/negative carrier delay mismatch (translated to phase) of θ_I for I-path and θ_Q for Q-path in TX. Then the output of I-path signal $S_I(t)$ and Q-path signal $S_Q(t)$ can be expressed as

$$\begin{aligned} S_I(t) &= A_I[\cos\omega t - \cos(\omega t + \pi + \theta_I)] \\ &= A_I[(1+\cos\theta_I)\cos\omega t - \sin\theta_I \sin\omega t] \\ S_Q(t) &= A_Q\big[\sin\omega t - \sin\big(\omega t + \pi + \theta_Q\big)\big] \\ &= A_Q\big[\big(1+\cos\theta_Q\big)\sin\omega t + \sin\theta_Q\cos\omega t\big] \end{aligned} \quad (4)$$

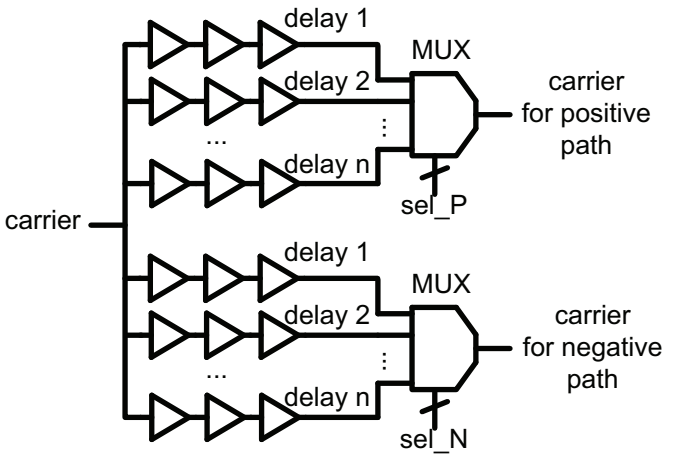


Fig. 10. Delay calibration by delay selection.

where A_I and A_Q are the signal amplitude of I- and Q-path, respectively. In RX end, the signal after downconversion is

$$\begin{aligned} R_{I,\mathrm{mix}}(t) &= G_{I,R}\cos\omega t\cdot\{A_{I,R}[(1+\cos\theta_I)\cos\omega t-\sin\theta_I\sin\omega t] \\ &\quad + A_{Q,R}\big[\big(1+\cos\theta_Q\big)\sin\omega t+\sin\theta_Q\cos\omega t\big]\} \\ &= \frac{1}{2}G_{I,R}\{A_{I,R}[(1+\cos\theta_I)(1+\cos 2\omega t)-\sin\theta_I\sin 2\omega t] \\ &\quad + A_{Q,R}\big[\big(1+\cos\theta_Q\big)\sin 2\omega t+\sin\theta_Q(1+\cos 2\omega t)\big]\} \\ R_{Q,\mathrm{mix}}(t) &= G_{Q,R}\sin\omega t\cdot\{A_{I,R}[(1+\cos\theta_I)\cos\omega t-\sin\theta_I\sin\omega t] \\ &\quad + A_{Q,R}\big[\big(1+\cos\theta_Q\big)\sin\omega t+\sin\theta_Q\cos\omega t\big]\} \\ &= \frac{1}{2}G_{Q,R}\{A_{I,R}[(1+\cos\theta_I)\sin 2\omega t-\sin\theta_I(1-\cos 2\omega t)] \\ &\quad + A_{Q,R}\big[\big(1+\cos\theta_Q\big)(1-\cos 2\omega t)+\sin\theta_Q\sin 2\omega t\big]\} \end{aligned} \tag{5}$$

where $G_{I,R}$ is the RX gain of I-path, $G_{Q,R}$ is the gain of Q-path, $A_{I,R}$ is the RX signal amplitude of I-path, and $A_{Q,R}$ is the RX signal amplitude of Q-path. After removal of 2ω components by LPF, the demodulated signal in RX is

$$\begin{aligned} R_{I,\mathrm{demod}}(t) &= \frac{1}{2}G_{I,R}\big[A_{I,R}(1+\cos\theta_I)+A_{Q,R}\sin\theta_Q\big] \\ R_{Q,\mathrm{demod}}(t) &= \frac{1}{2}G_{Q,R}\big[A_{Q,R}\big(1+\cos\theta_Q\big)-A_{I,R}\sin\theta_I\big]. \end{aligned} \tag{6}$$

Clearly, there is Q-path signal energy in I-path, and I-path signal energy in Q-path. This IQ cross-talk can degrade EVM significantly, as it both rotates and distorts constellation. Unless θ_I and θ_Q are equal, the IQ cross-talk issue cannot be solved by conventional constellation rotation algorithm in baseband. Therefore, we need to calibrate delay mismatch for positive/negative paths.

In order to reduce delay mismatch between positive path and negative path, carrier delayed by different delay cells are connected to multiplexer (Fig. 10). The delay mismatch of clock buffers in positive and negative paths is compensated by delay cells. The best compensated carrier is then selected by multiplexer. In proposed design with 28-nm technology, delay resolution is less than 2 ps and compensation range can be as large as 10 ps, which can cover device mismatch according to simulation.

IV. Design Methodology

Conventional analog TX design, which is based on full-custom circuit design, does not fully exploit benefit from technology scaling. For one thing, MOSFETs in conventional TX works in analog mode (saturation region). While digital circuit works in on/off state and its performance enhances directly with feature size shrink, the benefit of feature size shrink on analog circuit performance is greatly offset by short-channel effects and low power supply voltage [20].

In conventional analog TX design, linearity is directly related to power supply voltage. In order for MOSFETs to work linearly, MOSFETs must work in saturation region with large gate-source voltage and drain-source voltage [20]. With low power supply, the available gate-source and drain-source voltage headroom for MOSFETs decreases and linearity degrades. Also many analog techniques, such as cascode, need large voltage headroom to work. In advanced technology node, it becomes difficult to implement those analog techniques. In order to work under low supply voltage, inductor is commonly used as load. However, the large size of inductor is decided by wavelength of carrier, and does not scale with feature size shrink. Though inductor implemented by through-silicon via has been proposed with compact area [21]–[23], it is still very expensive in terms of cost. Also, the less-compact custom layout of circuits increases silicon area.

In terms of design effort, manual layout of custom circuit usually is time-consuming. In many reported ADTX frontends [7]–[12], custom design flow is still used for key blocks. In PLL-modulation-based ADTX [7], [8], manual design and layout of PLL is necessary for good EVM performance [24]. In RF DAC-based ADTX [9]–[12], it is also necessary to design and layout RF DAC by hand to avoid excess parasitic and guarantee acceptable mismatch. Unfortunately, in advanced technology node, manual layout becomes more painstaking. For one thing, the interconnect parasitic and layout-dependent effects (such as well-proximity effect and length of diffusion effect) become more significant in advanced technology node. Those effects are hard to model before actual layout. Therefore, it can take 3–4 iterations between schematic and layout design to finalize circuit. Furthermore, the design rule check (DRC) for layout in advanced node becomes very complicated to guarantee high yield. Consequently, it may take a lot of effort to clean up DRC errors. One iteration of schematic design cycle may need several days or even one week to finish, and the whole design cycle can take several weeks. Very often, design space is not fully explored due to tight schedule.

The proposed ADTX design based on standard cell and digital synthesis flow can solve the above issues. First, digital circuits are more scalable and can fully exploit technology scaling. Unlike analog circuits which work in saturation region and encounters voltage headroom issue in advanced technology node, digital circuits work in on-off region and simply runs faster as technology scales. As discussed in the previous section, in the advanced technology node, digital gates in SDM and up-mixer run faster. Therefore, the carrier frequency range and EVM improves with technology scaling. With higher standard cell density, more complicated digital design is possible

under the same area budget. In addition, digital design flow can solve the long design cycle issue. SPICE model with layout effects of standard cells is available from the vendor of standard cell library. Therefore, layout effects can be taken into account in the early stage of design and fewer iterations are needed to finalize circuit. Also, the design rule is automatically observed when physical synthesis tool is used to generate layout. Therefore, the time needed for layout of all-digital design is reduced by several orders of magnitude when compared with manual layout. This allows fast iteration and more trial-and-error for optimal design.

In the proposed ADTX design, we describe design with RTL code, then use logic synthesis tool (design compiler by Synopsys) to generate gate-level netlist and physical synthesis tool (system-on-chip encounter by cadence) to generate layout. System-level and silicon-level co-optimization under constraint [25] is adopted. The detailed design flow is shown in Fig. 11.

First, in RTL-level design, we need to decide the output buffer size and parameters of SDM. The size of output buffer is decided by required output power, which is in turn decided by link budget of wireless system. For a given standard cell library, the required size of output buffer for a given output power at a specific carrier frequency is decided. Therefore, the selection of output buffer size can be achieved through look-up table (LUT). The parameters of SDM include order of SDM and OSR. With higher order of SDM, we have stronger noise shaping and in-band EVM is improved. However, high-order SDM has stability issues and needs careful and complicated design. On the other hand, higher OSR also improves in-band EVM. In addition, it pushes out-of-band noise to frequency bands that are far away from carrier frequency. Consequently, the out-of-band noise can be better attenuated by BPF when OSR is large to meet spectral mask of communication standard. However, OSR is limited by the speed of digital gates in SDM, and also limited by the carrier frequency as discussed in Section III. Therefore, with given process technology, EVM requirement, spectral mask and carrier frequency, parameters of SDM can also be saved in LUT for fast ADTX design.

After RTL code is verified, we use logic synthesis tool to generate gate-level netlist. Proper timing constraint is necessary to guarantee correct function of sequential logic (e.g., SDM). In addition, the timing constraint for path delay is useful for delay balance of I/Q paths. Based on gate-level netlist, auto place-and-route (PnR) tool generates physical layout of ADTX. In order to reduce mismatch, we divide design into two partitions (shown in Fig. 12). The first partition is from input to SDM output. This part is sequential logic, and timing mismatch between I/Q paths can be well-controlled by proper timing constraint. The layout of this part is generated by PnR tool directly. The second partition includes mixer (XOR gate) and buffer chain. In order to avoid random placement of those combinational logic cells, we use PnR tool to generate the layout instance including the mixer and output buffer of one path. Then we use this instance for all four paths. Consequently, the systematic mismatch among four paths is minimized due to identical layout of mixer and output buffer. In addition, the power supply of partitions 1 and 2 are separated. Since there is only combinational logic in partition 2, and we can safely adjust power supply voltage of partition 2 to adjust output power and power consumption without setup/hold time concern. The carrier path is generated by clock tree insertion to guarantee small systematic mismatch.

Finally, after layout is generated, we run post-layout simulation to evaluate the performance of the ADTX, and fine tune ADTX design (e.g., output buffer size). Monte-Carlo simulation is also performed to find out systematic and random path delay mismatch of carriers. Carrier delay calibration block is synthesized and inserted into design to cover worst case in Monte-Carlo simulation.

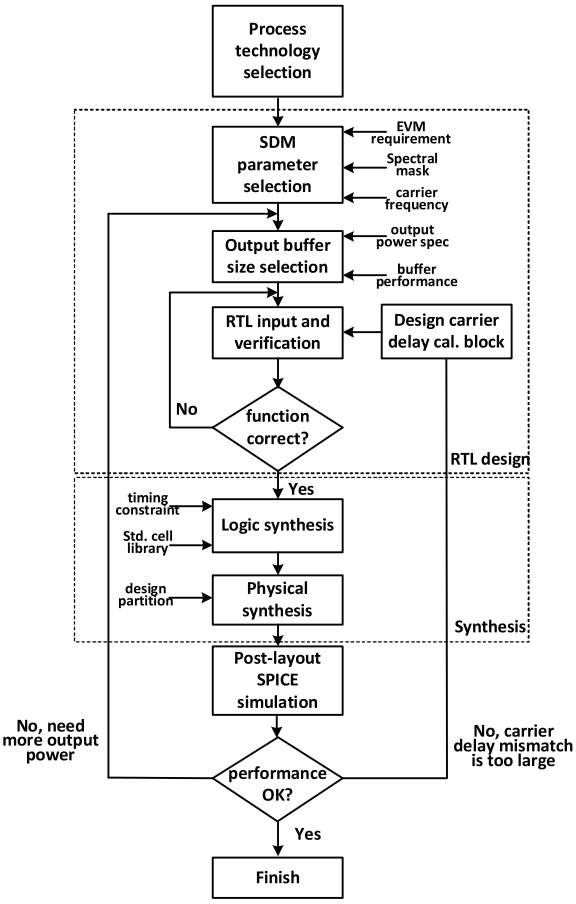


Fig. 11. Flow chart of proposed design methodology.

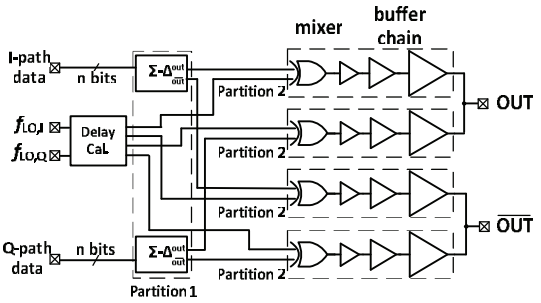


Fig. 12. Design partitioning.

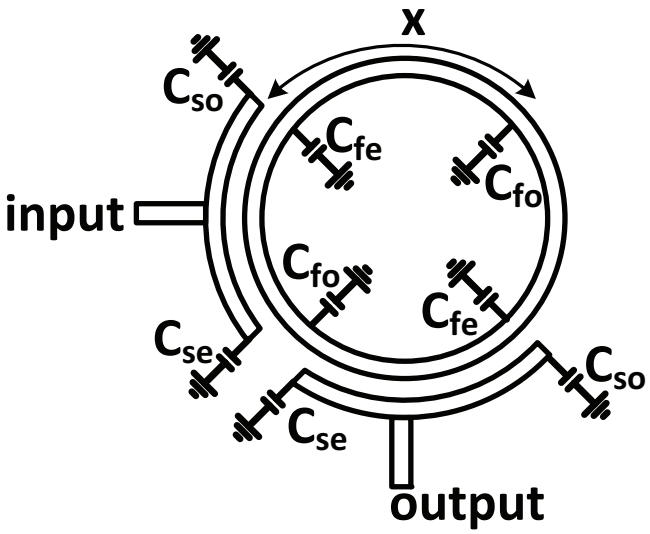


Fig. 13. Dual-mode ring BPF.

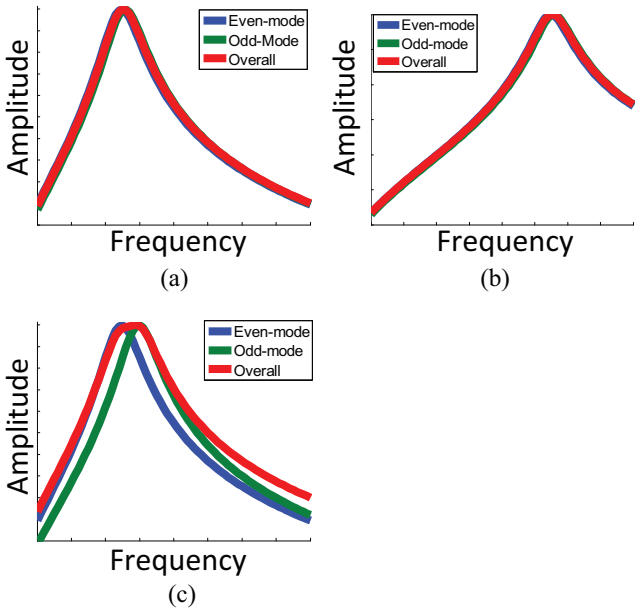


Fig. 14. (a) Frequency response of dual ring BPF. Tuning (b) center frequency by changing resonant frequencies of both even- and odd-mode and (c) pass-band bandwidth by offset resonant frequencies of even- and odd-mode.

V. Wide-Tuning-Range Bandpass Filter

The BPF is essential for eliminating out-of-band interference [26]. For flexible IoT applications, the BPF must have both good selectivity and wide tuning range. Dual-mode ring-resonator filter is an excellent choice to meet selectivity and tuning range requirements [27]. The overall frequency response of dual mode filter is the superposition of even- and odd-mode response. In a dual-mode resonator-based filter, the two modes of the resonator are orthogonal and hence, independently controllable. As such, the odd-mode and even-mode frequencies can be controlled by the capacitances C_{fo} and C_{fe}, respectively (Fig. 13). The two capacitance values can be implemented by varactor diodes, so that C_{fe} and C_{fo}, and consequently the resonant frequencies of even- and odd-mode, can be tuned by changing the bias voltages on varactor diodes. The center frequency of the filter is given as the average of the odd- and even-mode frequencies. Similarly, the relative spacing between the odd- and even-mode frequencies dictates the bandwidth of the BPF. From the above statements, it can be observed that by tuning the resonant frequencies of even- and odd-mode, the overall center frequency and pass-band bandwidth of dual-mode filter can be adjusted (Fig. 14). The tuning range of dual-mode filter is limited by tuning range of varactor. In addition, the selectivity (stop-band attenuation) is controlled by varactors C_{se} and C_{so}. Varactors C_{se} and C_{so} decide quality factor of filter, and therefore the selectivity can be configured through them. The filter is directly coupled to antenna and is impedance matched.

The design flow of filter synthesis is as follows.

Step 1: Choose a length L of the circular ring, such that $L > \lambda_g$, where λ_g is the guided-wavelength in the substrate. The ring behaves as a resonator with two orthogonal modes, which can be controlled by adding perturbations on the symmetrical and asymmetrical planes of the ring, respectively.

Step 2: On loading the planes with varactor diodes, the eigenmode equations for the two modes can be given as

$$\pi f_1 C_{fo} Z = \cot(\beta \cdot x) \tag{7}$$

$$\pi f_2 C_{fe} Z = \cot(\beta \cdot x) \tag{8}$$

where Z is the characteristic impedance of the ring, C_{fe} and C_{fo} the capacitances placed on the symmetrical and asymmetrical planes, respectively, and f_1 and f_2, the two resonant frequencies, respectively. It can be seen that by varying the value of C_{fe} and C_{fo}, the two frequencies can be independently tuned. Also, for two transmission zeroes to be present on either side of the passband, the condition is $C_{\text{fe}} > C_{\text{fo}}$. The operating frequency can be given as $(f_1 + f_2)/2$. The bandwidth of the filter is given as $f_1 - f_2$.

Step 3: Because of slight coupling between the orthogonal modes due to the series capacitance between the feeding arc and ring, the resonant frequency of both the modes would experience a slight downward shift, and iteration may be required to meet design spec. But as long as the capacitance values of varactors are not too large (causing a shift of 30% or more from unperturbed frequency), the movement of the two resonant frequencies remains independent.

A prototype dual-mode ring BPF is shown in Fig. 15. The BPF is implemented on a Rogers Duroid 3006 board with relative permittivity of 6.5. The center frequency of the filter can be tuned from 2.09 to 2.78 GHz with variable 3-dB bandwidth ranging from 45 to 85 MHz. The measured frequency response is shown in Fig. 16. The insertion loss is <3 dB within its tuning range. In addition, the stop-band attenuation

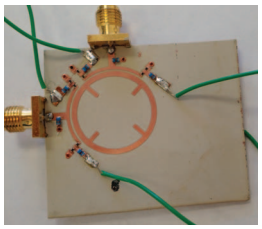


Fig. 15. Manufactured ring BPF.

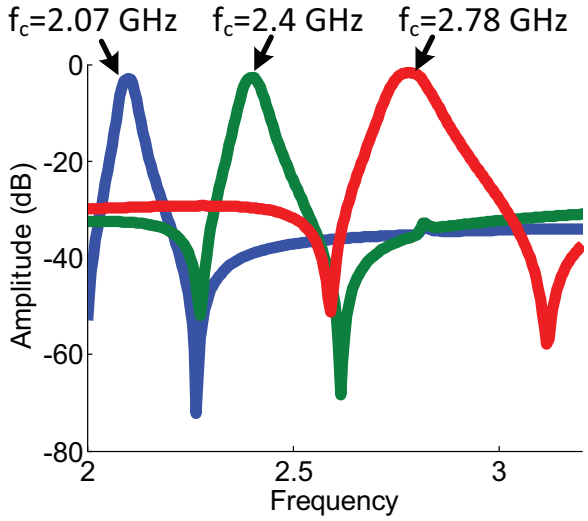


Fig. 16. Frequency response of tunable ring BPF.

is greater than 30 dB. Sharper selectivity can be achieved by cascading multiple stages of BPFs. This design can be easily adapted to MedRadio band, 900-MHz band and 5.8-GHz band by changing the electrical length of ring resonator. The prototype filter is implemented in printed circuit board (PCB) trace, and it can also be implemented by advanced package technology, such as InFO [15] with low cost and form factor.

VI. ADTX-BPF Array

In order to cover the fullband, it is mandatory to use multiple TX-BPF pairs due to limited tuning range of each filter. Multiple TX-BPF pairs form a TX-BPF array (Fig. 17), where each TX-BPF is responsible for one certain frequency range.

For integrated solution, multiple TXs are integrated on one chip to form a TX array, and each TX has its dedicated output port to connect to corresponding BPF [28]. For conventional TX design, TX array is expensive to implement. The conventional TX design generally needs on-chip inductor to save headroom voltage and work under low supply voltage. Since on-chip inductor occupies large area and does not shrink with technology, the whole TX array consumes large silicon area when many TXs are integrated. In addition, when inductor is used in circuit, the circuit has a band-pass transfer function and cannot cover wide band. Consequently, the circuit, and hence TX, cannot cover wideband. This means that in order to cover a wide range of carrier frequency, multiple different TXs must be designed, and only a small portion of TX blocks, which do not have band-pass transfer function, can be reused

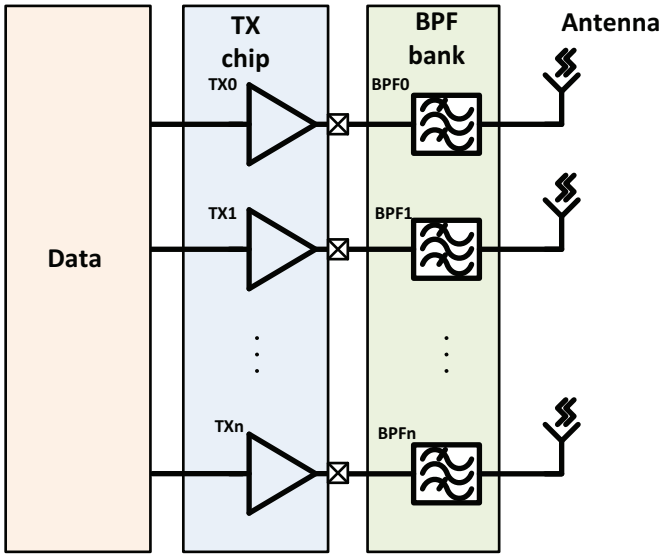


Fig. 17. TX-BPF array.

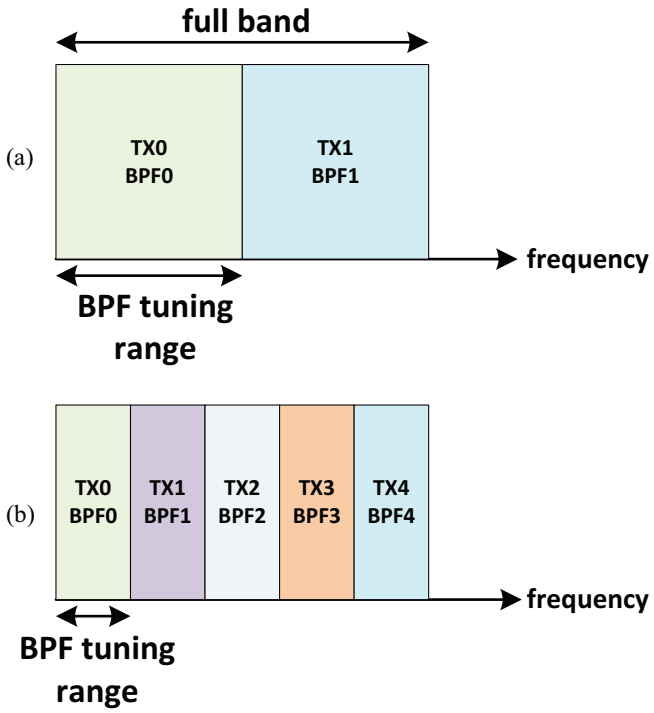


Fig. 18. Tuning range requirement of BPF. When (a) only a few TXs are available and (b) many TXs are available.

between multiple TXs. Finally, when multiple conventional TXs are turned on at the same time, there exists magnetic coupling among inductors from different TXs, which can degrade TX performance. To avoid magnetic coupling, inductors must be placed far away from each other. Therefore, the floor-plan of TX array cannot be very compact, which in turn increases area consumption. In order to verify magnetic coupling effect among TXs, full-wave electro-magnetic simulation needs to be performed, and this simulation can be very time-consuming.

The above issues are solved when the proposed ADTX is used in TX-filter array. First, since the proposed ADTX

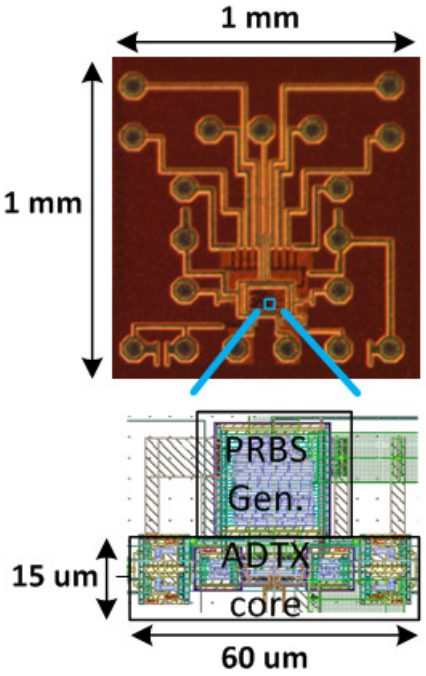


Fig. 19. Chip micrograph and corresponding layout.

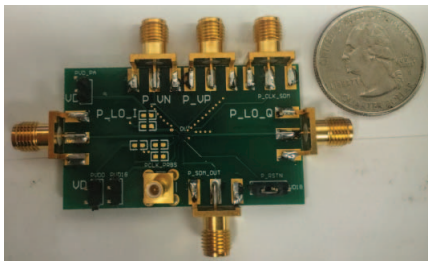


Fig. 20. Test board of ADTX.

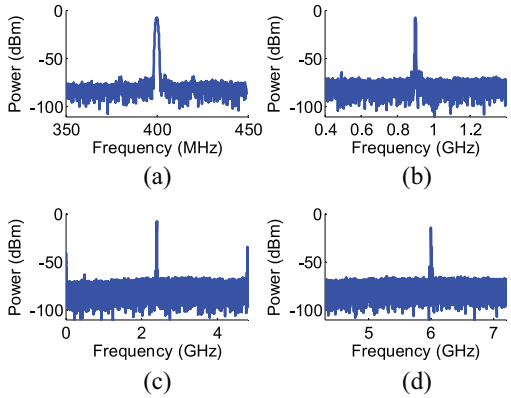
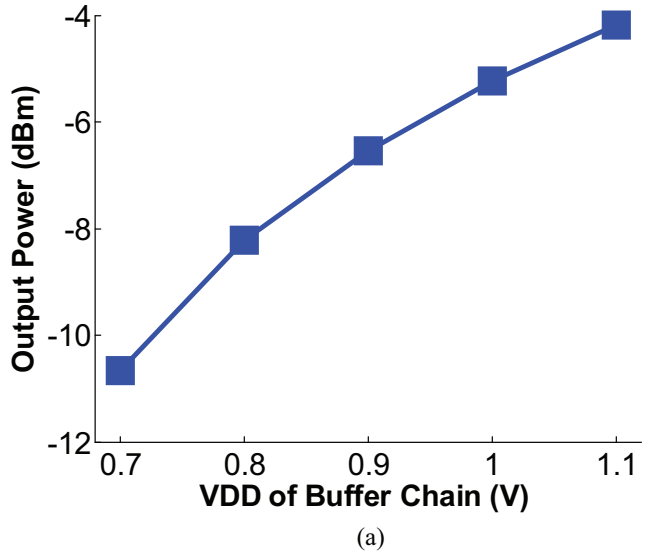


Fig. 21. Measured output at different carrier frequencies. (a) 400 MHz. (b) 900 MHz. (c) 2.4 GHz. (d) 6 GHz.



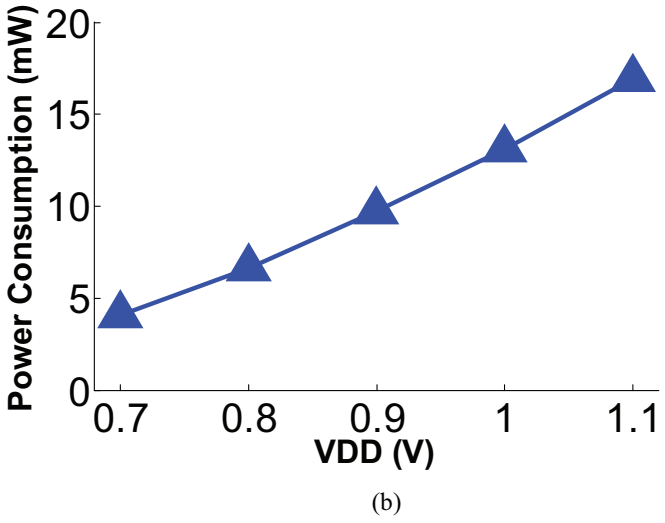


Fig. 22. (a) Output power. (b) Power consumption versus power supply voltage.

has extremely low area consumption, it is feasible to integrate tens of ADTX on the same chip without consuming too much area. This in turn relieves the design specifications of BPFs: since many TXs are available, the tuning range of each BPF does not need to be very large (Fig. 18). In addition, the design can be fully reused since each TX can cover the full band. Therefore, in TX array, each ADTX is identical, which greatly saves design burden. Besides, with the evolving of microelectromechanical systems (MEMS), BPF array is expected to have small size with MEMS implementation, and can be integrated along with ADTX array on the same die or within the same package. MEMS implementation will also allow more BPFs to be integrated and therefore increase the number of TXs in an ADTX array. Finally, since no inductor is used, magnetic coupling is no longer a problem. With proposed ADTX-filter array, a flexible low-cost full-band radio system is available.

VII. Implementation and Measurement Results

The proposed ADTX is implemented with TSMC 28-nm high-performance compact technology. The test chip micrograph and its corresponding layout are shown in Fig. 19. The ADTX only occupies a core area of 60 um $\times$ 15 um, and its gate count is less than 200. Along with ADTX, a pseudo-random bit stream generator is also designed to provide input

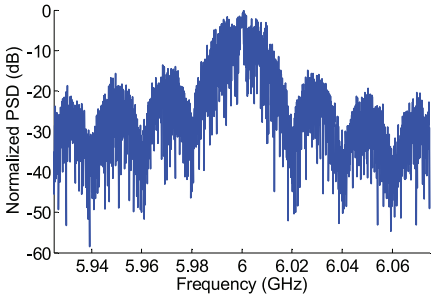


Fig. 23. Output PSD with 6-GHz carrier and 80-Mb/s data rate.

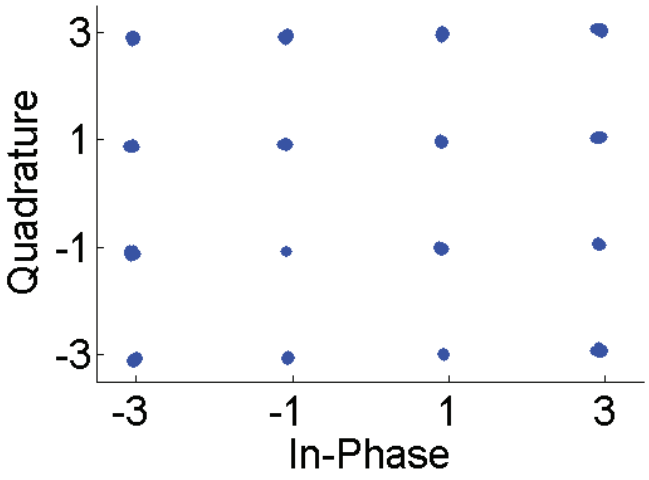


Fig. 24. Constellation of ADTX output w/o carrier delay calibration (EVM = −27 dB).

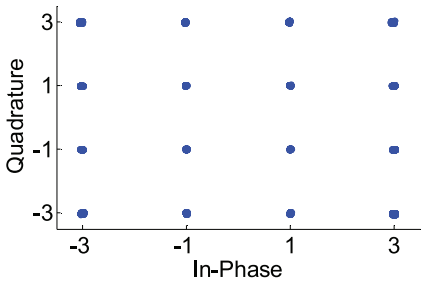


Fig. 25. Constellation of ADTX with carrier delay calibration (EVM < −30 dB).

pattern to ADTX. Flip-chip package is used to reduce the effect of parasitic inductance.

he test board of ADTX is shown in Fig. 20. The proposed ADTX works with nominal voltage of 0.9 V. It can cover a wide band of dc ∼6 GHz. The I/Q carrier for ADTX is provided by HP83640A synthesized sweeper with phase shifter. The output power spectral density (PSD) plots when carrier frequency is 400 and 900 MHz, and 2.4 and 6 GHz are shown in Fig. 21. The measured output power on 50-Ω load of spectrum analyzer is −7.55 dBm at 400 MHz, −8.91 dBm at 900 MHz, −9.46 dBm at 2.4 GHz, and −14.72 dBm at 6 GHz. After de-embedding external loss (PCB trace, co-axial cable, and balun), the real output of ADTX is 3.5 dBm at 400 MHz, 0.8 dBm at 900 MHz, −0.9 dBm at 2.4 GHz,

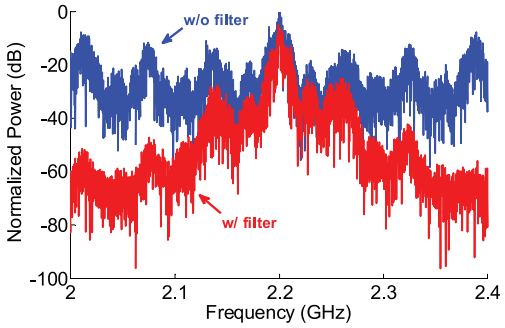


Fig. 26. Output PSD with and without filter.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work	**[31]**	**[3]**
Process	28 nm	90 nm	180 nm
Supply Voltage (V)	0.7-1.1*	1	1
Area (mm^2)	0.0009	1.48**	0.299**
Modulation Scheme	QAM-16	OOK	OQPSK
Architecture	Cartesian all-digital	Direct-Conversion	MUX-based all-digital
Design Methodology	Synthesis	Full custom	Full custom
Operation Freq. (GHz)	0-4	2.4	0.36-0.44
Max. Data Rate (Mbps)	64	0.1	4
EVM (dB)	-30	N/A	-32
Pout (dBm)	-10.2∼-4.9	0	-8
DC Power (mW)	4.5-17	2.53	2.6
Energy effieicncy (nJ/bit)	0.07-0.27	25.3	0.65

*: Power supply of output buffer chain
**: Include PLL

and −6.3 dBm at 6 GHz. Due to the low-pass transfer function of ADTX, the output power drops as carrier frequency increases. By adjusting power supply of buffer chain from 0.7 to 1.1 V, the output power can be adjusted from −10.5 to −4.2 dBm at 6 GHz, while total power consumption varies from 4.5 to 17 mW (Fig. 22). The trends of output power versus supply voltage are similar with other carrier frequencies. The ADTX supports QPSK/QAM16 modulation. To achieve an in-band SNR of 30 dB for QAM-16 signals, an OSR larger than 25 is needed from simulation. With 6-GHz carrier, the SDM samples at 1.5 GHz, and it supports a highest symbol rate of 20 MS/s (OSR=37 which is enough to guarantee good SNR), which translates to the highest data rate of 80 Mb/s with QAM-16. The measured close-in PSD with 80-Mb/s data rate is shown in Fig. 23. The output EVM without carrier delay calibration is −27 dB, as shown in Fig. 24. The EVM after carrier delay calibration is shown in Fig. 25. The EVM is below −30 dB, which is sufficient for demodulation of QAM16 with low BER. The carrier delay calibration improves output EVM by 3 dB. We also measured output PSD of ADTX with/without ring BPF. When no BPF is present, there is out-of-band spectrum leakage, since no pulse-shaping is used in this ADTX. With BPF, the out-of-band leakage can be suppressed by 35 dB (Fig. 26), which makes the spurious emission lower than the FCC regulation of −42 dBm [29], [30]. The nonmonotonic sidelobe amplitude is observed, which is due

to the SDM sidelobe. The performance summary and comparison is in Table I. Compared with recent works, this paper has extremely low area consumption and excellent energy efficiency.

VIII. Conclusion

An ultracompact ADTX is proposed in this paper. This ADTX IP is described by RTL code and can be synthesized by logic and physical synthesize tools. Therefore, the ADTX IP can be easily implemented in various process technologies without tuning. In addition, this ADTX can cover a wide carrier frequency range, and can be universally used for IoT bands within carrier frequency range. Measurement results of prototype chip verified our ADTX design.

Acknowledgment

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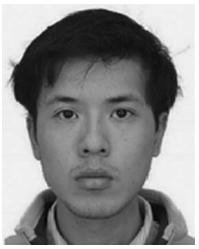

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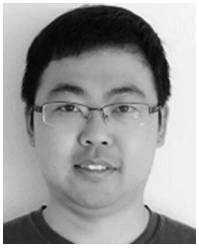

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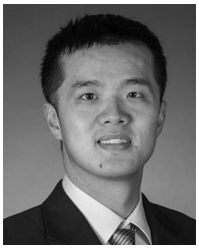

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