A 95 GHz Centimeter Scale Precision Confined Pathway System-on-Chip Navigation Processor for Autonomous Vehicles in 65nm CMOS

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***Abstract* — This paper presents a 95 GHz centimeter scale navigation system which allows a unmanned ground vehicle (UGV) or possibly even aerial vehicle (UAV) to navigate through a highly cluttered environment and follow a safe obstacle-free pathway to a desired goal. The navigation system defines multiple pathways using mm-wave base-stations called path generators and then uses a single CMOS SoC containing a receiver, ADC and an FFT processor to detect and navigate these pathways. The demonstrated confined pathway SoC (CP-SoC) occupies 5.4mm^2 of silicon area in 65nm technology, and consumes only 199 mW, making it suitable for lightweight payloads associated with UAVs and UGVs.**

Index Terms — Navigation System, UAV

I. Introduction

The rapid development of unmanned aerial / ground vehicle (UAV / UGV) technology not only for military applications, but also for commercial uses (mail & package delivery, remote security monitoring, transporting hazardous materials, search and rescue in debris) has created the need for higher and higher resolution navigation systems to enable operation in highly cluttered environments [1]. While GPS remains dominant for outdoor navigation, indoor environments are filled with a maze of walls, furniture, and other obstacles, and GPS reception itself is often unavailable [2,3]. For these emerging UAV/UGV navigation applications where cm-scale precision is required, we propose the Confined Pathway SoC (CP-SoC) navigation processor shown in Fig 1(a), which evolves from the software-only concept presented in [4] to add multiple pathway support and an SoC-based implementation for lower size/power/cost (as a PC is not needed).

II. Navigation Processor Architecture

In our confined path navigation processor a collection of pathway generators (base-stations) send out a set of mm-wave beams to define a grid of desired pathways through a cluttered indoor environment. Each pathway has the same mm-wave carrier so that a single CMOS receiver can be used to detect all signals and multiple-bands are not needed. However each path is modulated with a different ASK frequency so that they are distinct to the UAV/UGV vehicle's receiver/processor. The vehicle is programmed with a sequence of ASK frequencies to follow (for example 1.5 MHz, then 0.7 MHz, then 2.5 MHz in Fig 1). The vehicle will start out following the 1.5 MHz path until it detects the 0.7 MHz signal (the second frequency in the sequence). Once detected it will follow the 0.7 MHz signal until it detects the next step in the sequence (2.5MHz). After the last step of the sequence is followed it arrives at the destination.

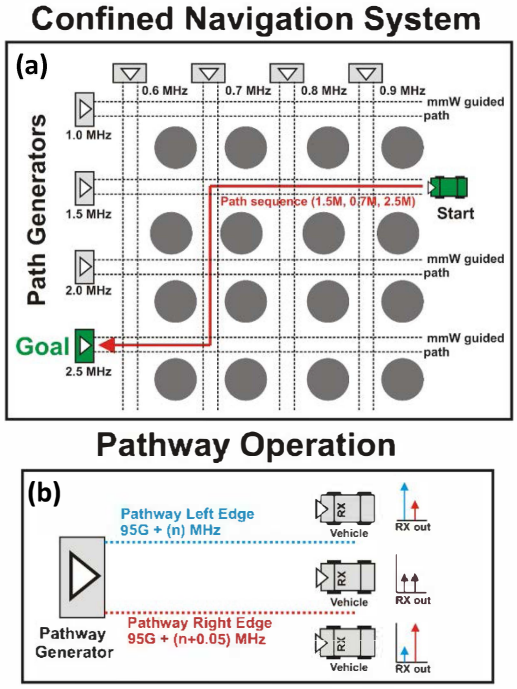

Fig 1(a). Overall confined path navigation system showing mm-wave pathway generators (base-stations) creating a grid that can navigate autonomous vehicles through safe defined pathways, each with a unique frequency. (b) The pathway is defined by two 95 GHz mm-wave beams transmit from a pathway generator. The right edge is ASK modulated at the path frequency while the left is offset by + 50 KHz.

The 95 GHz carrier was selected as it offers an excellent tradeoff between the antenna size (smaller at higher frequency) and availability of GaN PAs for the path generator modules (not readily available above W-band). In order to define the desired pathway for the UAV/UGV to follow, the path generator needs to generate two separate beams to define the left and the right side of the path. In order to distinguish right edge from left edge, the ASK frequency of the right edge is offset from the left side by 50 KHz as shown in Fig 1b. When the vehicle is close to the right edge of the 1 MHz pathway for example, the right ASK (1MHz + 50KHz) tone will have higher amplitude than the left edge (1 MHz). The vehicle then follows the centerline of each pathway by moving in the direction which balances the

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two ASK signals. Fig. 2(a) shows the block diagram of the path generator (implemented in III-V MMIC to obtain the necessary tx power), containing a 95 GHz LO, GaN PA, power splitter, two isolators, two ASK modulators and two transmit horns.

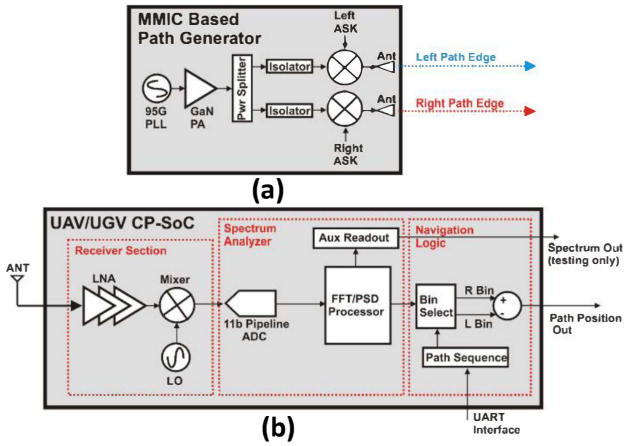

Fig 2(a). MMIC based path generator module which uses two modulated beams (left and right) to define the edge of each pathway. (b) UAV/UGV CP-SoC module carried on the vehicle to receive the 95 GHz pathway signal, identify the ASK tones with integrated spectrum analyzer, and make navigation decisions.

In order to remain compatible with the small payload size and power availability of UAVs/UGVs, we have developed the Confined Position System-on-Chip (CP-SoC) in 65nm CMOS shown in Fig. 2(b), which contains a 95 GHz receiver (to first capture the pathway signals), an integrated spectrum analyzer (ADC+FFT) to analyze each pathway's ASK signal, and navigation logic section to track the path sequence and determine the direction of the vehicle. The SoC's receiver schematic and measured performance is shown in Fig 3. Interestingly, the circuit can use a free-running LO, which normally would create frequency offset issues, but is okay for this application as the FFT bins are wide enough to accommodate drifts in the VCO frequency.

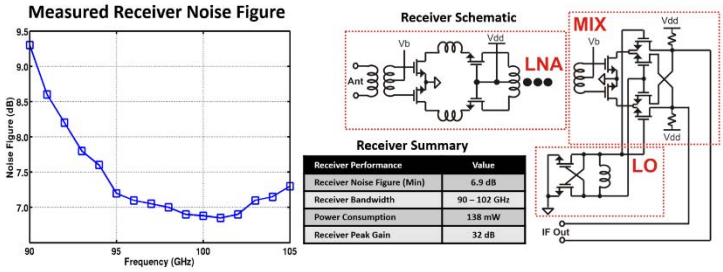

Fig 3. Schematic and measured performance for the receiver contained within the proposed CP-SoC, showing cascode-based amplification stages (5 stages total), mixer schematic, and LO generation.

The LNA is implemented as a 5-stage transformer-coupled cascode with series inductors as the cascode node to provide enhanced isolation and in-band stability. The NF of the receiver is shown to be competitive, as low as 7.5 dB from 95 to beyond 105 GHz, and 12 GHz bandwidth. Fig. 4 details the spectrum analyzer portion of the SoC. The ADC is implemented as a 1.5b per stage pipeline with op-amp sharing between adjacent stages to reduce power and area. The FFT processor is a fully-pipelined complex (IQ) radix-2 implementation with 128 points and a squaring function to compute the PSD. With this 128 point, 128 different frequencies can be distinguished, supporting an overall system with up to 64 different pathways.

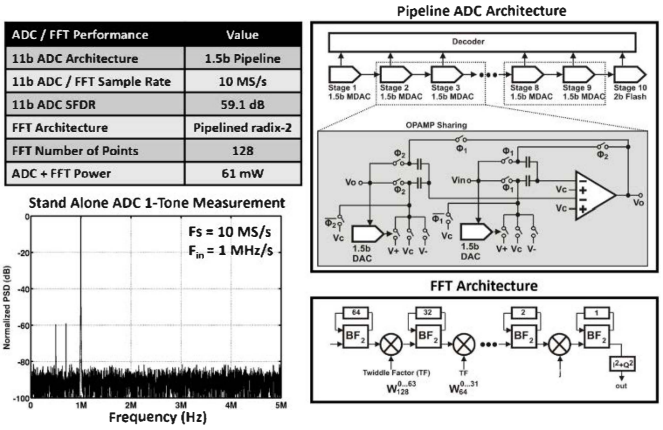

Fig 4. Block diagram and performance summary for the spectrum analyzer within the proposed CP-SoC, including 11b op-amp sharing pipeline ADC and 128 point radix-2 complex (IQ) FFT processor.

More pathways can be supported by increasing the FFT point count further. Fig. 5 shows the testing setup used to validate the proposed confined pathway navigation system, including the assembly details of the path generator and UAV/UGV SoC.

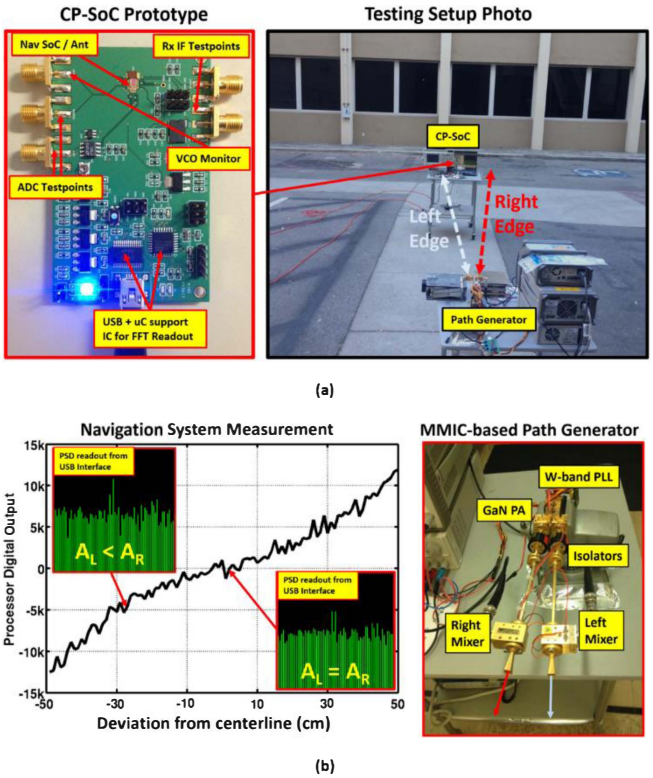

Fig 5(a). Test setup showing the CP-SoC prototype and location of the path edges, (b) Path generator assembly and measurements of amplitude difference between the left and right edge ASK signal amplitude as the CP-SoC is moved across the pathway. Also shown

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are downloaded spectrums at two points on the deviation vs. output code response.

The CP-SoC is bonded onto a PCB with regulators & support ICs for downloading the spectrum to a PC computer, as well as a specialized antenna module [5] originally developed at JPL for phase array applications. The antenna is implemented on a high-resistivity silicon substrate and beam lead connected to the CMOS CP-SoC via a differential RF port. The remaining DC and control connections are wire-bonded directly to the PCB on the 3 edges of the SoC not occupied by the RF interface.

To validate pathway operation, the CP-SoC and path generator are set up on two push-carts 5 m apart and the amplitude difference of the right and left edge signals are plotted in Fig. 5 as the pathway is crossed. The units of y-axis in Fig. 5 are relative digital amplitude values originating from the size of the ADC LSB referred through the gain of the FFT processor. When the CP-SoC is near the left edge of the pathway (-50 cm) the value of (A_{right}-A_{left}) is very negative (<10K codes) as the left signal is dominant. In the middle of the pathway (0 cm) the SoC output value is almost zero as A_{left} = A_{right}. At the right edge of the pathway (50 cm) the right side is dominant so the value of (A_{right}-A_{left}) is very positive (>10K codes). As the digital code changes significantly (>1000) with only 3-4 cm of displacement, the vehicle can easily follow the pathway with cm-scale accuracy even at several meters away. Experiments show accuracy can be improved by averaging multiple measurements at the cost of latency, which will limit the maximum speed of the vehicle relative to the widths of the pathways, and spacing of obstacle clutter.

VI. Conclusions

MMIC Path Generator Summary		
Saturated Output Power	20 dBm	
Power Dissipation	1325 mW	
Weight	0.5 Kg	
Frequency	95 GHz (Fixed DRO)	
UAV / UGV CP-SoC Summary		
Power Dissipation	199 mW (138mW for Rx / 61mW Digital+ADC)	
Die Area	5.4 mm^2	
Receiver Noise Figure	<7.5 dB	
Receiver Bandwidth	90-102 GHz	
Spectrum Analyzer Bandwidth	5 MHz (10 MS/s)	
Spectrum Analyzer Point	128 point	
Technology	65nm CMOS (TSMC)	
Navigation System Performance	**[4]**	**This Work**
Implementation	FPGA / PC	CMOS SoC
Frequency	144 GHz	95 GHz
Maximum Range	10 m	125 m (computed from SNR)
Position Accuracy	<10 cm	< 5.3 cm (computed from Fig 5)
Power Consumption on UAV/UGV payload	> 10W (FPGA/PC based)	199 mW

Fig 6. Performance summary of proposed CP-SoC navigation processor and comparison to the PC/FPGA based navigation system proposed in [4].

This CP-SoC has been developed for UAV/UGV guidance based on known confined paths for passage through highly cluttered environments. The system achieves centimeter precision by comparing the ASK modulation amplitudes of a 95 GHz signal defining the edge of each pathway. The small chip size (5.4mm2) and low total power consumption (199 mW) make it ideal for battery powered UAVs/UGVs where size/power constraints are critical. Fig 6 summarizes the CP-SoC performance and compares to the software-based system implementation in [1]. Fig. 7 shows the die photo of the CP-SoC with the external antenna module (connected with a beam lead interface) and major circuit blocks of the mm-wave receiver and integrated spectrum analyzer identified.

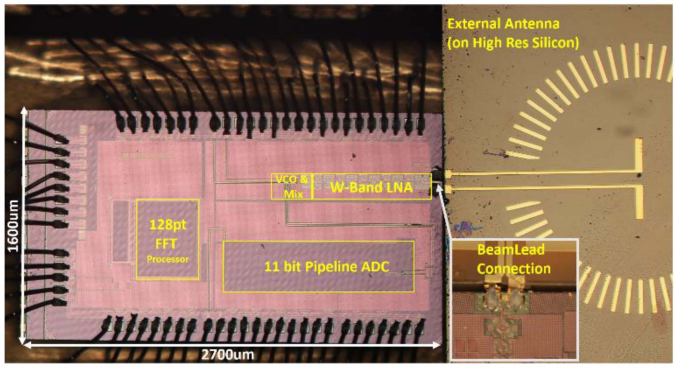

Fig 7. Die photo of the proposed SoC navigation processor combined with the external beam-lead connected antenna module (from [5]) with major blocks identified.

Acknowledgement

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