

Cycle	1	2	3	4	5	6	7	8	9	10
LDR r1, [r3]	Main	FIFO	Monitor							
LDR r2, [r3, #4]		Main	FIFO		Monitor					
ADD r0, r1, r2			Main	FIFO			Monitor			
ADD r0, r0, #15				Main	STALL		FIFO		Monitor	
STR r0, [r4]								Main	STALL	FIFO
Fifo Entries Free	2	1	1	0	0	0	0	0	0	0