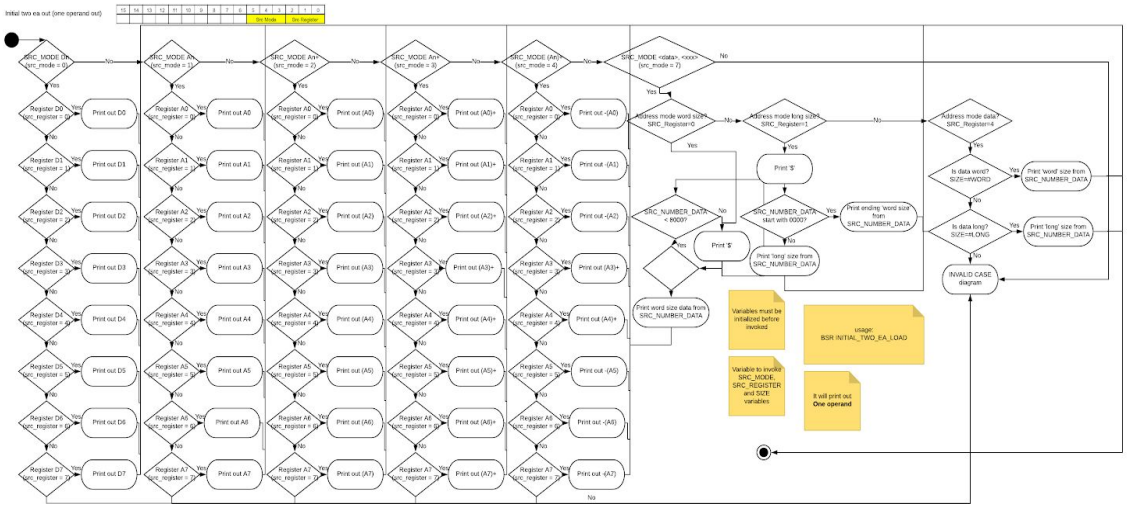
Program Description

Design Philosophy:

1. Making subroutines which can apply to as many cases as possible for disassembling.
2. Modularize the subroutines so that logical error in a subroutine does not affect the entire program.
3. Minimizing data and address register usage, so that other subroutines can utilize more data and address registers.
4. Detailed flow charts so that the developer can easily trace the error and debug.

Flowchart:



This subroutine is for printing an operand that uses the SRC_MODE variable and SRC_REGISTER variable. Based on this subroutine, every opcode can print every operand.

Limitations:

1. The valid range of this code is from #$3500 ~ #%9FFF, because our program does not have enough test on disassembling memory more than %10000
2. Sometimes open data change the PC of the assembly, so in case that PC is modified from $1000, the user must modify the PC to $1000 first, and then run the program.
3. If the user of the program load the data in between $1000 ~ $3500, the program will not run. (Do not override testing code on our code!)