

ECE 65 – Components and Circuits Lab

Lab 4 Report – Diode Waveform Shaping Circuits

May 4, 2023

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Abstract

The purpose of this lab was to analyze and simulate three circuits: a rectifier and peak detector circuit, an op-amp peak detector circuit, and a clamp circuit. The experiments involved first simulating via software the given circuit sans capacitor, and then with a capacitor in parallel with the resistor as shown to build a peak detector circuit, plotting both results to determine the optimal peak detector value between 1nF and 100nF (small and large relatively). Next, the op-amp peak detector was simulated in order to show the comparator function of the op-amp, in which it maximizes output voltage with a synchronous periodic dip with the input voltage, operating as a peak detector as in part 1. Then, the clamp circuit was next to be analyzed, and after simulation, we noted the clamped circuit goes from a DC offset of -5V to 5V to fully negative; the output DC offset was -10V to 0V. Building the circuits in the lab using various resistors, capacitors, 1N4148 diodes, and the LF411 op-amp, we were able to verify the results from our simulations and achieve the desired waveform shapes using the function generator for input and the oscilloscope for plotting.

Experimental Procedures and Results

Problem 1: Rectifier & Peak Detector Circuit

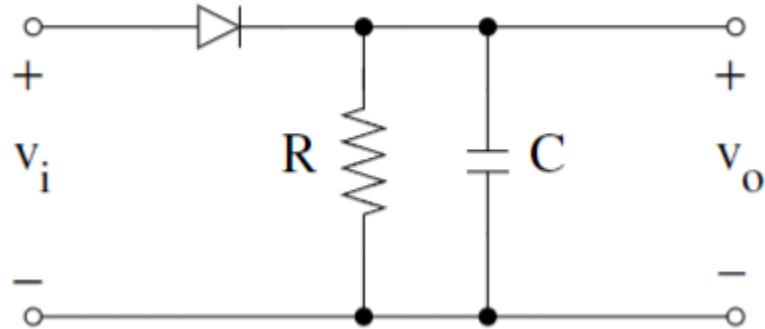


Figure 1: The circuit to be simulated in PSpice

1. First, we simulated the above circuit in LTSpice without the capacitor, with $R = 100\text{k}\Omega$, a 1N4148 diode, and V_i being a sinusoidal wave with an amplitude = 5V, DC offset = 0, and frequency = 2 kHz, with an appropriately small step size.

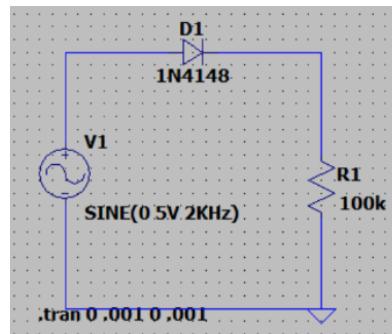


Figure 2: Circuit 1 (no capacitor) simulation

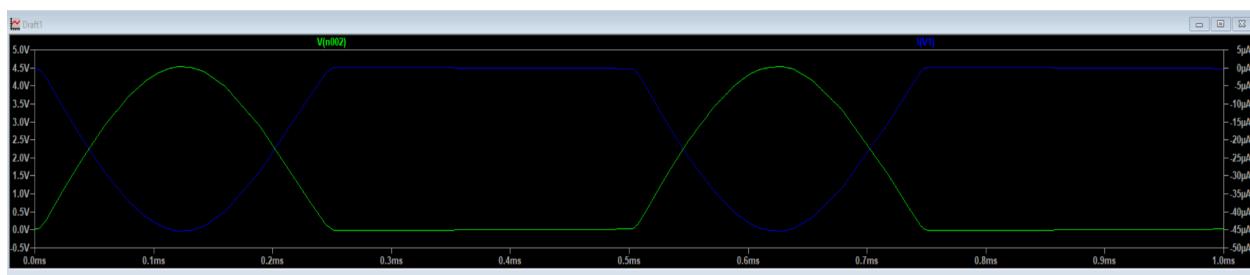


Figure 3: Circuit 1 (no capacitor) plots of V_i , V_o

2. Then, by adding a capacitor in series with the resistor as shown, we simulated the rectifier circuit. The three possible values of the capacitor we chose were 1 nF, 50nF, and 100nF. As voltage equals charge divided by capacitance, with a very small capacitor, high voltages are possible, but with the largest possible capacitance, the lowest voltages are attainable, an undesirable feature when building a peak detector. The peak detector also has a shorter and more relevant time constant when comparing the three plots and the values of τ .

3. The plots of three peak detector capacitance values:

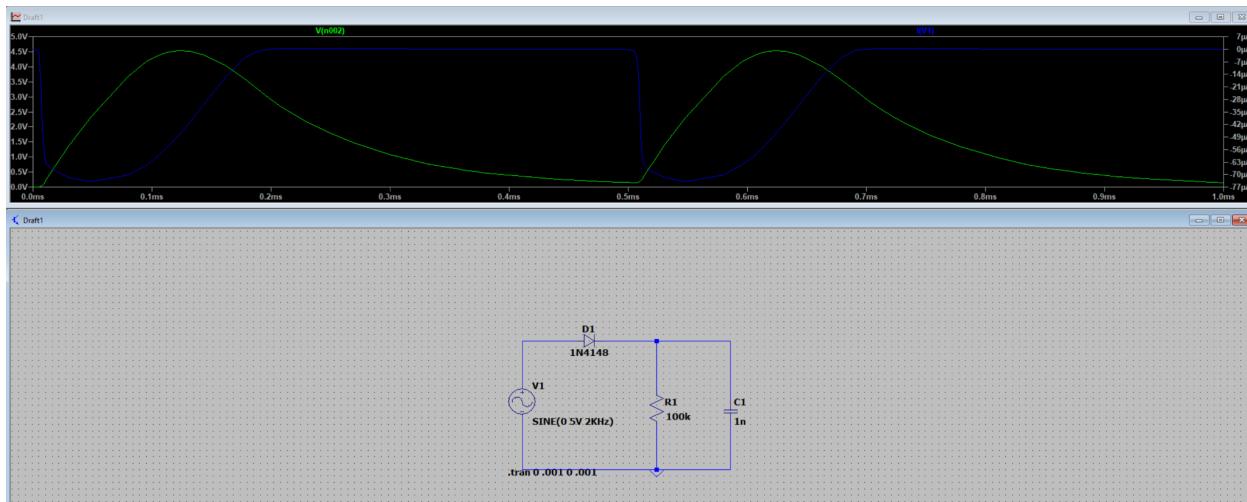


Figure 4: Plot of peak detector capacitance = 1nF

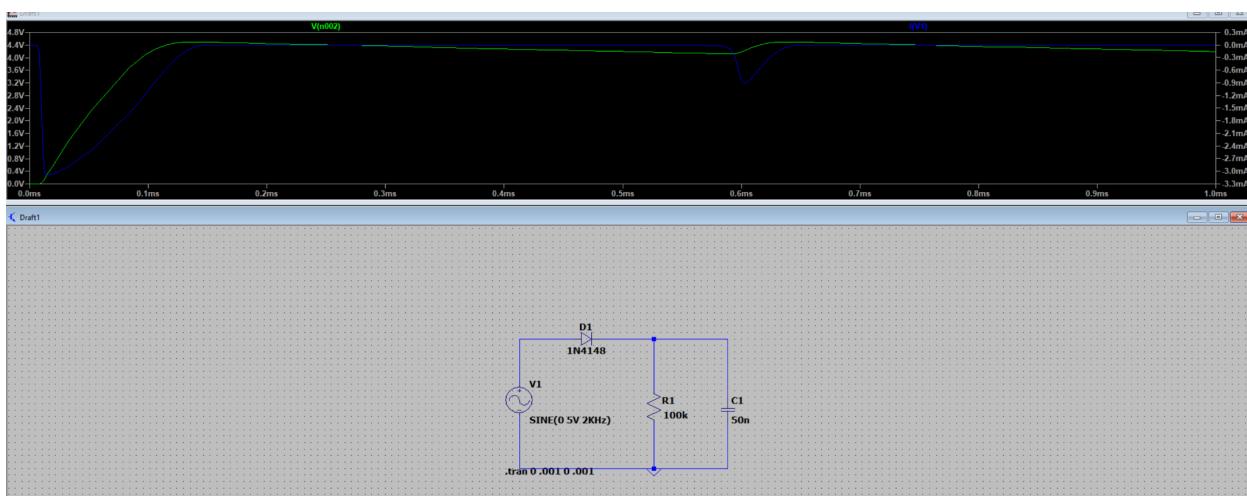


Figure 5: Plot of peak detector capacitance = 50nF

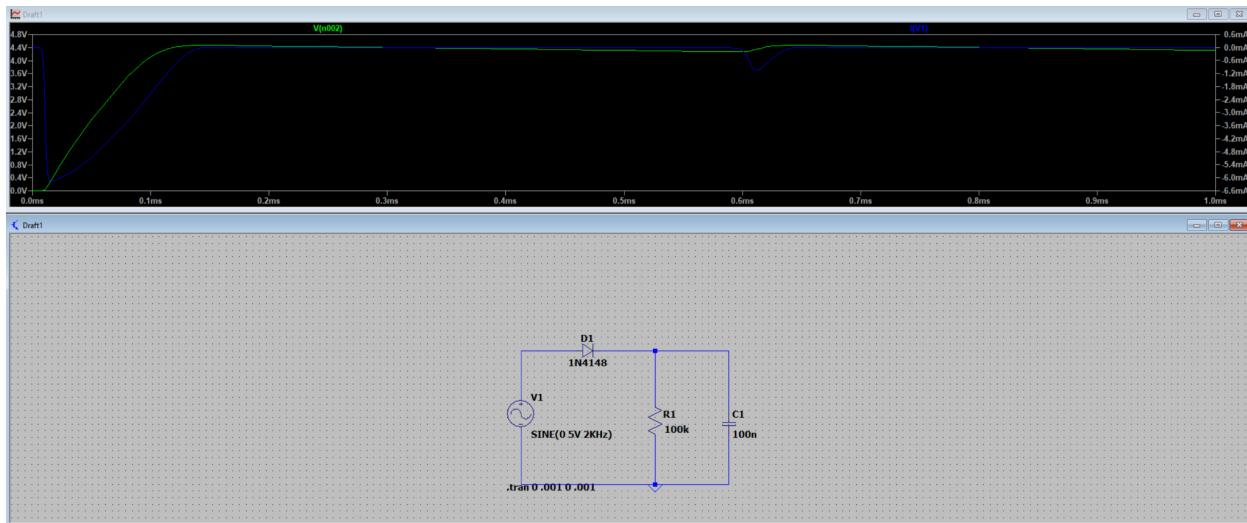


Figure 6: Plot of peak detector capacitance = 100nF

4. Our plots did match our expectations, as from observation the smallest capacitor provides the most accurate depiction of the peak detector behavior, and the peak detector observably performs “worse” with less accuracy as the capacitor size increases.

1. We then constructed the circuit on the breadboard, sans capacitor.

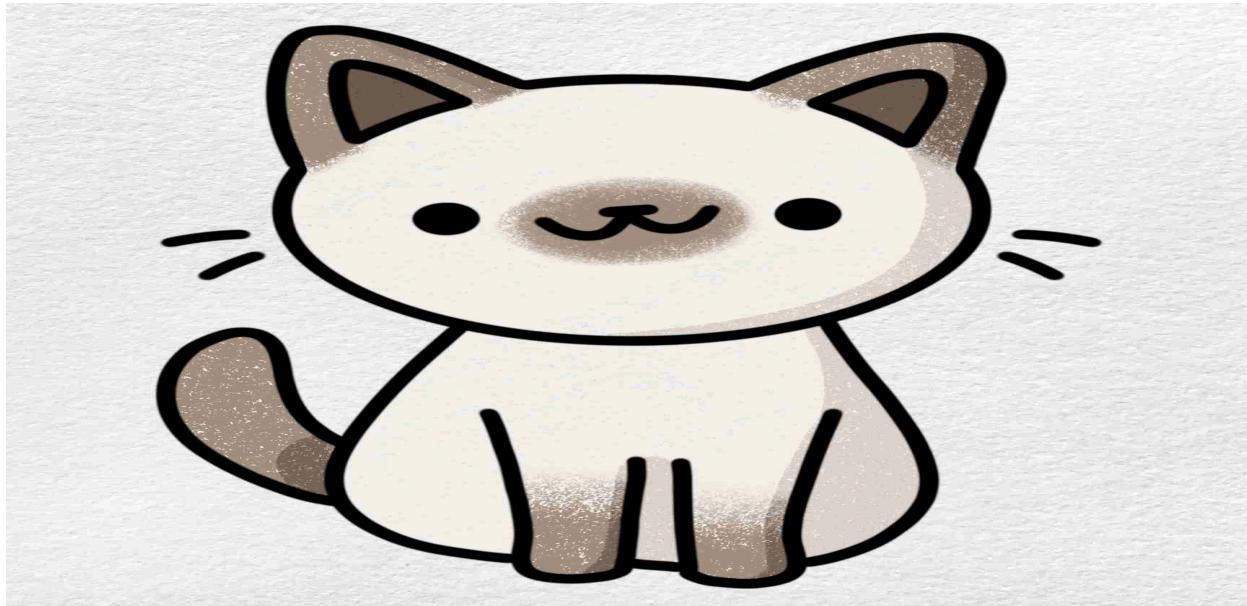


Figure 7: Circuit 1 on the breadboard, no capacitor.



Figure 8: Plot of Circuit 1 waveforms V_o and V_i , no capacitor.

2. Then, we set the function generator for V_i = a sinusoidal wave with an amplitude = 5V, DC offset = 0, and frequency = 2 kHz for channel 1 as the “trigger,” and channel 2 being V_o .
3. We then set both channels to the largest volts per division setting.
4. After that, we moved the two traces to center the zero voltage values for both channels.
5. We then expanded the time selection for 2 periods of the waveform.
6. After using no capacitor, we repeated this process with 10nF, 50nF, and 100nF capacitors oriented as in the pre-lab simulation.
7. We took pictures of each oscilloscope display as shown.
8. Then we repeated the process for each circuit for the three capacitances:

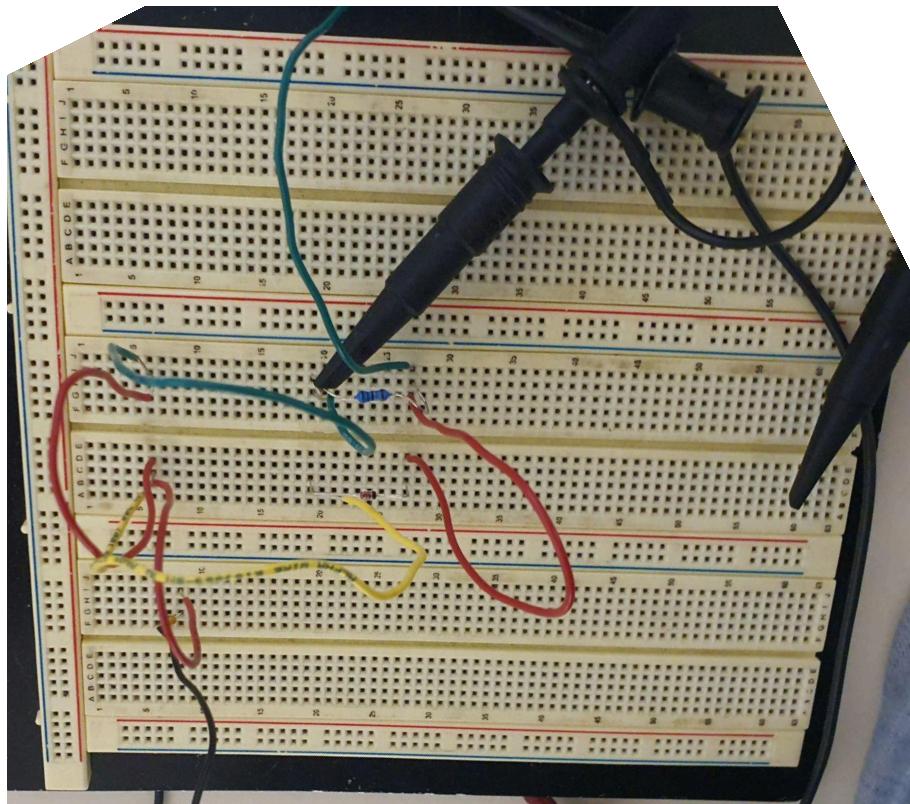


Figure 9: Circuit 2 on the breadboard, 1nF capacitor.

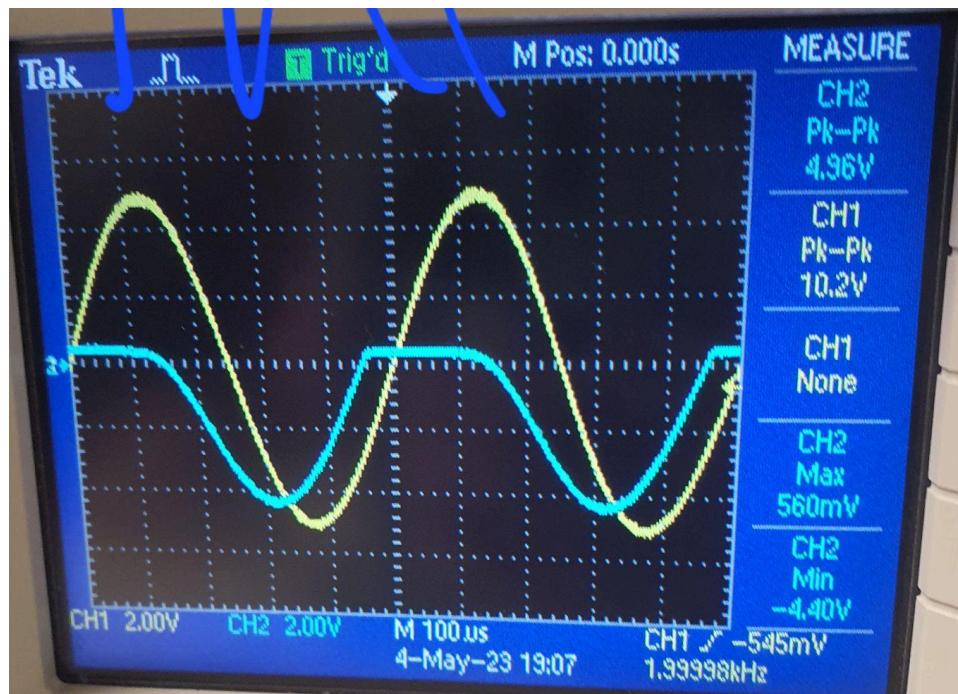


Figure 10: Circuit 2 plotted, V_o & V_i



Figure 11: Circuit 3 on the breadboard, 50nF capacitor.

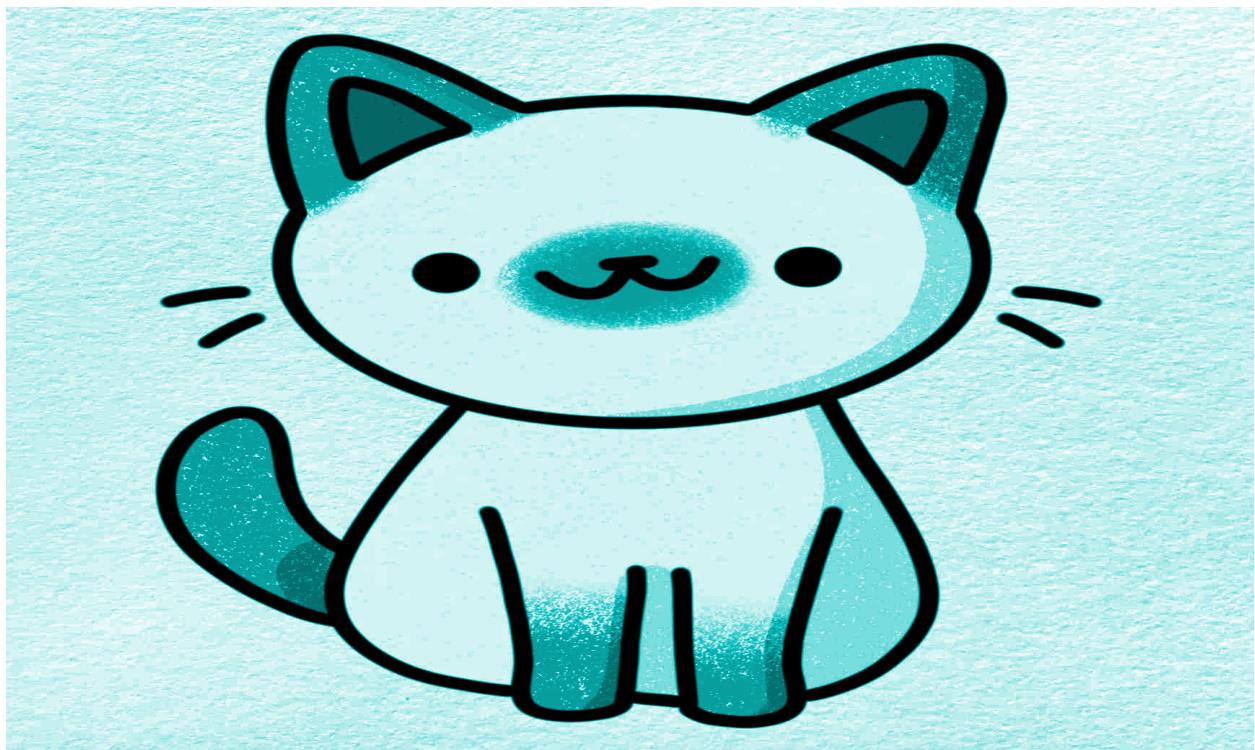


Figure 12: Circuit 3 plotted, Vo & Vi

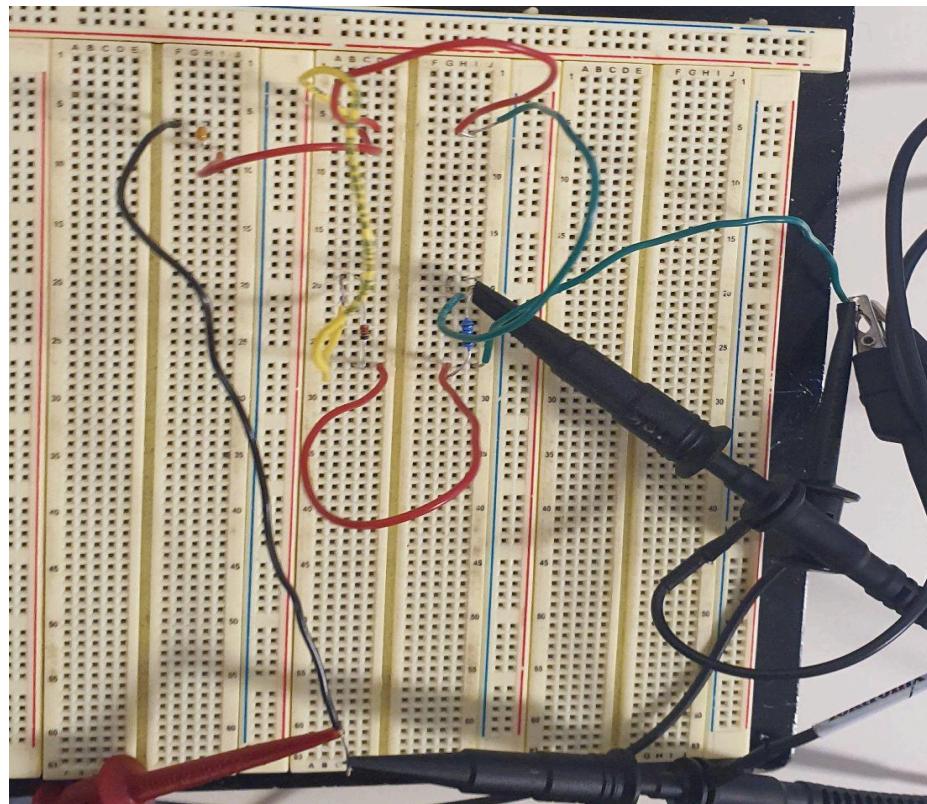


Figure 13: Circuit 4 on the breadboard, 100nF capacitor.

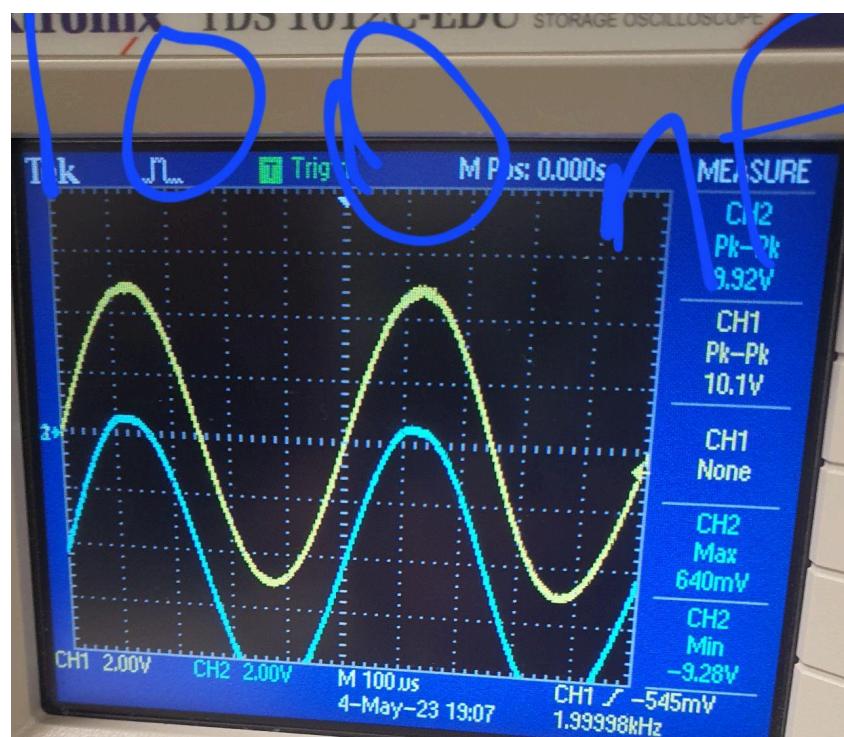


Figure 14: Circuit 4 plotted, V_o & V_i

9. Our conclusions followed that from the pre-lab simulation; the larger the capacitance the weaker the peak detecting effect of the circuit was. We could see by observing the waveforms that the 1nF capacitor had the most accurate peak detection.

Problem 2: Op-amp Peak Detector

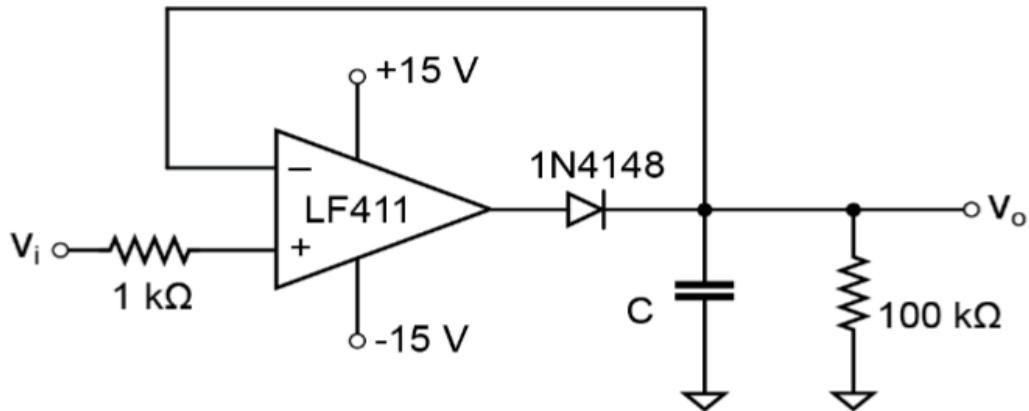


Figure 15: The op-amp circuit to be analyzed.

- First, we simulated the circuit using software, with a 1N4148 diode, $C = 10\text{nF}$, and V_i = a sinusoidal wave with an amplitude = 5V, DC offset = 0, and frequency = 2 kHz, with an appropriately small step size (again) and two full periods for V_i and V_o (experiment 1 with $C = 10\text{nf}$ shown below):

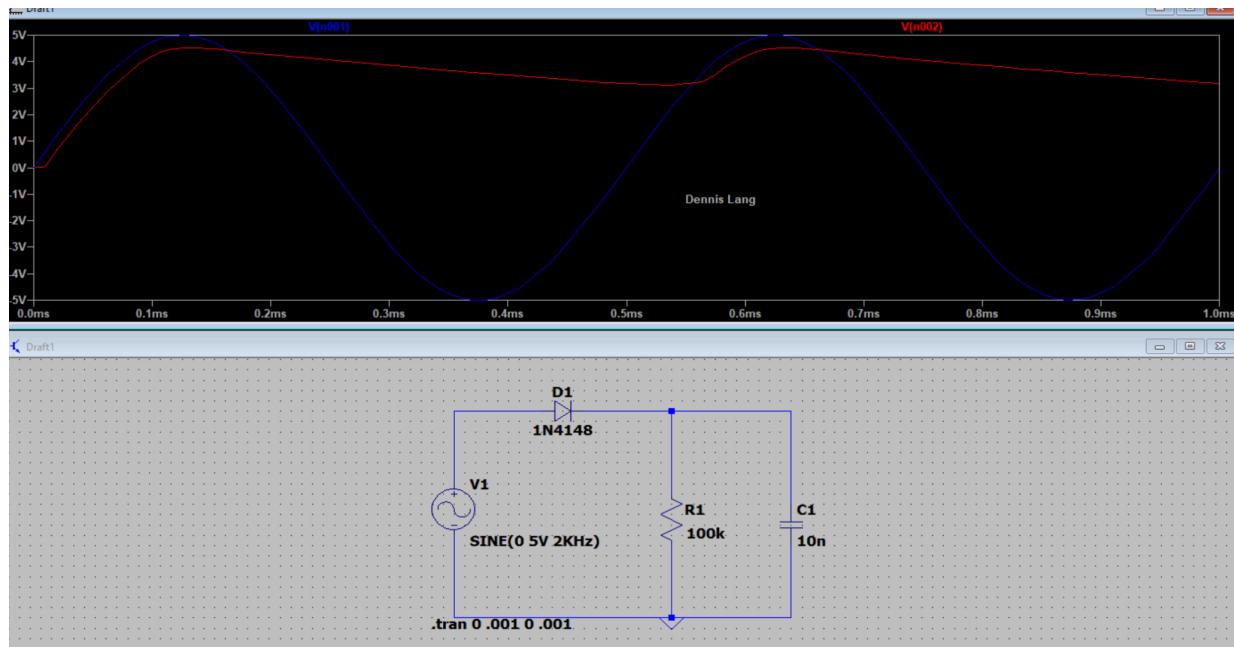


Figure 16: The circuit from part 1 with $C = 10\text{nF}$.

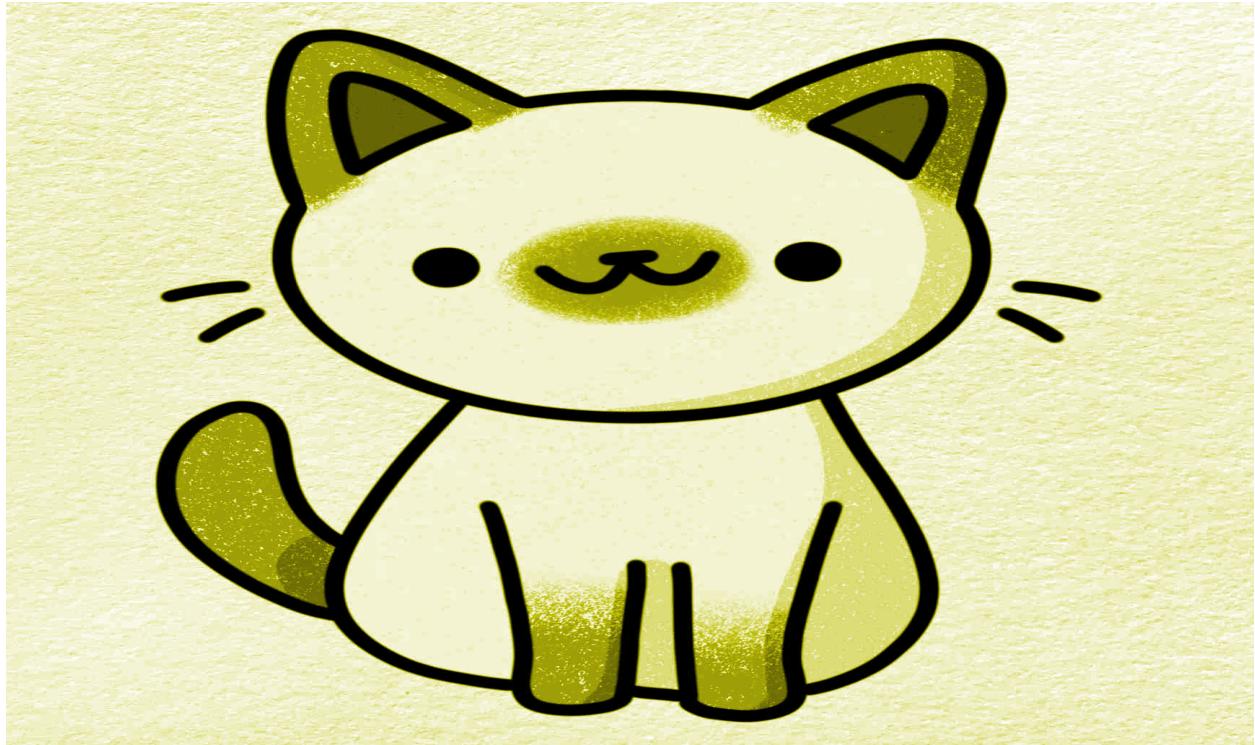


Figure 17: The op-amp circuit plotted, V_o and V_i (C also is $10nF$)

2. With $C = 10nF$, this circuit is undergoing the same peak voltage detection function as the previous example, but using the op-amp to avoid constantly needing to discharge the capacitor. The way the circuit works is that the op-amp acts as the comparator, to keep the output voltage near maximum at all times, and the diode allows high voltage to pass through to the capacitor for storage and output of the highest voltage.

1. We then assembled the circuit in the lab with the function generator now responsible for the same sinusoidal wave we've been inputting: a sinusoidal wave with an amplitude = 5V, DC offset = 0, and frequency = 2 kHz, with an appropriately small step size and two full periods for V_i and V_o as scope channels 1 and 2 respectively:

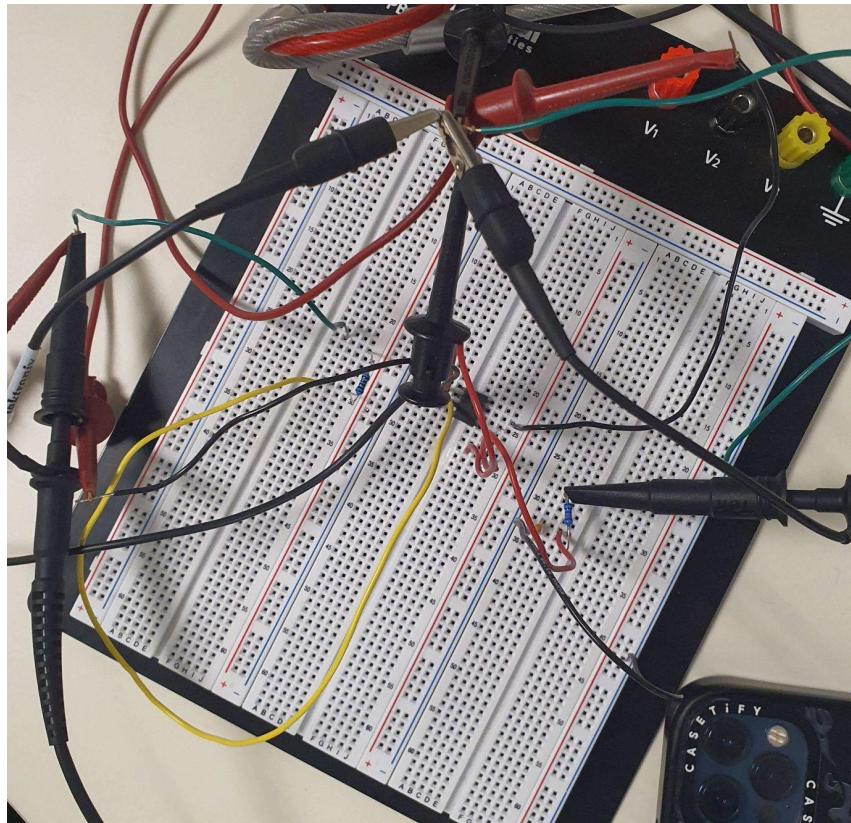


Figure 18: The op-amp circuit on the breadboard

2. The oscilloscope display is shown here:



Figure 19: The op-amp circuit plotted, V_o and V_i ($C = 10\text{nF}$), on the oscilloscope

Problem 3: Clamp Circuit

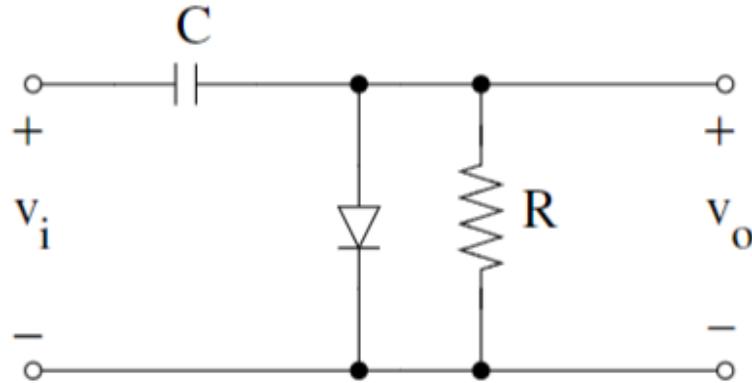


Figure 20: The given clamp circuit

- We simulated this clamp circuit in the lab with the same sinusoidal wave we've been inputting: a sinusoidal wave with an amplitude = 5V, DC offset = 0, and frequency = 2 kHz, with an appropriately small step size and two full periods for V_i and V_o ; using $R = 100\text{k}\Omega$, $C = 100\text{nF}$ and a 1N4148 diode:

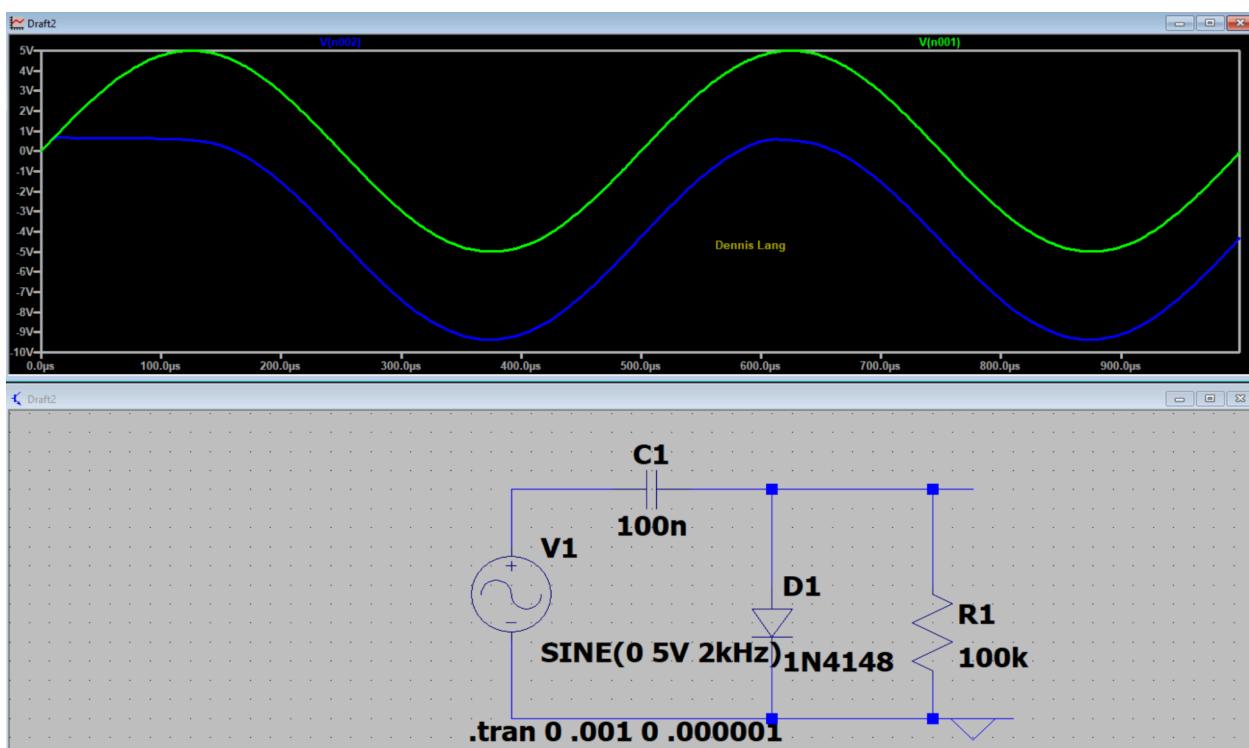


Figure 21: Clamp circuit V_o and V_i with $C = 100\text{nF}$

2. We also performed the experiment with a 1nF capacitor for V_o and V_i :

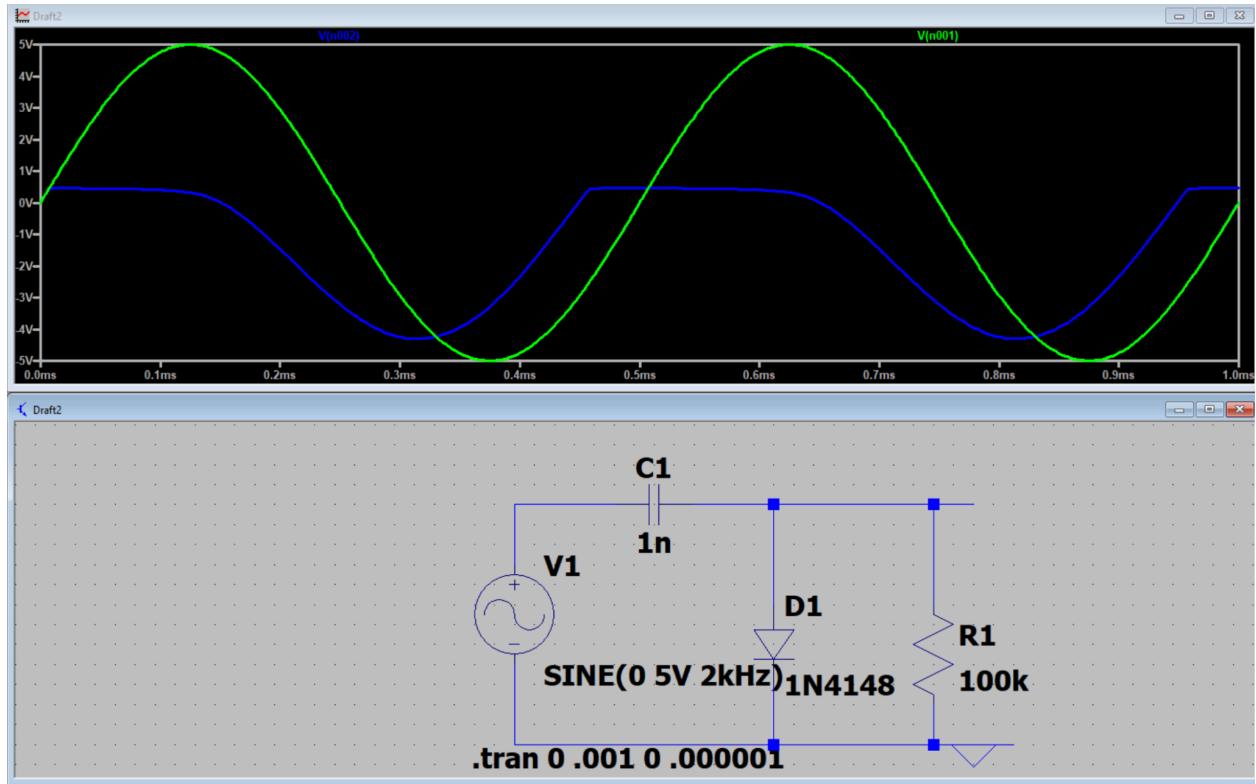


Figure 22: Clamp circuit V_o and V_i with $C = 1\text{nF}$

3. We determined that the first circuit clamps the input voltage from our input -5V to 5V with no DC offset to a full negative version, -10V to 0V, an expected behavior from such a small (almost negligible capacitance). Increasing the capacitance to a more relevant number for our desired circuit output, the clamping at 100nF is now half negative, or the clamping only appears on the 0V to 5V while the negative side is preserved.

1. We then built the circuit by hand with our same function generator sinusoidal wave we've been inputting: a sinusoidal wave with an amplitude = 5V, DC offset = 0, and frequency = 2 kHz, with an appropriately small step size and two full periods for V_i and V_o as scope channels 1 and 2 respectively (for $C = 100\text{nF}$):

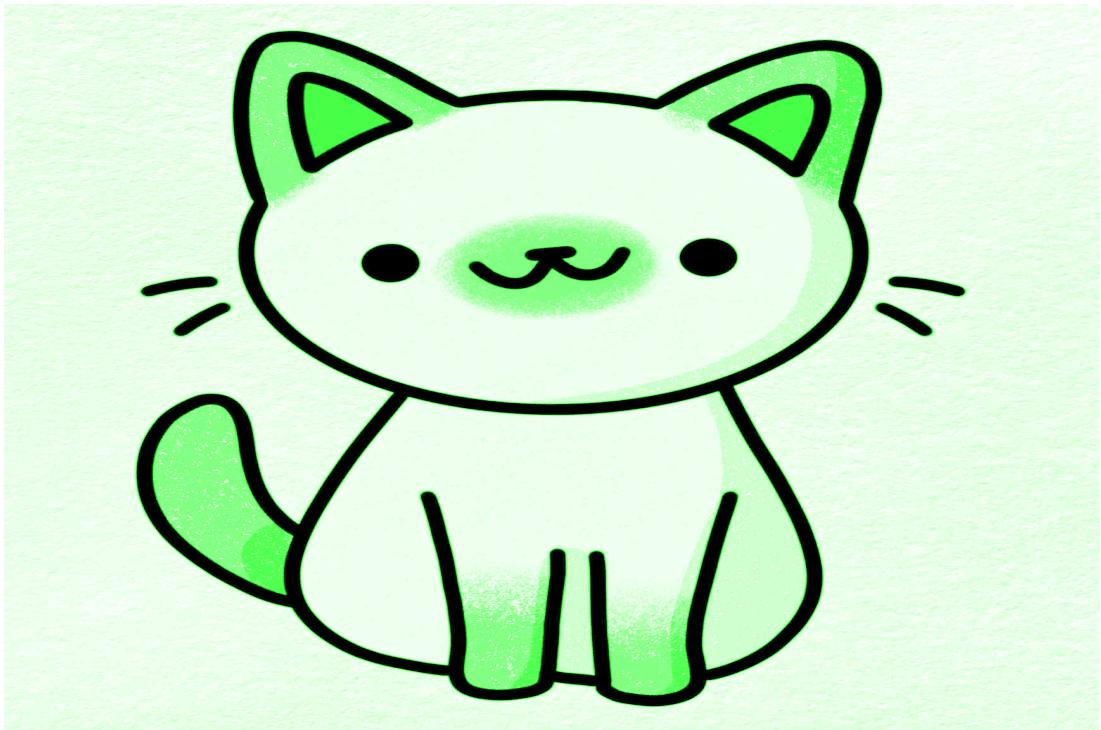


Figure 23: Oscilloscope display of clamp circuit ($C = 100\text{nF}$)

2. We then repeated the same for $C = 1\text{nF}$:

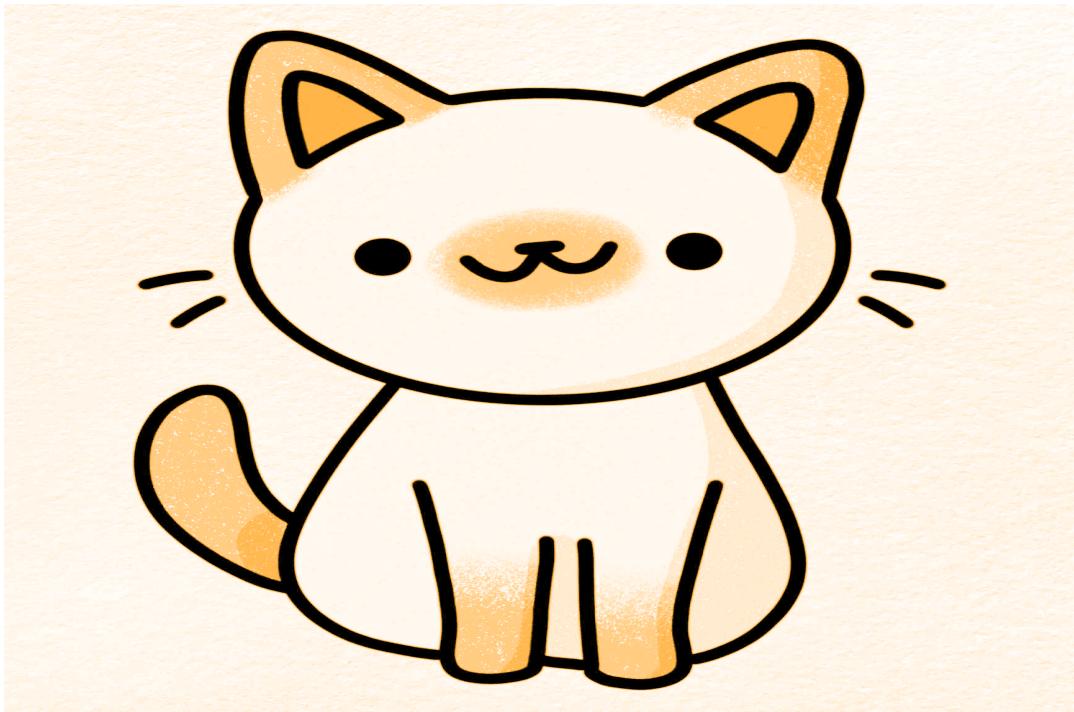


Figure 24: Oscilloscope display of clamp circuit ($C = 1\text{nF}$)

3. We concluded the same as the pre-lab experiment: the original, high-capacitance circuit clamps the input voltage from our input -5V to 5V with no DC offset to a full negative version, -10V to 0V, an expected behavior from such a small (almost negligible capacitance). Increasing the capacitance to a more relevant number for our desired circuit output, the clamping at 100nF is now half negative, or the clamping only appears on the 0V to 5V while the negative side is preserved.

Conclusion

We analyzed three circuits in this lab, each with the same input voltage using a sinusoidal waveform voltage with an amplitude of 5V, a DC offset of 0, and a frequency of 2 kHz, with 1% ratio step size for smooth results and two full periods for input and output voltages. The first circuit to be analyzed in this lab was a rectifier and peak detector circuit with a $100\text{k}\Omega$ resistor, 1N4148 diode, and an initially missing capacitor. The second was an op-amp peak detector circuit with an LF411 op-amp, resistors, and capacitor. The third was a clamp circuit with a 1N4148 diode, $100\text{k}\Omega$ resistor, and two separate capacitance values.

For the first experiment, LTSpice was used to model the circuit with no capacitor to see the mirrored waveform, and then with a capacitor parallel before the resistor as shown in the diagram to build a peak detector circuit, plotting both results to determine the optimal peak detector value for comparatively large and small capacitors. After building a physical model, we determined that as voltage equals charge divided by capacitance, as capacitors store the charge, with a very small capacitor, certain voltages are possible to be output but with the largest possible capacitance, a smaller variance of voltages are attainable. The peak detector also has a shorter and more relevant time constant with a small capacitor when comparing the three plots and the values of τ , as we are using a small step so we clearly want a more precise reading via the smaller capacitor's capabilities giving us the most accurate peak detection.

Next, the op-amp peak detector was simulated in order to show the ability of the op-amp to act as a peak detector in circuits. With the arranged circuit diagram in LTSpice, we were able to obtain peak detecting output voltage from the sinusoidal given input. The more "standard" peak detector waveform is modeled here vs experiment 1, as the op-amp configuration doesn't require the capacitor's discharge as it usually would, so it results in a more accurate waveform

than previous. We verified these results with the oscilloscope and function generator on a physical breadboard, and were able to match the waveforms on the oscilloscope.

Finally, we analyzed in LTSpice a clamping circuit, which takes an input waveform and uses (in our example) a capacitor, a 1N4148 diode, and a $100\text{k}\Omega$ resistor. We noticed that the circuit with a 1nF capacitor clamps the input voltage from our input -5V to 5V with no DC offset to a full negative version, -10V to 0V , an expected behavior from such a small capacitance value. Increasing the capacitance to a more relevant number for our desired circuit behavior, with the capacitance now at 100nF , the clamping is now half negative, or the waveform is restricted to only negative outputs (-5V to 0V). We concluded that using an appropriately high capacitance is the correct means of clamping a circuit to either negative or positive values only.