



PONTIFICIA UNIVERSIDAD CATOLICA DE CHILE  
SCHOOL OF ENGINEERING

**DISCRETE-TIME NOISE FILTERING FOR  
PULSE-PROCESSING IN PARTICLE  
PHYSICS EXPERIMENTS**

**DIEGO ÁVILA GÁRATE**

Thesis submitted to the Office of Research and Graduate Studies  
in partial fulfillment of the requirements for the degree of  
Master of Science in Engineering

Advisor: ÁNGEL ABUSLEME HOFFMAN

Santiago de Chile, April 2014

© MMXIII, DIEGO ÁVILA GÁRATE



PONTIFICIA UNIVERSIDAD CATOLICA DE CHILE  
SCHOOL OF ENGINEERING

**DISCRETE-TIME NOISE FILTERING FOR  
PULSE-PROCESSING IN PARTICLE  
PHYSICS EXPERIMENTS**

**DIEGO ÁVILA GÁRATE**

Members of the Committee:

ÁNGEL ABUSLEME HOFFMAN

ENRIQUE ÁLVAREZ FONTECILLA

PROFESOR INVITADO

JAIME NAVÓN COHEN

Thesis submitted to the Office of Research and Graduate Studies  
in partial fulfillment of the requirements for the degree of  
Master of Science in Engineering

Santiago de Chile, April 2014

© MMXIII, DIEGO ÁVILA GÁRATE



## **ACKNOWLEDGEMENTS**

First and foremost I'd like to thank my advisor, Professor Ángel Abusleme, whose enthusiasm, patience, and knowledge, were fundamental to achieve the most precious goal of any grad student, reach the end of his thesis.

I wish to thank to all those who are and were members of the IC-UC group, and especially to Professor Enrique Álvarez, Hernán Campillo and Cristóbal Alessandri.

I would like to express my gratitude to Cleve Moler, for making such a terrific piece of software call MATLAB, which was a fundamental tool for the development of this thesis. I am also extremely grateful to Gottfrid Svartholm, Fredrik Neij and Peter Sunde.

Finally, I want to thank to my family for the continuous love they have provided me since I was a couple of cells (a.k.a gametes) living apart.

## TABLE OF CONTENTS

ACKNOWLEDGEMENTS . . . . .	iv
TABLE OF CONTENTS . . . . .	v
LIST OF FIGURES . . . . .	vii
LIST OF TABLES . . . . .	ix
ABSTRACT . . . . .	x
RESUMEN . . . . .	xi
1. INTRODUCTION . . . . .	1
1.1 Particle physics experiments . . . . .	1
1.2 Electronics for particle physics experiments . . . . .	2
1.3 Noise minimization in circuits for particle physics instrumentation . . . . .	3
1.4 Thesis content . . . . .	5
2. PROBLEM DEFINITION . . . . .	7
2.1 The International Linear Collider . . . . .	7
2.2 The Bean . . . . .	8
3. NOISE ANALYSIS IN PULSE-PROCESSING DISCRETE-TIME FILTERS . . . . .	9
3.1 Introduction . . . . .	9
3.2 Discrete-Time Analysis . . . . .	10
3.3 Example . . . . .	15
3.4 <i>ENC</i> Minimization . . . . .	19
3.5 Conclusion . . . . .	23
4. A SC FILTER FOR ARBITRARY WEIGHTING FUNCTION SYNTHESIS . . . . .	25
4.1 Introduction . . . . .	25
4.2 System-Level Design . . . . .	25

4.2.1	Filter Specifications . . . . .	26
4.3	Circuit Design . . . . .	27
4.3.1	Operational Transconductance Amplifier . . . . .	28
4.3.2	Variable Capacitor . . . . .	31
4.3.3	Rail-to-Rail buffer . . . . .	31
4.3.4	IC bias network . . . . .	33
5.	RESULTS . . . . .	36
5.1	The Bean 2 prototype Implementation . . . . .	36
5.2	Filter simulation results . . . . .	36
6.	CONCLUSION . . . . .	44
6.1	Summary . . . . .	44
6.2	Future work . . . . .	44
	APPENDIX . . . . .	45
A.	The Bean 2 prototype pinout . . . . .	46
	References . . . . .	50

## LIST OF FIGURES

1.1	Block diagram for a single channel, generic instrumentation circuit for particle physics experiments. . . . .	2
1.2	CSA using a voltage amplifier. Detector is modeled as a photodiode. . . . .	4
3.1	Model for noise analysis in a typical front-end circuit. . . . .	11
3.2	Noise contribution of the pulses generated within $P_i$ and measured at an arbitrary sample $k$ (i.e., $t = kT_s$ ), using an arbitrary filtered noise core function $\hat{y}(t)$ . The independent contribution of each pulse is pointed out with black dots.	13
3.3	Evolution of the total integrated noise at the filter input, where the noise of each sample was split according to (3.10). . . . .	15
3.4	$\sigma^2(t)$ for thermal, shot and flicker noise with normalized time $t/\tau$ and an arbitrary amplitude. . . . .	16
3.5	Front-end circuit used for noise analysis. . . . .	17
3.6	$\hat{\sigma}_{\text{th}}^2(N)$ and $N \frac{\overline{v_n^2}}{2\hat{\tau}} \frac{C_{tot}^2}{C_F^2}$ as a function of $\hat{\tau}$ , using $\overline{v_n^2} = 1$ , $C_{tot}^2/C_F^2 = 1$ and $N = 20$ .	18
3.7	Minimum $ENC^2$ as a function of $\hat{\tau}$ for a fixed $N$ . . . . .	22
3.8	Optimum WF for different values of $\hat{\tau}$ for $N = 20$ . . . . .	23
3.9	Optimum $ENC^2$ as a function of $N$ for $\hat{\tau} = 0.03 \mu\text{s}$ . . . . .	24
4.1	Simplified filter schematic. Reset switches are depicted in gray. . . . .	26
4.2	Recycling folded cascode OTA schematic. Three terminal NMOS and PMOS devices are with their bodies tied to ground and $V_{DD}$ respectively. . . . .	29
4.3	OTA discrete-time common-mode feedback circuit schematic. . . . .	30
4.4	OTA bias network schematic. . . . .	30
4.5	6-bit programmable capacitor. . . . .	31
4.6	Rail-to-rail operational amplifier schematic. . . . .	33
4.7	Op-amp bias network schematic. . . . .	34

4.8	Current distribution bias scheme. . . . .	35
4.9	$\beta$ -multiplier bias schematic. . . . .	35
5.1	The Bean 2 prototype layout. . . . .	37
5.2	Charge-sensitive amplifier layout. . . . .	38
5.3	Recycling folded cascode OTA layout. . . . .	38
5.4	Rail-to-rail operational amplifier layout. . . . .	39
5.5	Filter Layout. . . . .	39
5.6	Bode plot for the OTA open-loop response. . . . .	40
5.7	Weighting function test circuit. . . . .	40
5.8	SPICE-simulated weighting function. $\tau = 8 \text{ ns}$ , $N = 16$ and $T_s = 19.25 \text{ ns}$ . .	41
5.9	Filter output step response with the 64 programmable gains. $V_{in} = 0.1 \text{ V}$ and $T_s = 40 \text{ ns}$ . . . . .	41
5.10	Filter linearity test results, full-scale input range. . . . .	42
5.11	Filter control signals testing. $V_{in} = 0.1 \text{ V}$ and gain = $0.25 \text{ V/V}$ . . . . .	42
5.12	Bode plot for the buffer open-loop response. . . . .	43
A.1	The Bean 2 prototype bonding diagram. . . . .	49

## LIST OF TABLES

2.1	BeamCal instrumentation ASIC specifications summary. . . . .	8
2.2	Channel noise budget. . . . .	8
4.1	Filter specifications summary. . . . .	27
4.2	Filter OTA design values. . . . .	30
4.3	Rail-to-rail buffer main design values. . . . .	33
A.1	The Bean 2 prototype pinout . . . . .	48

## ABSTRACT

Particle Physics is the branch of physics that studies the fundamental constituents of matter and radiation, and their mutual interactions. The main tools used by particle physicists are particle accelerators, which uses electromagnetic fields to accelerate charged particles to relativistic speeds before they are made to collide inside detectors. The International Linear Collider (ILC), a next generation, 31-kilometer long linear particle accelerator, will smash electron and positron bunches at up to 500 GeV. Located at the ILC detector forward region, is the BeamCal, a highly segmented calorimeter detector. The BeamCal specifications for radiation tolerance, noise, signal charge, pulse rate and occupancy pose unique challenges for the instrumentation system.

Framed in the design, integration and testing of the Bean IC, a 5-channel application specific integrated circuit (ASIC) planned to meet the BeamCal instrumentation needs, this thesis presents: the development of a new mathematical framework for a design-oriented analysis of discrete-time filters in the discrete-time domain; and the design and implementation of a Switched Capacitor (SC) filter for arbitrary weighting function synthesis to be included in the Bean IC, which aims to take full advantage of the introduced mathematical framework.

**Keywords:** Charge Measurements, Low-noise filters, Noise, Nuclear Physics  
Instrumentation, Optimum Digital Filtering.

## RESUMEN

La Física de Partículas es la rama de la física que estudia las constituyentes fundamentales de la materia y la radiación, y sus interacciones mutuas. Las principales herramientas utilizadas por los físicos de partículas son los aceleradores de partículas, los cuales usan campos electromagnéticos para acelerar partículas cargadas a velocidades relativistas, para después hacerlas colisionar dentro de detectores. El Colisionador Lineal Internacional (ILC) es un acelerador de partículas lineal de la próxima generación de 31 kilómetros de largo que colisionará grupos de electrones y positrones a 500 GeV. Ubicado en la región delantera del ILC se encuentra el BeamCal, un detector calorímetro altamente segmentado. Las especificaciones del BeamCal para tolerancia a la radiación, ruido, señal de carga, tasa de pulsos y ocupación plantean desafíos únicos para el sistema de instrumentación.

Enmarcado en el diseño, integración y prueba de *Bean IC*, un circuito integrado de aplicación específica (ASIC, por sus siglas en inglés) de cinco canales para satisfacer las necesidades de instrumentación del BeamCal, esta tesis presenta: el desarrollo de un nuevo marco matemático para el análisis orientado al diseño de filtros de tiempo discreto; y el diseño y implementación de un filtro de Capacitores Comutados para la síntesis de funciones de peso arbitraria que sera incluido en *Bean IC*, el cual busca aprovechar al máximo el marco matemático propuesto.

**Palabras Claves:** Medición de carga, Filtros de Bajo Ruido, Ruido, Instrumentación para Física Nuclear, Filtración Digital Optima

# 1. INTRODUCTION

## 1.1 Particle physics experiments

Particle physics, also called High Energy Physics, is the branch of physics that studies the fundamental constituents of matter and radiation, and their mutual interactions. It aims to answer some of the profound questions of physics, with benefits spanning everything from advancing humankind's understanding of the universe, to applications in other fields of science as well as daily life (Tuttle, 2013).

The main tools used by experimental particle physicists are particle accelerators, which uses electromagnetic fields to accelerate charged particles to relativistic speeds before they are made to collide inside detectors. The detectors gather clues about the particles – including their speed, mass and charge – from which physicists can work out a particle's identity (CERN, 2013). An example of such an accelerators is the Large Hadron Collider (LHC) at *Organisation européenne pour la recherche nucléaire* (CERN), which recently proves the existence of the Higgs field (Aad et al., 2012; Chatrchyan et al., 2012), a key element to complete the Standard Model and one of the greatest scientific achievements of the past 50 years.

Because experimenters seek ever-increasing high-energy collisions to make new discoveries, and because there are greatest discoveries yet to be made, new and larger particle accelerators appears in the roadmap of the scientific community. Up to date, there are two projects in the race to define the LHC's successor, the International Linear Collider (ILC) and the Compact Linear Collider (CLIC), both coordinate by the Linear Collider Collaboration.

As the collision energy increases with each new accelerators generation, so does the complexity of the detectors used to gather information about the collisions. This make it

---

This work was supported by the National Commission for Scientific and Technological Research (CONICYT) of Chile, under grant FONDECYT 11110165 and scholarship CONICYT-PCHA/Magíster Nacional/2013 - folio 221320673.

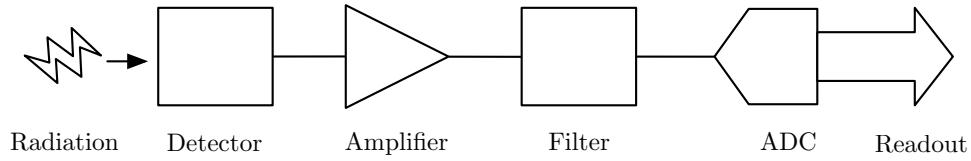


FIGURE 1.1. Block diagram for a single channel, generic instrumentation circuit for particle physics experiments.

necessary a continuous improvement of the techniques used in instrumentation for particle physics, an example of this is the introduction of the CMOS technology in the early 80's, which changed the trend of detector front-end electronics from printed circuit boards (PCBs) to custom integrated circuits, improving integration and allowing on-site electronics with a minimum of mass added to the detector system (Abusleme, 2011).

This thesis deal with an emerging trend to improve the electronics used in particle physics, the use of discrete-time filters to lower the noise present in the detectors front-end circuits. A new mathematical framework for noise analysis of discrete-time filter is presented, in an attempt to guide a proper filter design when a discrete-time filter is used for pulse-processing purposes. Additionally, the design and characterization of a front-end filter for one of the detectors planned for the ILC is presented.

In this chapter, a typical front-end circuit for a detector system is described. Then, current trends in noise minimization in front-end electronics for particle physics experiments are reviewed. Finally, a brief outline of this thesis is presented.

## 1.2 Electronics for particle physics experiments

A typical particle physics experiment detector system contains different layers of detectors, each of which is usually highly segmented into a multichannel array. A single channel of a certain layer includes a detector, an amplifier, a filter, an analog-to-digital converter (ADC), and a readout circuit (Spieler, 2005). Fig. 1.1 shows a highly simplified block diagram for a generic detector channel.

The initial amplifier translates the input charge signal, coming from the detector electrodes, into an output voltage signal. Charge-to-voltage translation is done by transferring the charge  $Q_{in}$  from the nonlinear detector capacitance to a linear, known capacitor  $C$ . The generated voltage  $V_{out}$  is simply given by  $V_{out} = Q_{in}/C$ , with  $C$  easily and precisely tailorable. Fig. 1.2 depict the most common preamplifier implementation, which consists of a voltage amplifier with a capacitor in negative feedback configuration. The resulting feedback circuit is a charge-sensitive amplifier (CSA), extensively studied in the literature (Alvarez, Avila, Campillo, Dragone, & Abusleme, 2012; Aspell et al., 2001; De Geronimo & O'Connor, 2005; O'Connor & De Geronimo, 1999; Snoeys, Campbell, Heijne, & Marchioro, 2000). The amplified detector signal includes noise from the detector and the amplifier. Since the noise statistics are well modeled, they can be used to design a filter that maximizes the signal-to-noise ratio (SNR) at the detector front-end. Usually the filter is an analog block, either time-invariant or time-varying, used to convert the voltage signal at the CSA output into a shaped voltage pulse. The pulse shape defines the weights of white series, white parallel and flicker series noise sources on the front-end output noise, thus a proper selection of the pulse shape form part of the solution to the SNR maximization problem. A memory acts as a buffer necessary to store data for a number of events before readout. For high-frequency pulse trains, analog memory is particularly well suited (Haller & Wooley, 1994; Kleinfelder, Chen, Kwiatkowski, & Shah, 2004). Filtered signals can be quickly stored as charge in integrated capacitors, to be converted into digital signals by dedicated ADCs during the readout phase. Integration and feature size reduction has allowed the design of highly dense digital memory arrays. If a digital memory is used instead, ADCs are used to digitize the signal prior to storage, and conversion throughput per IC must be as high as the collision rate times the number of channels.

### 1.3 Noise minimization in circuits for particle physics instrumentation

Noise minimization in particle physics experiments is done by a careful design of the channel, and specifically, on the detector, CSA and filter parameters. Understanding and designing for low noise has been one of the main concerns in modern particle physics

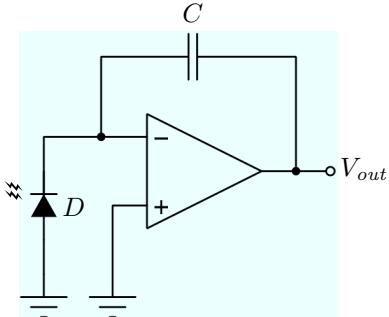


FIGURE 1.2. CSA using a voltage amplifier. Detector is modeled as a photodiode.

instrumentation. Any survey on this topic starts with a work published in 1968 (Radeka, 1968), where important concepts of pulse shaping for particle physics experiments were described. At this time, the search of practical optimum shapers and simpler analysis methods were the main concerns. The concept of a weighting function, equivalent to impulse response, but valid for time-varying systems as well, was introduced.

In 1972, a powerful time-domain analysis technique was published (Goulding, 1972), for comparing the filtering effects of different pulse shapers. Starting from a physical approach and assuming only white noise, it was shown that all the noise sources in a front-end for particle physics experiments can be reduced to two components at the input node: step (parallel) noise and delta (series) noise. Integration of each component in frequency yields two noise coefficients that make it possible to characterize the noise-filtering capabilities of a pulse shaper, independently of the time scale. These ideas are still in use today.

In 1984, a good review and some examples of readout electronics techniques for semiconductor detectors in particle physics instrumentation systems was published (Gatti & Manfredi, 1984). The author emphasized the importance of the input stage of the front-end electronics in the overall noise performance. By that time, there was already some interest in MOS technology (with lower performance than JFETs or MESFETs) due to the potential of integrating the semiconductor detector and its electronics. In the same year, a good summary of semiconductor position-sensitive detectors was also published (Radeka,

1984). It was shown that the minimum noise is achieved when the detector and amplifier input capacitances are matched.

In 1988, one of the most influential papers in low-noise techniques for particle physics instrumentation was published (Radeka, 1988). In this paper, the results from previous works on noise were summarized.

Flicker noise research in particle physics electronics was published in 1989 (Lutz, Manfredi, Re, & Speziali, 1989). Before this paper, flicker noise was rarely mentioned and seldom considered in analysis equations for particle physics electronics. In 1990, the issue of optimum shapers for particle physics electronics, including low frequency noise in the analysis, was published (Gatti, Sampietro, & Manfredi, 1990). The same year, an excellent derivation of noise for particle physics front-end electronics, including thermal, flicker and shot noise sources was presented (Sansen & Chang, 1990).

In 1992 (Gadomski et al., 1992), the deconvolution method for pulse-shaping was presented. Major innovations of this work come from the use of switched-capacitor filters for pulse-processing purposes and the introduction of the concept of discrete-time pulse-shaping.

In 1998 (Pullia, 1998), for the first time the contribution of the low-frequency noise is computed in the time domain, using fractional derivatives. It is an extension of earlier noise computation methods (Goulding, 1972). A generalization of this work was presented in 2004 (Pullia & Riboldi, 2004), allowing time-domain simulations of almost all kind of noise sources. A powerful tool for computer-aided filter design.

Finally, excellent books on particle physics instrumentation systems have been published (Radeka, 2011), compiling and explaining the results from many papers in the field.

## 1.4 Thesis content

Chapter 2 starts with an introduction to the project that prompt the work of this thesis, the design and implementation of a second iteration of The Bean, an instrumentation

application-specific integrated circuit (ASIC) which forms part of the proposal for the ILC. It is followed by an overview of the motivations that lead to the development of a new mathematical framework for noise analysis in discrete-time filters, alongside with the presentation of the requirements for a filter intended to take full advantage of this framework. Chapter 3 presents the complete formulation of this noise analysis, including examples and applications for optimal filter computation. In Chapter 4 , the design and implementation of a filter for arbitrary weighting function synthesis are presented. Chapter 5 shows the results that contribute to the ongoing project, functionality verifications of the designed filter and the implementation of an early prototype of The Bean 2, with the filter as one of its core building blocks. Finally, Chapter 6 summarizes the results and contributions of this work, and presents ideas for future research.

## 2. PROBLEM DEFINITION

### 2.1 The International Linear Collider

The work described in this thesis form part of the design and implementation of the front-end circuit for one of the detector systems of the International Linear Collider (ILC).

Planned to be operating in the mid 2020's, the ILC will be the largest linear collider ever built. Consisting of two linear accelerators that will stretch approximately 32 kilometers in length, the ILC will smash electrons and positrons together at nearly the speed of light. The intended beam collision energy is 500 billion-electron-volts (GeV) for the first stage, with the possibility for a later upgrade to 1 TeV.

Superconducting accelerator cavities operating at temperatures near absolute zero give the particles more and more energy until they smash in centre of the machine, where a bunch of detectors gather clues about the particles identity .

Located at the ILC detector forward region, the BeamCal is a highly segmented ( $> 90000$  channels) calorimeter that will serve three main purposes: improve the hermeticity of the ILC detector for low polar angles, reduce the backscattering from pairs into the inner ILC detector part and protect the final magnet of the beam delivery system, and assist the beam diagnostics. The BeamCal specifications for radiation tolerance, noise, signal charge, pulse rate and occupancy pose unique challenges for the instrumentation system.

The project FONDECYT 11110165: Application of Advanced CMOS Techniques in Pulse Processors for Particle Physics Experiments deals with the design and implementation of a mixed-signal integrated circuit (IC) to address the BeamCal instrumentation needs.

Input rate	3.25 MHz during 0.87 ms, repeated every 200 ms
Channels per ASIC	32
Occupancy	100%
Resolution	10 bits for individual channels, 8 bits for fast feedback
Modes of operation	Standard data taking (SDT), Detector Calibration (DCal)
Input signals	4 fC - 40 pC in SDT, 0.74 pC in DCal
Input capacitance	65 pF
Additional feature	Low-latency ( $1\ \mu\text{s}$ ) output
Additional feature	Internal pulser for electronics calibration
Radiation tolerance	1 Mrad ( $\text{SiO}_2$ ) total ionizing dose
Power consumption	2.19 mW per channel
Total ASIC count	2836

TABLE 2.1. BeamCal instrumentation ASIC specifications summary.

Noise source	Noise power budget
CSA	$1 \times Q_n^2$
Filter $kT/C$	$1 \times Q_n^2$
Filter amplifier	$0.25 \times Q_n^2$
Buffers	$0.25 \times Q_n^2$
ADC	$0.25 \times Q_n^2$
Total	$2.75 \times Q_n^2$

TABLE 2.2. Channel noise budget.

## 2.2 The Bean

The Bean – BeamCal Instrumentation IC – is a 32-channel front-end and readout ASIC that will address the BeamCal instrumentation requirements. By employing a charge-sensitive amplifier and a switched-capacitor filter, the Bean will process the input charge signals at the ILC pulse rate. Each channel will have a 10-bit successive approximation register analog-to-digital converter and digital memory for readout purposes. The Bean will also feature a fast feedback adder, capable of providing an 8-bit, low-latency output for beam diagnostics purposes.

### **3. NOISE ANALYSIS IN PULSE-PROCESSING DISCRETE-TIME FILTERS<sup>1</sup>**

#### **3.1 Introduction**

In particle physics experiments, where the results from the collisions are inferred from the measurement of electric charge in various sets of detectors (Gatti & Manfredi, 1986; Radeka, 1988), noise sets a fundamental limit for the charge measurement resolution (Geronimo, O'Connor, Radeka, & Yu, 2001). In such experiments, the typical detector front-end circuit comprises a charge-sensitive amplifier (CSA) and a filter, often referred to as pulse shaper. The former is used to convert the input charge signal, coming from the detector electrodes, into a voltage signal, and is responsible for most of the noise present in the readout circuit signal path (De Geronimo & O'Connor, 2005; Geronimo et al., 2001). The filter is used to convert the voltage signal at the CSA output into a shaped voltage pulse, in order to maximize the signal-to-noise ratio (SNR) at the measurement time.

Different noise analysis methods have been proposed to guide a proper filter design. The outcome of these methods is the equivalent noise charge (*ENC*), a measure of the front-end noise defined as the charge required at the detector input to produce an output SNR of 1. A time-domain analysis based on the weighting function (WF) concept (Goulding, 1972; Radeka, 1988) has long been the preferred analysis, since it allows to find the optimum filter for a wide range of detector configurations (Gatti, Geraci, & Ripamonti, 1996; Geraci & Gatti, 1995; Pullia, 1997; Pullia & Gatti, 2002; Radeka, 1968).

Traditionally, the filter synthesis has been performed using continuous-time networks. However, since producing arbitrary WFs by means of continuous-time analog circuitry is often impossible (Gatti et al., 1996), this approach does not always allow to synthesize optimum filters. A different approach based on discrete-time filters, implemented by means of digital signal processor (DSP) units (Geraci, Zambusi, & Ripamonti, 1996;

---

<sup>1</sup>See also (Avila, Alvarez, & Abusleme, 2013)

Jordanov, 2003; Sampietro, Bertuccio, Geraci, & Fazzi, 1995) or switched capacitor networks (Abusleme, Dragone, Haller, & Wooley, 2012; Fiorini & Buttler, 2002; Porro, Herrmann, & Hornel, 2007), allows to synthesize WFs with virtually any shape, producing near-optimum filters. Moreover, this promising approach takes advantage of the aggressive technology scaling and the new techniques of the VLSI industry, allowing to implement fast, reliable and flexible filters.

In this work, a mathematical framework for a design-oriented analysis of discrete-time filters in the discrete-time domain is presented. Although discrete-time filters can be analyzed using a continuous-time method, it is not insightful and the resulting expressions are complex and difficult to use for design purposes. Furthermore, the analysis of discrete-time filters in the discrete-time domain provides a better insight on how their discrete nature affects the front-end noise. The proposed analysis can produce closed-form expressions for the *ENC* calculation, which can be used for efficient algorithms for the *ENC* evaluation and filter optimization procedures.

In order to validate the proposed framework in this work, an example is developed, and the result obtained is analyzed and compared with the result provided by the continuous-time approach. Also, an example of optimal filter computation is presented to demonstrate the capabilities of the proposed framework.

### 3.2 Discrete-Time Analysis

Figure 3.1 shows a simplified model to compute the output-referred noise contribution of a single noise source in a typical front-end detector. It consists of a linear block with a transfer function  $H(s)$  that models the effect of the CSA on the noise source under analysis, and a pulse shaper, which in this case is a finite impulse response (FIR) filter with a discrete-time transfer function given by

$$F(z) = \sum_{j=0}^{N-1} a_{N-j} z^{-j} \quad (3.1)$$

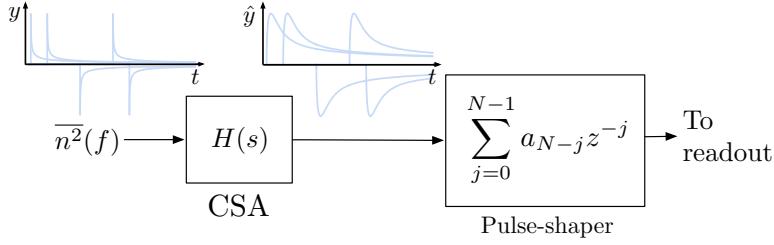


FIGURE 3.1. Model for noise analysis in a typical front-end circuit.

where  $a_{N-j}$  are arbitrary coefficients and  $N$  is the filter length. The noise source is characterized by its two-sided power spectral density (PSD)  $\overline{n^2}(f)$ .

For this analysis it is not necessary to consider the details of the physical processes that cause the noise. It will be assumed that the noise source is an arbitrary white or filtered white noise source, which represents any of the fundamental noise sources present at a detector front-end circuit, such as thermal noise, shot noise and flicker noise. This assumption allows to model the noise source in the time domain in terms of a sequence of noise pulses with core function  $y(t)$ , arriving Poissonianly at times  $t_a$  with an average rate  $\nu$  and random sign (Goulding, 1972; Radeka, 1988). A general procedure to calculate a function  $y(t)$  that represents the noise process characterized by  $\overline{n^2}(f)$  can be found in (Pullia & Riboldi, 2004).

By using the CSA transfer function and  $y(t)$ , the effect of an individual noise pulse at the filter input can be determined as

$$\hat{y}(t) = y(t) * \mathcal{L}^{-1}\{H(s)\}(t). \quad (3.2)$$

Both sequences of pulses, at the input and at the output of  $H(s)$ , are illustrated in Figure 3.1.

Assuming a periodic, synchronous front-end, where the stimulus arrival time within each frame is fixed and known, the CSA can be reset at the beginning of each frame, prior to the corresponding stimulus. Thus, the analysis can be carried out considering a non-stationary noise process that starts at  $t = 0$ . Then the total integrated noise at the filter input is a function of time (Radeka, 2011). Using (3.2) and Campbell's theorem, the

following expression for the total integrated noise at the filter input can be derived:

$$\sigma^2(t) = \nu \int_0^t \hat{y}^2(t - t_a) dt_a. \quad (3.3)$$

Let us define  $P_i$  as the time interval between an arbitrary sample  $i$  and its predecessor, given by  $P_i = [(i-1)T_s, iT_s]$ , where  $T_s$  is the filter sampling period. Now consider the noise contribution of the pulses originated within  $P_i$  and measured at an arbitrary sample  $k$  (i.e.,  $t = kT_s$ ),  $\sigma_i^2(k)$ , as shown in Figure 3.2. Using Campbell's theorem,  $\sigma_i^2(k)$  can be computed as

$$\sigma_i^2(k) = \nu \int_{(i-1)T_s}^{iT_s} \hat{y}^2(kT_s - t_a) dt_a. \quad (3.4)$$

It can be shown that (3.4), can be expressed as

$$\sigma_i^2(k) = \int_0^{T_s} \hat{y}^2((k-i+1)T_s - \eta_1) d\eta_1 \quad (3.5)$$

where  $\eta_1 = t_a + T_s - iT_s$ . This integral can be split into two integrals as follows

$$\begin{aligned} \sigma_i^2(k) &= \int_0^{(k-i+1)T_s} \hat{y}^2((k-i+1)T_s - \eta_1) d\eta_1 \\ &\quad - \int_{T_s}^{(k-i+1)T_s} \hat{y}^2((k-i+1)T_s - \eta_2) d\eta_2. \end{aligned} \quad (3.6)$$

Defining  $\eta_2 = \eta_3 + T_s$ , (3.6) can be written as

$$\begin{aligned} \sigma_i^2(k) &= \int_0^{(k-i+1)T_s} \hat{y}^2((k-i+1)T_s - \eta_1) d\eta_1 \\ &\quad - \int_0^{(k-i)T_s} \hat{y}^2((k-i)T_s - \eta_3) d\eta_3. \end{aligned} \quad (3.7)$$

Since  $\hat{y}^2(t)$  is zero for negative arguments, then  $\sigma_i^2(k) = 0$  for  $k < i$ . For  $k \geq i$ , and according to (3.3), (3.7) can be alternatively expressed as

$$\sigma_i^2(k) = \sigma^2((k-i+1)T_s) - \sigma^2((k-i)T_s) \quad (3.8)$$

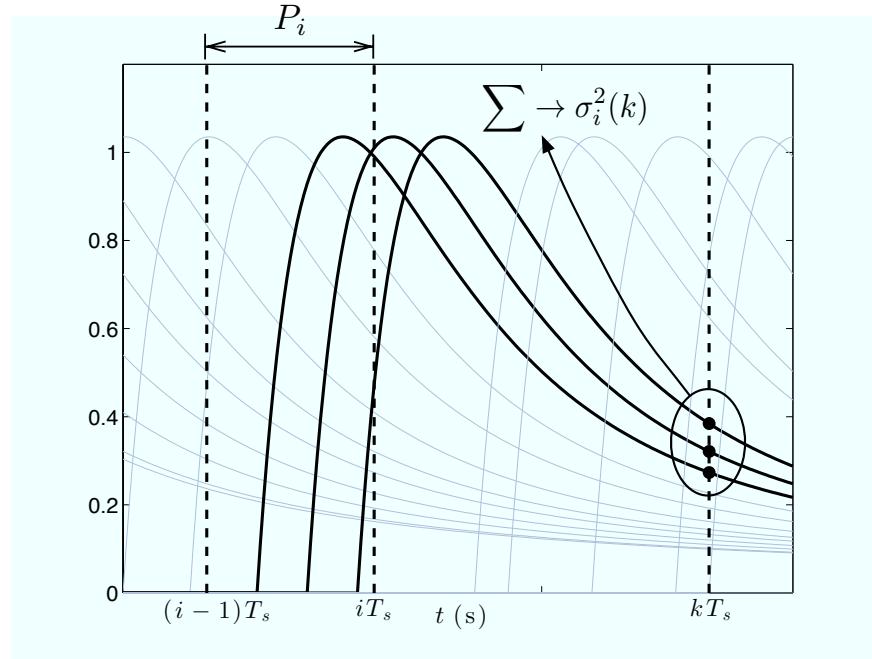


FIGURE 3.2. Noise contribution of the pulses generated within  $P_i$  and measured at an arbitrary sample  $k$  (i.e.,  $t = kT_s$ ), using an arbitrary filtered noise core function  $\hat{y}(t)$ . The independent contribution of each pulse is pointed out with black dots.

therefore

$$\sigma_i^2(k) = \begin{cases} \sigma^2((k-i+1)T_s) - \sigma^2((k-i)T_s), & k \geq i \\ 0, & k < i. \end{cases} \quad (3.9)$$

Based on (3.9), the total integrated noise at the filter input measured at the  $k$ -th sample,  $\sigma^2(kT_s)$ , can be written as the sum of the individual noise contributions originated at each interval  $P_i$ :

$$\sigma^2(kT_s) = \sum_{i=1}^N \sigma_i^2(k). \quad (3.10)$$

The evolution of the total integrated noise at the filter input according to (3.10) is illustrated in Figure 3.3.

Since (3.10) is composed by noise contributions originated at different time intervals  $P_i$ , the total integrated noise at the filter input holds partial correlation between samples, and the output noise cannot be computed by convolving (3.10) with  $F(z)$ . However, since all evaluations of  $\sigma_i^2(k)$  are originated from the same pulses (for a fixed  $i$ ), and thus are fully correlated, (3.10) can be split into  $N$  independent discrete-time signals  $\sigma_1^2(k), \sigma_2^2(k) \dots \sigma_N^2(k)$ . Each of these signals can be referred to the filter output as

$$\begin{aligned}\hat{\sigma}_i(k) &= \sqrt{\sigma_i^2(k)} * \mathcal{Z}^{-1}\{F(z)\}(k) \\ &= \sum_{j=0}^{k-i} a_{N-j} \sqrt{\sigma_i^2(k-j)}.\end{aligned}\quad (3.11)$$

Signals  $\hat{\sigma}_1(k), \hat{\sigma}_2(k) \dots \hat{\sigma}_N(k)$  are also independent, and can be added up as noise variances to compute the total integrated noise at the filter output as a function of  $k$ :

$$\begin{aligned}\hat{\sigma}^2(k) &= \sum_{i=1}^k \hat{\sigma}_i^2(k) \\ &= \sum_{i=1}^k \left( \sum_{j=0}^{k-i} a_{N-j} \sqrt{\sigma_i^2(k-j)} \right)^2.\end{aligned}\quad (3.12)$$

Evaluating (3.12) at the measurement time  $t_m = NT_s$  (i.e.,  $k = N$ ) yields

$$\hat{\sigma}^2(N) = \sum_{i=1}^N \left( \sum_{j=0}^{N-i} a_{N-j} \sqrt{\sigma_i^2(N-j)} \right)^2.\quad (3.13)$$

Finally, replacing (3.9) in (3.13) and defining  $h = N - j - i$ , a closed-form expression for the front-end noise can be obtained:

$$\hat{\sigma}^2(N) = \sum_{i=1}^N \left( \sum_{h=0}^{N-i} a_{i+h} \sqrt{\sigma^2((h+1)T_s) - \sigma^2(hT_s)} \right)^2.\quad (3.14)$$

The only term of (3.14) that depends on the input-referred noise process is  $\sigma^2(t)$ , which can be calculated analytically or numerically for typical noise processes by using (3.3). For instance, Figure 3.4 illustrates  $\sigma^2(t)$  for thermal, shot and flicker noise. Even

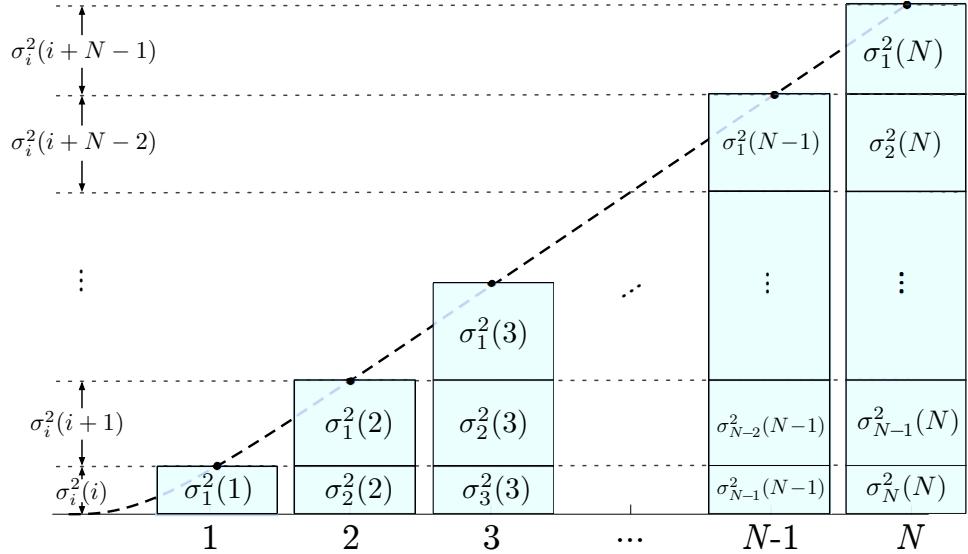


FIGURE 3.3. Evolution of the total integrated noise at the filter input, where the noise of each sample was split according to (3.10).

though the analysis presented here has been applied for a single noise source, it can be easily extended for circuits with several noise sources by applying the superposition principle in quadrature.

### 3.3 Example

For validation purposes, the thermal noise contribution at the output of a discrete-time integrator filter will be computed using the proposed discrete-time analysis. The result obtained will be analyzed and then compared with the result produced by the traditional continuous-time approach. Figure 3.5 shows the front-end circuit used for general noise analysis. The detector is modeled as capacitance  $C_D$ , whereas the CSA is shown as a voltage amplifier with open loop gain  $A(s) = A/(1 + s\tau)$ , input capacitance  $C_{in}$  and a feedback capacitor  $C_F$ . Resistor  $R_R$  across the feedback capacitor  $C_F$  represents the CSA reset element. The filter coefficients are  $a_i = 1$ . The detector shot noise represented by  $\overline{i_D^2}$  will be omitted for the purpose of this example. Thermal noise has been assumed to be dominated by the CSA input device and is represented by two fully-correlated noise

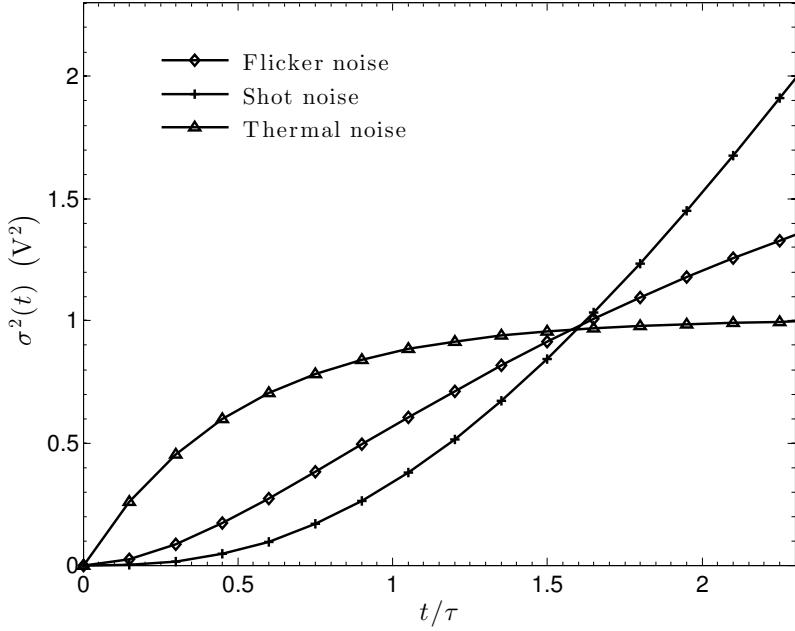


FIGURE 3.4.  $\sigma^2(t)$  for thermal, shot and flicker noise with normalized time  $t/\tau$  and an arbitrary amplitude.

sources (Sansen & Chang, 1990), a voltage white noise source with a two-sided PSD  $\overline{v_n^2}$  and a current noise source with a two-sided PSD  $\overline{i_n^2}$ . Both noise sources are related as follows:

$$\overline{i_n^2} = (sC_{in})^2 \overline{v_n^2}. \quad (3.15)$$

Considering that the effect of the reset switch during the relatively short time that it takes the CSA to produce an output voltage is negligible,  $R_R$  can be assumed to be infinite (Pullia & Riboldi, 2004). The CSA open loop DC gain ( $A$ ) is assumed to be very large as well. Under these assumptions and using (3.15), the PSD of the thermal noise referred to the CSA output,  $\overline{v_o^2}$ , can be approximated to

$$\overline{v_o^2} \approx \left| \frac{C_{tot}}{C_f} \frac{1}{1 + s\hat{\tau}} \right|^2 \overline{v_n^2} \quad (3.16)$$

where  $C_{tot} = C_D + C_F + C_{in}$  and  $\hat{\tau} = (\tau/A)(C_{tot}/C_f)$  is the CSA closed-loop time-constant.

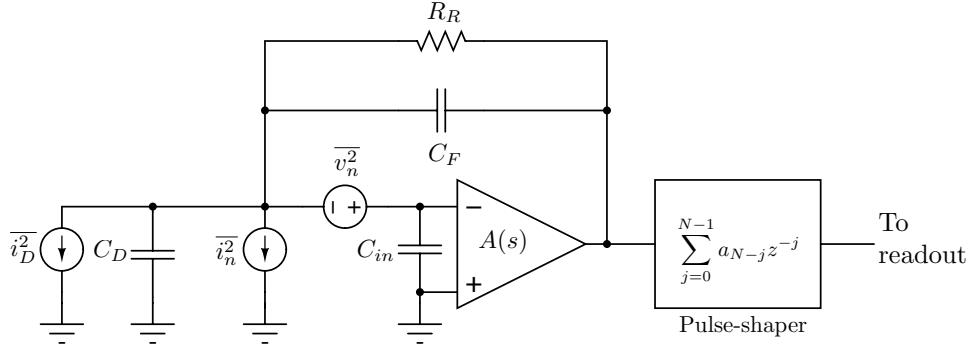


FIGURE 3.5. Front-end circuit used for noise analysis.

The PSD in (3.16) can be treated as the result of passing a fictitious noise source with PSD  $\bar{v_n^2}$  through a block with transfer function  $H_{\text{th}}(s)$  given by

$$H_{\text{th}}(s) = \frac{C_{\text{tot}}}{C_f} \frac{1}{1 + s\hat{\tau}}. \quad (3.17)$$

Since  $\bar{v_n^2}$  characterizes a white noise source, it can be modeled as a sequence of Dirac impulses with core function  $y_{\text{th}}(t)$  occurring at an arbitrary rate  $\nu$  and random sign (Pullia & Riboldi, 2004), where  $y_{\text{th}}(t)$  is given by

$$y_{\text{th}}(t) = \sqrt{\frac{\bar{v_n^2}}{\nu}} \delta(t). \quad (3.18)$$

Replacing (3.17) and (3.18) in (3.2), each pulse in the sequence can be referred to the CSA output as an exponentially decaying pulse (Pullia & Riboldi, 2004) as follows

$$\hat{y}_{\text{th}}(t - t_a) = \sqrt{\frac{\bar{v_n^2}}{\nu} \frac{C_{\text{tot}}}{C_F}} \frac{e^{-(t-t_a)/\hat{\tau}}}{\hat{\tau}} u(t - t_a) \quad (3.19)$$

where  $u(t)$  is the unit step function. Substituting (3.19) in (3.3), the filter input total integrated noise due to the thermal noise,  $\sigma_{\text{th}}^2(t)$ , can be derived:

$$\sigma_{\text{th}}^2(t) = \bar{v_n^2} \frac{C_{\text{tot}}^2}{C_F^2} \frac{1 - e^{-2t/\hat{\tau}}}{2\hat{\tau}} u(t). \quad (3.20)$$

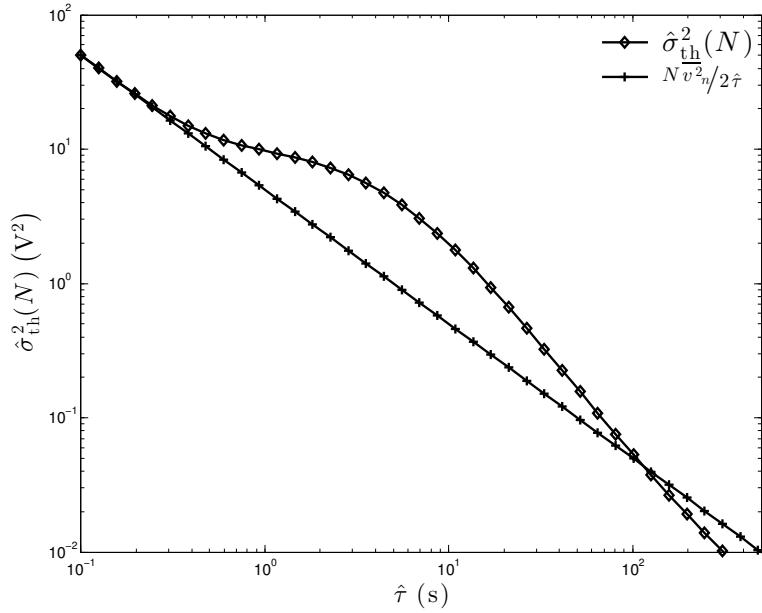


FIGURE 3.6.  $\hat{\sigma}_{th}^2(N)$  and  $N \frac{\bar{v}_n^2}{2\hat{\tau}} \frac{C_{tot}^2}{C_F^2}$  as a function of  $\hat{\tau}$ , using  $\bar{v}_n^2 = 1$ ,  $C_{tot}^2/C_F^2 = 1$  and  $N = 20$ .

Finally, replacing (3.20) in (3.14) and defining  $x = e^{T_s/\hat{\tau}}$ , the front-end noise,  $\hat{\sigma}_{th}^2(N)$ , can be obtained:

$$\hat{\sigma}_{th}^2(N) = \frac{\bar{v}_n^2 C_{tot}^2}{2\hat{\tau} C_F^2} \frac{(N(x^2 - 1) - 2x - x^{-2N} + 2x^{-N} + 2x^{1-N} - 1)}{(x - 1)^2}. \quad (3.21)$$

When the time interval between samples is large enough to consider that consecutive noise samples are uncorrelated (i.e.,  $\hat{\tau} \ll T_s$ ),  $\hat{\sigma}_{th}^2(N)$  can be approximated without the use of the proposed analysis as a weighted sum of the uncorrelated samples of the total integrated noise at the CSA output as follows:

$$\hat{\sigma}_{th}^2(N) \Big|_{\hat{\tau} \ll T_s} \approx N \lim_{t \rightarrow \infty} \sigma^2(t) = N \frac{\bar{v}_n^2}{2\hat{\tau}} \frac{C_{tot}^2}{C_F^2}. \quad (3.22)$$

As shown in Figure 3.6, (3.21) behaves as predicted by (3.22) for small values of  $\hat{\tau}$ .

Now, the same example will be analyzed using the traditional continuous-time approach. Using (3.19), the WF  $w(t)$ , defined as the contribution of each pulse occurring at

time  $t$  measured at a fixed time  $t_m = NT_s$  at the output of the filter, is given by

$$\begin{aligned} w(t) &= \sum_{n=1}^N \hat{y}_{\text{th}}(nT_s - t) \\ &= \sqrt{\frac{v_n^2}{\nu} \frac{C_{\text{tot}}}{C_F}} \sum_{n=1}^N \frac{e^{-(nT_s - t)/\hat{\tau}}}{\hat{\tau}} u(nT_s - t). \end{aligned} \quad (3.23)$$

Integrating (3.23) from the reset time ( $t = 0$ ) to the signal measurement time ( $t = t_m$ ), the filter total integrated noise at  $t = t_m$  can be computed as

$$\begin{aligned} \hat{\sigma}_{\text{th}}^2(N) &= \nu \int_0^{t_m} w^2(t) dt \\ &= \frac{v_n^2}{\nu} \frac{C_{\text{tot}}^2}{C_F^2} \int_0^{NT_s} \left( \sum_{n=1}^N \frac{e^{-(nT_s - t)/\hat{\tau}}}{\hat{\tau}} u(nT_s - t) \right)^2 dt. \end{aligned} \quad (3.24)$$

Defining  $\alpha = T_s/\hat{\tau}$  and  $\beta = t/\hat{\tau}$ , (3.24) can be re-written as

$$\hat{\sigma}_{\text{th}}^2(N) = \frac{\overline{v_n^2}}{\hat{\tau}} \frac{C_{\text{tot}}^2}{C_F^2} \int_0^{N\alpha} e^{2\beta} \left( \sum_{n=1}^N e^{-n\alpha} u(n\alpha - \beta) \right)^2 d\beta \quad (3.25)$$

which can be split into a sum of integrals as follows

$$\hat{\sigma}_{\text{th}}^2(N) = \frac{\overline{v_n^2}}{\hat{\tau}} \frac{C_{\text{tot}}^2}{C_F^2} \sum_{n=1}^N \int_{(n-1)\alpha}^{n\alpha} e^{2\beta} \left( \sum_{k=n}^N e^{-k\alpha} \right)^2 d\beta. \quad (3.26)$$

Finally, defining  $x = e^\alpha$  it can be shown that (3.26) is equal to (3.21).

### 3.4 ENC Minimization

For filter optimization purposes, a typical front-end circuit with thermal, shot and flicker noise components is considered. The front-end configuration from Figure 3.5 will be used. In this case, the pulse shaper is a discrete-time FIR filter with indeterminate coefficients  $a_i$ . Shot noise is assumed to be dominated by the detector noise and is represented by a white noise current source with two-sided PSD  $\overline{i_D^2}$  in parallel with the detector capacitance  $C_D$  and given by

$$\overline{i_D^2} = qI_L \quad (3.27)$$

where  $q$  is the electron charge and  $I_L$  the detector leakage current. Thermal noise and flicker noise are assumed to be dominated by the noise of the CSA input device and are represented by two fully-correlated noise sources, a voltage noise source with two-sided PSD  $\overline{v_n^2}$  given by

$$\overline{v_n^2} = a_T + \frac{a_F}{|f|} \quad (3.28)$$

where  $a_T$  and  $a_F$  are the thermal and flicker coefficients, and a current noise source with two-side PSD  $\overline{i_n^2}$  given by (3.15). Traditionally, the coefficients  $a_T$  and  $a_F$  are obtained from the CSA input device models. However, for design purposes the most accurate values shall be used, and these coefficients should be extracted from experiments (Bertuccio & Pullia, 1993) or precise simulations.

Considering the contribution of each noise process separately, the  $ENC^2$  for the output measured at  $t = NT_s$  can be written as

$$ENC^2 = \frac{\hat{\sigma}_{\text{shot}}^2(N) + \hat{\sigma}_{\text{th}}^2(N) + \hat{\sigma}_{1/f}^2(N)}{q^2 |\max[w(t)]|^2 / C_F^2} \quad (3.29)$$

where  $\hat{\sigma}_{\text{shot}}^2(N)$  is the shot noise contribution,  $\hat{\sigma}_{\text{th}}^2(N)$  is the thermal noise contribution,  $\hat{\sigma}_{1/f}^2(N)$  is the flicker noise contribution and  $w(t)$  is the weighting function at the front-end output given by (3.23).

In order to find the coefficients  $a_i$  that minimize (3.29), and hence the optimal FIR filter, the signal measurement time  $t_m = NT_s$  was assumed to be a constant determined by the processing time budget constraints, and the filter sampling period  $T_s$  was assumed to be a constant determined by the filter maximum clock rate. Although  $\hat{\tau}$  is a design variable that depends on the CSA and not on the filter, it has been included in the optimization analysis.

Given that a common WF reaches its maximum value at  $t = t_m/2$ , and that the WF height is commonly a design constraint, the denominator of (3.29) was forced to be constant by fixing the WF height,  $h_w$ , through the following constraints

$$\sum_{i=1}^{N/2} a_i \left(1 - e^{-T_s(N/2-i+1)/\hat{\tau}}\right) = h_w \quad (3.30)$$

$$\sum_{i=1}^N a_i \left(1 - e^{-T_s(N-i+1)/\hat{\tau}}\right) = 0. \quad (3.31)$$

Although these constraints appear from foreknowledge about the shape of the optimum WF, the actual computation of  $w(t)$  was never required for the optimization problem formulation. For illustration purposes, the length of the filter  $N$  was assumed to be an even number. Considering these constraints, minimizing the  $ENC^2$  is equivalent to minimizing its numerator, and according to (3.14), the resulting objective function  $f_o$  is given by

$$f_o = \sum_{i=1}^N \left\{ \left( \sum_{h=0}^{N-i} a_{i+h} \sqrt{\sigma_{\text{shot}}^2((h+1)T_s) - \sigma_{\text{shot}}^2(hT_s)} \right)^2 + \left( \sum_{h=0}^{N-i} a_{i+h} \sqrt{\sigma_{\text{th}}^2((h+1)T_s) - \sigma_{\text{th}}^2(hT_s)} \right)^2 + \left( \sum_{h=0}^{N-i} a_{i+h} \sqrt{\sigma_{1/f}^2((h+1)T_s) - \sigma_{1/f}^2(hT_s)} \right)^2 \right\}. \quad (3.32)$$

To obtain a numerical solution for the optimization problem, given by the objective function (3.32) and constraints (3.30) and (3.31), the parameters of an HPGe segmented detector with an input FET transistor were considered. Assuming that the input device is in strong inversion, the coefficient  $a_T$  can be calculated as

$$a_T = \frac{2KT\gamma}{g_m} \quad (3.33)$$

where  $K$  is the Boltzmann constant,  $T$  is the absolute temperature,  $g_m$  is the transconductance of the input device and  $\gamma$  is a constant factor, typically  $\approx 2/3$  (Van Der Ziel, 1970).

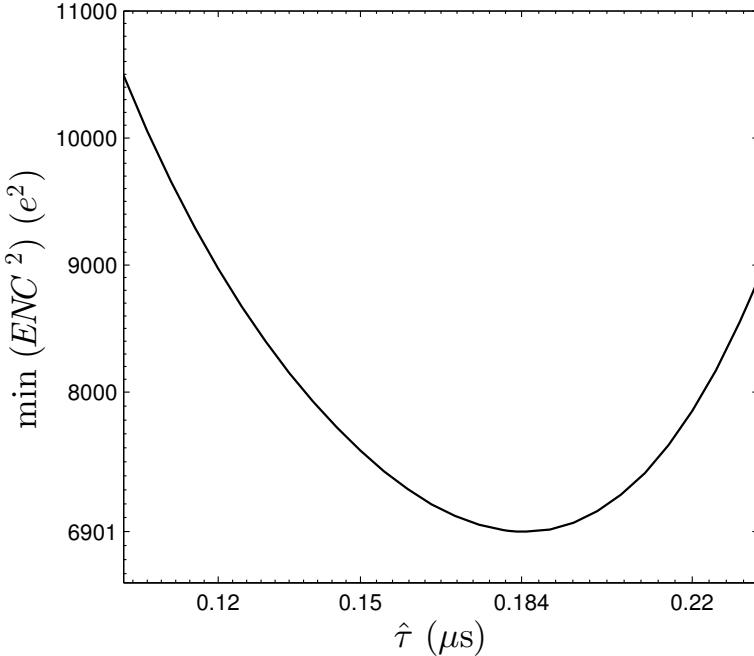


FIGURE 3.7. Minimum  $ENC^2$  as a function of  $\hat{\tau}$  for a fixed  $N$ .

The following parameters, typical of an HPGe segmented detector (Pullia & Riboldi, 2004), were used:  $T = 120 \text{ K}$ ,  $g_m = 15 \text{ mS}$ ,  $R_F = 1 \text{ G}\Omega$ ,  $I_L = 100 \text{ pA}$ ,  $C_T = 40 \text{ pF}$ ,  $C_F = 1 \text{ pF}$  and  $a_F = 10^{-15} \text{ V}^2$ . Additionally, the following parameters were arbitrarily selected:  $t_m = 10 \mu\text{s}$ ,  $T_s = 0.5 \mu\text{s}$  and  $h_w = 1$ .

The optimization problem was formulated in MATLAB and then solved through convex optimization with CPLEX (IBM, n.d.). Figure 3.7 shows the optimum value of the  $ENC^2$  as a function of  $\hat{\tau}$ , where the existence of a global optimum at  $\hat{\tau} = 0.184 \mu\text{s}$  can be seen. Figure 3.8 shows the optimum WF for different values of  $\hat{\tau}$ . Using the optimum WF and the noise parameters shown above the  $ENC$  can be computed as described in (Gatti & Manfredi, 1986) and (Pullia, 1998).

The initial assumption that the filter sampling period  $T_s$  is determined by the filter maximum clock rate is only valid if the optimum  $ENC^2$  is lower bounded by  $T_s$ , or equivalently, by  $N$ . To support this assumption, Figure 3.9 shows the optimum value of the  $ENC^2$  as a function of  $N$ . Although Figure 3.9 suggests to use the filter at the maximum

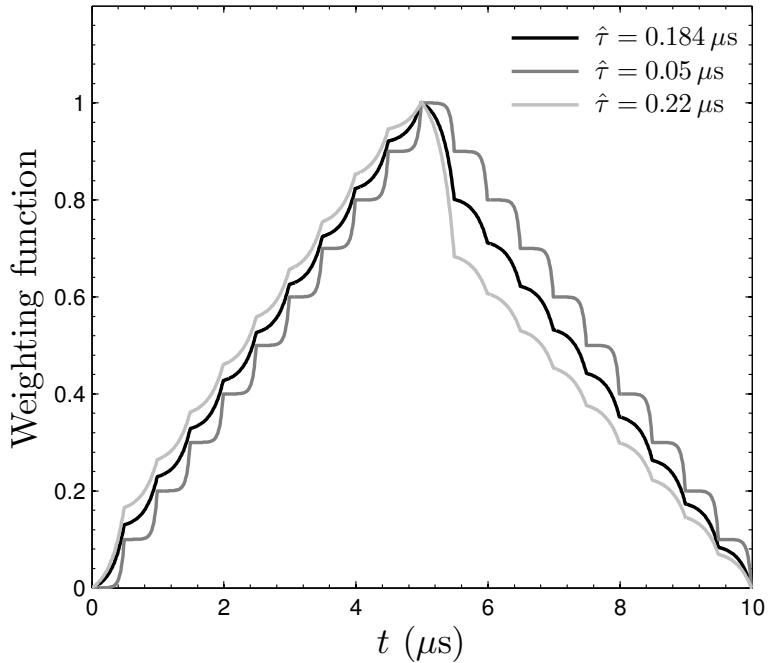


FIGURE 3.8. Optimum WF for different values of  $\hat{\tau}$  for  $N = 20$ .

clock rate, for a large number of samples the contribution of an additional sample is marginal, thus to determine  $N$  other considerations should be taken into account, such as the filter power consumption and the filter design complexity. Additional requirements, such as flat-top or zero-area, can be easily added as constraints in the optimization problem.

### 3.5 Conclusion

This work presents a mathematical framework for the analysis of discrete-time filters in the discrete-time domain. The analysis is based on decomposing the total integrated noise at the filter input into a set of discrete-time noise signals, in order to refer them to the filter output and calculate the *ENC*. The proposed analysis only depends on the calculation of the total integrated noise at the filter input, which can be analyzed prior to taking into account the filter itself in order to understand and predict the noise behavior.

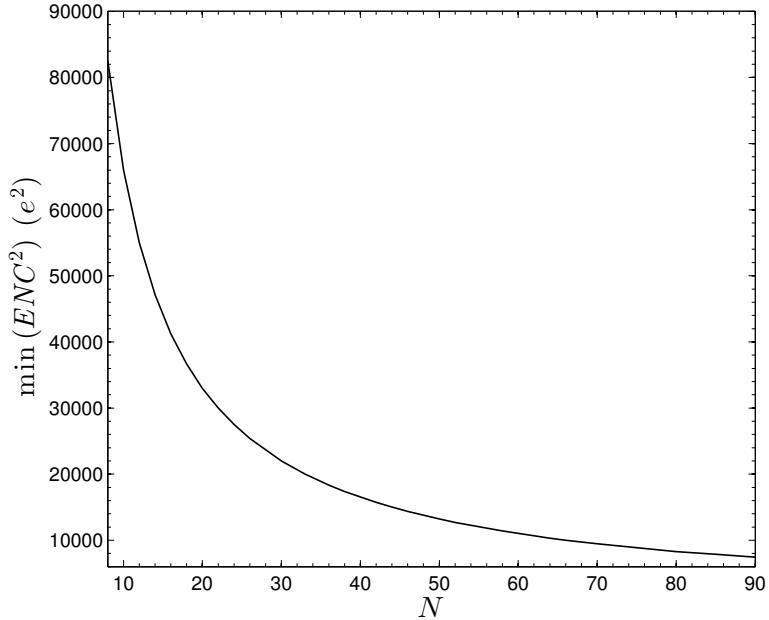


FIGURE 3.9. Optimum  $ENC^2$  as a function of  $N$  for  $\hat{\tau} = 0.03 \mu s$ .

In order to validate the proposed framework, the computation of the thermal noise contribution at the output of a discrete-time integrator is presented, and the result is compared to the result produced by the traditional continuous-time approach. Although both methods produce mathematically equivalent results, the former is simpler and more insightful.

This work also presents an example of optimal filter computation, in order to demonstrate the proposed framework capabilities and its application to optimization problems with several noise sources.

## 4. A SC FILTER FOR ARBITRARY WEIGHTING FUNCTION SYNTHESIS

### 4.1 Introduction

One of the greatest benefits of the mathematical framework presented in the previous chapter is that it allows to easily compute the optimal discrete-time filter that maximize the SNR of a typical detector front-end circuit, a difficult task to undertake using the traditional methods for continuous-time networks. The filter presented in this chapter is designed to be flexible enough to synthesize arbitrary weighting functions within an adequate resolution. Therefore, it can be used to synthesize the optimal filter described above. The filter is a prototype of the front-end filter for the Bean 2, which was introduced in the Chapter 2. Hence, main specifications are derived from the Bean specifications. Also, power, noise and space budgets of the referred IC are taken as constraints.

There are two common options for implementing the required filter, the simplest is to directly digitize the CSA output with a fast analog-to-digital converter (ADC) -  $N$  time faster than the typical used ADC, with  $N$  the number of desired samples - and then process the samples in the digital domain, while the other option is to use a custom switched capacitor (SC) network as a filter, without changing the ADC requirements. Considering the Bean timing constraints, the former option is not feasible, given that such fast ADC would exceed the available power and space budgets. Hence, the SC solution was chosen.

### 4.2 System-Level Design

As mentioned in the previous Chapter, to synthesis arbitrary weighting functions the front-end filter should be designed to have a discrete-time transfer function  $F(z)$  given by

$$F(z) = \sum_{j=0}^{N-1} a_{N-j} z^{-j} \quad (4.1)$$

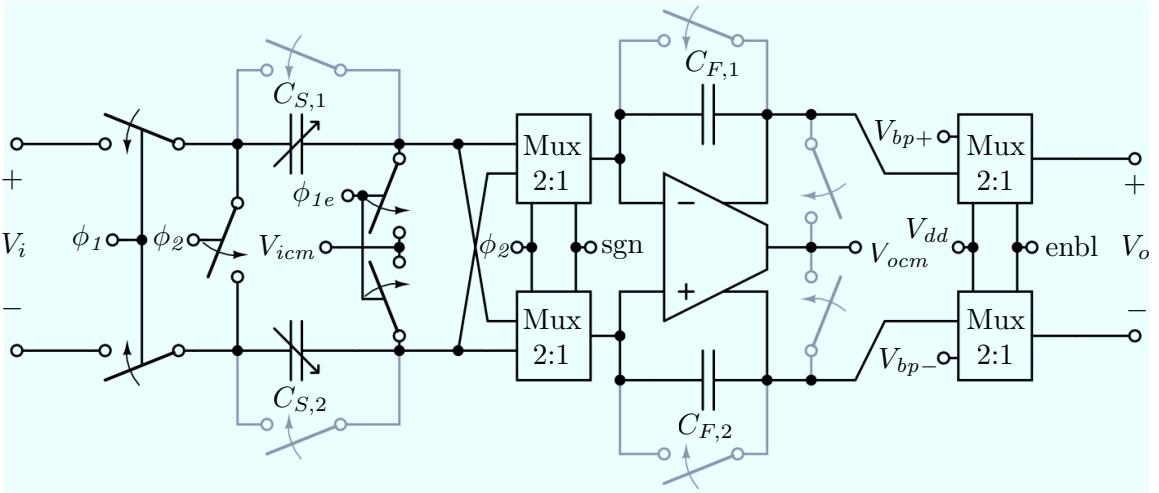


FIGURE 4.1. Simplified filter schematic. Reset switches are depicted in gray.

where  $a_i$  are arbitrary coefficients and  $N$  is the filter length. Fig. 4.1 shows a simplified circuit diagram of fully-differential SC integrator designed to implement  $F(z)$ . Some control logic and switches have been purposely omitted.

In this configuration, the filter gain is given by the ratio of the capacitors  $C_S$  and  $C_F$ . Considering that to obtain arbitrary coefficients the filter gain must be programmable, either  $C_S$  or  $C_F$  should be implemented with a variable capacitor. For simplicity, capacitor  $C_S$  was selected for this purpose. The OTA input multiplexers are used to swap the OTA inputs, and therefore, to invert the filter gain sign. The OTA output common-mode level is set by the OTA's internal common-mode feedback (CMFB) circuit, whereas the input common-mode level is set by the external reference  $V_{icm}$ . The OTA output multiplexers are used to bypass the filter for the SDT operation mode and for diagnostic purposes.

#### 4.2.1 Filter Specifications

Table 4.1 summarize the filter specifications derived from the Bean specifications. Also, CSA output specifications and ADC input specifications were taken into account. The sampling frequency is 51.95 MHz. Thus, each integration subcycle is 19.25 ns long. Since each subcycle involves two phases, sampling and holding, each phase has only 9.625 ns for settling. Considering this time, to assure a dynamic error of 0.1 % (to meet

Specification	Value
Modes of operation	SDT and DCal
Input swing	0.9 V or close
Output swing	1 V or close
Dynamic range	10 bit
Gain resolution	6 bit (7.8 mV/V - 0.5 V/V)
Noise budget	$1.25 \times Q_n^2$
Operation speed	51.95 MHz
Power consumption	Minimize

TABLE 4.1. Filter specifications summary.

the dynamic range specification) the designed OTA must have an unitary frequency of  $f_u = 118$  MHz, this without considering slew-rate regime. Also, a static error of 0.1 % is required, which implies an OTA open-loop gain of at least 60 dB.

### 4.3 Circuit Design

Previous version of the Bean uses a two-stage miller-compensated OTA as the filter amplifier. However, this topology doesn't lead to a feasible design given the filter specifications, mainly, because of the existing trade-off between noise and bandwidth resulting from the Miller capacitor. For this version of the Bean, a single stage OTA topology was chosen, as it can theoretically meet the filter specifications. A folded cascode (FC) OTA would be the first candidate to implement this amplifier, because of its good balance between gain, speed, input-output swing and complexity. Nonetheless, the settling-time specification would require high bias currents due to the slew-rate limitation, which would come into conflict with the power budget. The recycling folded cascode OTA (RFC) (Assaad & Silva-Martinez, 2009), a small variation of the FC OTA, was chosen to overcome this problem, since it exhibits an enhanced transconductance, gain, and slew-rate (SR) over that of the conventional FC OTA for the same power and area budgets.

In a SC integrator, noise is sampled at both clock phases, namely  $\phi_1$  and  $\phi_2$ . Thus, to calculate the filter output-referred total integrated noise, both noise contributions must be

calculated separately and added up in quadrature. After  $N$  integration cycles and assuming an arbitrary  $C_S$  at each cycle, the contribution from noise sampled at  $\phi_1$  can be computed as:

$$\overline{V_{\phi_1}^2} = 2kT \sum_{i=1}^N \frac{1}{C_F} \left( 1 + \frac{C_{S_i}}{C_F} \right) \quad (4.2)$$

In a proper design, switches resistance will be much smaller than  $1/(\beta g_{m,eff})$ , so noise at  $\phi_2$  can be assumed dominated by OTA noise (Vleugels, 2011). Thus, contribution from noise sampled at  $\phi_2$  can be approximated as:

$$\overline{V_{\phi_2}^2} \approx \frac{2N_f kT \gamma}{g_{m,eff}} \sum_{i=1}^N \frac{1}{\beta_i C_{Ltot_i}} \quad (4.3)$$

where  $N_f$  is a noise factor dependent on the single-stage OTA topology, for a RFC:

$$N_f \approx \frac{1}{1+K} \left( \frac{1+K^2}{1+K} + \frac{g_{m,f}}{g_{m,in}} + \frac{1}{1+K} \frac{g_{m,l}}{g_{m,in}} \right) \quad (4.4)$$

$$G_{m,eff} \approx g_{m,in}(1+K) \quad (4.5)$$

$$R_{out} \approx g_{m,cf} r_{o,cf} (r_{o,in} \| r_{o,aux3}) \| g_{m,cl} r_{o,cl} r_{o,l} \quad (4.6)$$

$$\text{SR} = \frac{2K I_{tail}}{C_L} \quad (4.7)$$

$$\omega_u = \frac{G_{m,eff}}{C_L} \quad (4.8)$$

### 4.3.1 Operational Transconductance Amplifier

In a traditional FC OTA, folding transistors conduct the most current and generally have the largest transconductance. However, their role is only limited to providing a folding node for the small signal current (Assaad & Silva-Martinez, 2009). In a RFC OTA

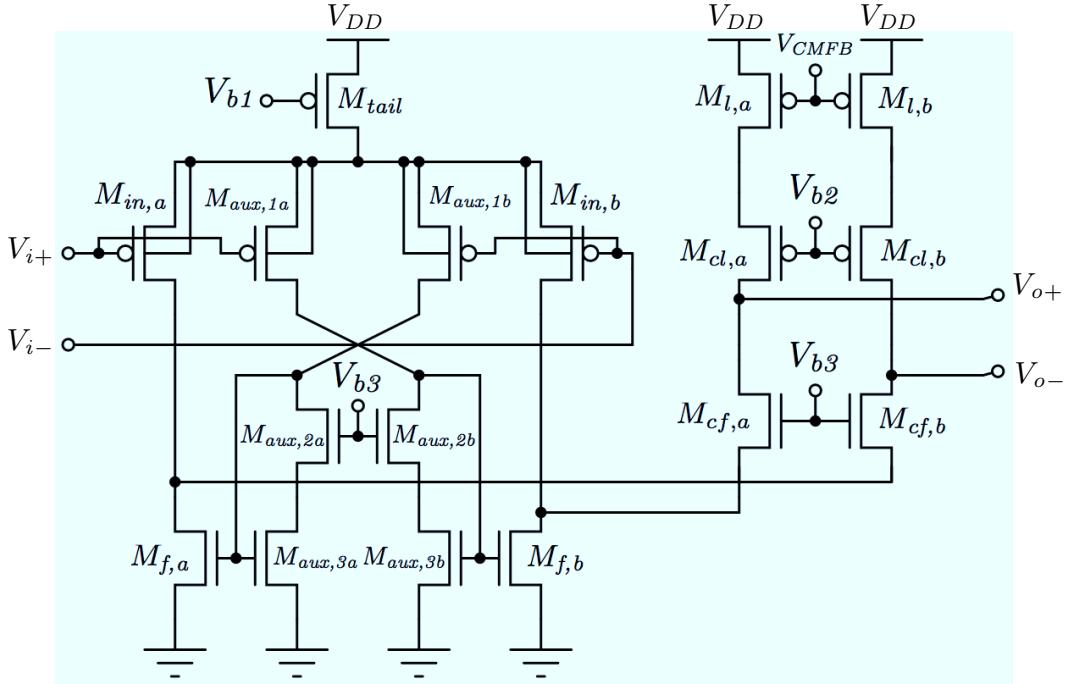


FIGURE 4.2. Recycling folded cascode OTA schematic. Three terminal NMOS and PMOS devices are with their bodies tied to ground and  $V_{DD}$  respectively.

(Fig. 4.2), a small modification over the conventional FC topology allows to use the folding transistors as additional drivers for the small signal input. Therefore, they are used to enhance the effective transconductance of the amplifier. Also, there are additional enhancements over the conventional FC OTA, such as: higher and symmetrical SR, higher output resistance and higher crossover-frequency.

Table 4.2 shows the parameter values for the OTA design, transistor sizes were calculated with an semi-exhaustive search script, with tabulated pre-simulated data and using the  $g_m/I_D$  design technique (Silveira, Flandre, & Jespers, 1996). Computational power was not a problem at this point. However, for a deeper optimal design, a bigger domain must be chosen (not increasing the boundaries but increasing the domain resolution) and an intelligent algorithm must be used, e.g like the use of Support Vector Machines in (Bernardinis, Jordan, & Sangiovanni-Vincentelli, 2003) for analog circuit automated design.

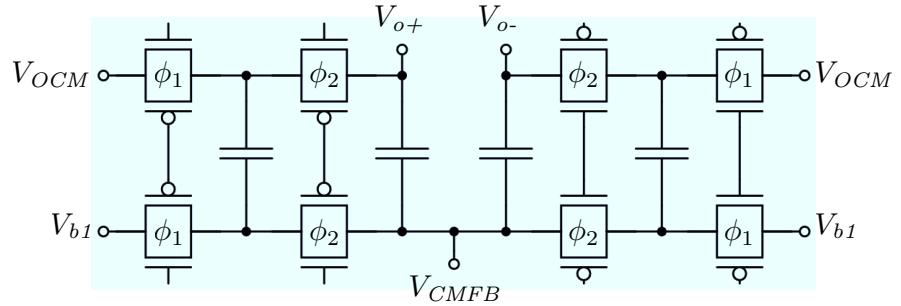


FIGURE 4.3. OTA discrete-time common-mode feedback circuit schematic.

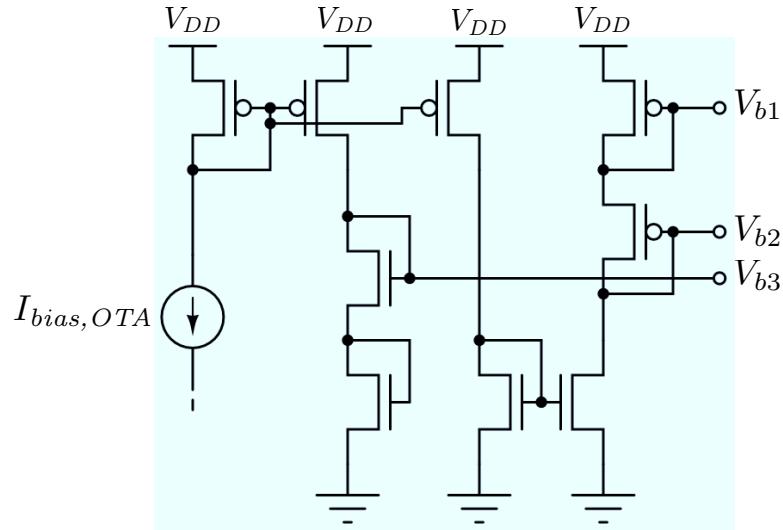


FIGURE 4.4. OTA bias network schematic.

Transistor	Bias current	$g_m/I_D$	$W$	$L$
$M_{in}$	$51.3 \mu\text{A}$	$14.9 \text{ mS/mA}$	$48 \mu\text{m}$	$0.36 \mu\text{m}$
$M_{tail}$	$201.7 \mu\text{A}$	$8.2 \text{ mS/mA}$	$64 \mu\text{m}$	$0.45 \mu\text{m}$
$M_f$	$100.6 \mu\text{A}$	$8.7 \text{ mS/mA}$	$8 \mu\text{m}$	$0.45 \mu\text{m}$
$M_{cf}$	$49.3 \mu\text{A}$	$11.7 \text{ mS/mA}$	$8 \mu\text{m}$	$0.45 \mu\text{m}$
$M_{cl}$	$49.3 \mu\text{A}$	$10.7 \text{ mS/mA}$	$16 \mu\text{m}$	$0.3 \mu\text{m}$
$M_l$	$49.3 \mu\text{A}$	$7.6 \text{ mS/mA}$	$32 \mu\text{m}$	$1 \mu\text{m}$
$M_{aux,1}$	$49.6 \mu\text{A}$	$15 \text{ mS/mA}$	$48 \mu\text{m}$	$0.36 \mu\text{m}$
$M_{aux,2}$	$49.6 \mu\text{A}$	$9.5 \text{ mS/mA}$	$2 \mu\text{m}$	$0.18 \mu\text{m}$
$M_{aux,3}$	$49.6 \mu\text{A}$	$6 \text{ mS/mA}$	$4 \mu\text{m}$	$0.45 \mu\text{m}$

TABLE 4.2. Filter OTA design values.

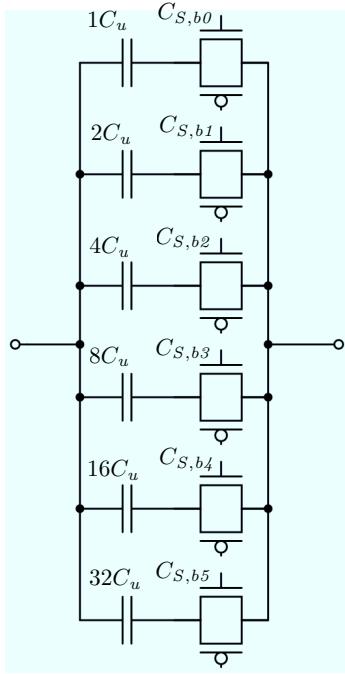


FIGURE 4.5. 6-bit programmable capacitor.

### 4.3.2 Variable Capacitor

Fig. 4.5 shows a schematic of the binary-weighted array used to implement the variable capacitor  $C_S$ . All capacitors  $C_{S,bn}$  were designed as a parallel connection of unit MOM capacitors  $C_u = 8.1 \text{ fF}$  (with size  $2.7 \mu\text{m} \times 2.7 \mu\text{m}$ ), which for matching purposes were also used to implement capacitor  $C_F$ . CMOS switches were sized to meet filter speed specifications. Switch control signals will be directly bonded out off-chip. A serial-programmable memory to store the filter coefficients, and which will be connected directly to this control signals - to avoid the unnecessary waste of IC pads -, will be included in future revisions of the Bean.

### 4.3.3 Rail-to-Rail buffer

A signal buffer is required to buffer some of the Bean prototype nodes for scope probing. The buffer must be able to drive a  $8 \text{ pF}$  load at a reasonable speed and power dissipation, with truly rail-to-rail input and output voltages. Fig. 4.6 shows the schematic

of a rail-to-rail operational amplifier (op-amp) used to implement an unity gain voltage buffer amplifier.

The two-stage op-amp consists of a rail-to-rail constant- $g_m$  input stage (Hogervorst, Tero, & Huijsing, 1995), composed by two complementary input pairs and an electronic zener diode,  $M_{in1}$ - $M_{in2}$ ,  $M_{ip,a}$ - $M_{ip,b}$  and  $M_{zp}$ - $M_{zn}$ , followed by folded-cascode, current-mirroring loads,  $M_{chn1}$ - $M_{ln1}$ ,  $M_{chn2}$ - $M_{ln2}$ ,  $M_{clp1}$ - $M_{lp1}$  and  $M_{clp2}$ - $M_{lp2}$ , and a class-AB output (Hogervorst, Tero, Eschauzier, & Huijsing, 1994),  $M_{op}$ - $M_{on}$ . Transistors  $M_{sn1}$ - $M_{sn2}$  and  $M_{sp1}$ - $M_{sp2}$  implement a translinear loop (Sansen, 2006), producing the voltage shifts necessary to set the output devices quiescent current consumption.

Table 4.3 shows the parameter values for the rail-to-rail buffer design, transistor sizes were calculated with the same methodology as for the OTA design.

As for most of two-stage amplifiers, stability must be assured with a proper compensation scheme. In this design, capacitor  $C_C$ , also known as Miller capacitor, is placed to lower the frequency of the dominant pole and to increase the frequency of the secondary pole, and thus, it helps to increase the phase margin of the amplifier, while resistor  $R_Z$  is used to cancel the right-half plane zero that appears because adding  $C_C$ . Since  $C_C$  is calculated as a function of the input stage's total transconductance, the constant- $g_m$  compensation technique used for the input stage helps to maintain a constant frequency response over all the input common mode range.

To assure predictable bias currents and a true rail-to-rail input and output voltage ranges, a proper bias network must be designed. Fig. 4.7 shows a schematic of the bias network used for this op-amp (Baker, 2010). All bias voltages are driven by cascaded current mirrors, which have high output resistance in order to reduce the influence of  $V_{ds}$  over the mirrored current. Transistor sizes were calculated to assure a maximum amplifier output swing and current mirrors currents were chosen to maintain a good compromise between mirrored currents sensibility and bias network power consumption.

SPICE simulations predict an open-loop DC gain of 103 dB, a crossover frequency of 52 MHz, and a phase margin of 78° measured with an 8 pF load.

Transistor	Bias current	$g_m/I_D$	$W$	$L$
$M_{in}$	$10.4 \mu\text{A}$	$21.2 \text{ mS/mA}$	$12.8 \mu\text{m}$	$0.45 \mu\text{m}$
$M_{ip}$	$9.2 \mu\text{A}$	$19.4 \text{ mS/mA}$	$40 \mu\text{m}$	$0.45 \mu\text{m}$
$M_{tp}$	$60.6 \mu\text{A}$	$7.4 \text{ mS/mA}$	$20 \mu\text{m}$	$0.45 \mu\text{m}$
$M_{tn}$	$62.9 \mu\text{A}$	$9.2 \text{ mS/mA}$	$6.4 \mu\text{m}$	$0.45 \mu\text{m}$
$M_{lp}$	$26.3 \mu\text{A}$	$9.1 \text{ mS/mA}$	$10 \mu\text{m}$	$0.45 \mu\text{m}$
$M_{clp}$	$16 \mu\text{A}$	$14.2 \text{ mS/mA}$	$20 \mu\text{m}$	$0.45 \mu\text{m}$
$M_{ln}$	$25.2 \mu\text{A}$	$10.9 \text{ mS/mA}$	$3.2 \mu\text{m}$	$0.45 \mu\text{m}$
$M_{cln}$	$16 \mu\text{A}$	$16.8 \text{ mS/mA}$	$6.4 \mu\text{m}$	$0.45 \mu\text{m}$
$M_{op}$	$282 \mu\text{A}$	$9 \text{ mS/mA}$	$100 \mu\text{m}$	$0.45 \mu\text{m}$
$M_{on}$	$282 \mu\text{A}$	$10.7 \text{ mS/mA}$	$32 \mu\text{m}$	$0.45 \mu\text{m}$

TABLE 4.3. Rail-to-rail buffer main design values.

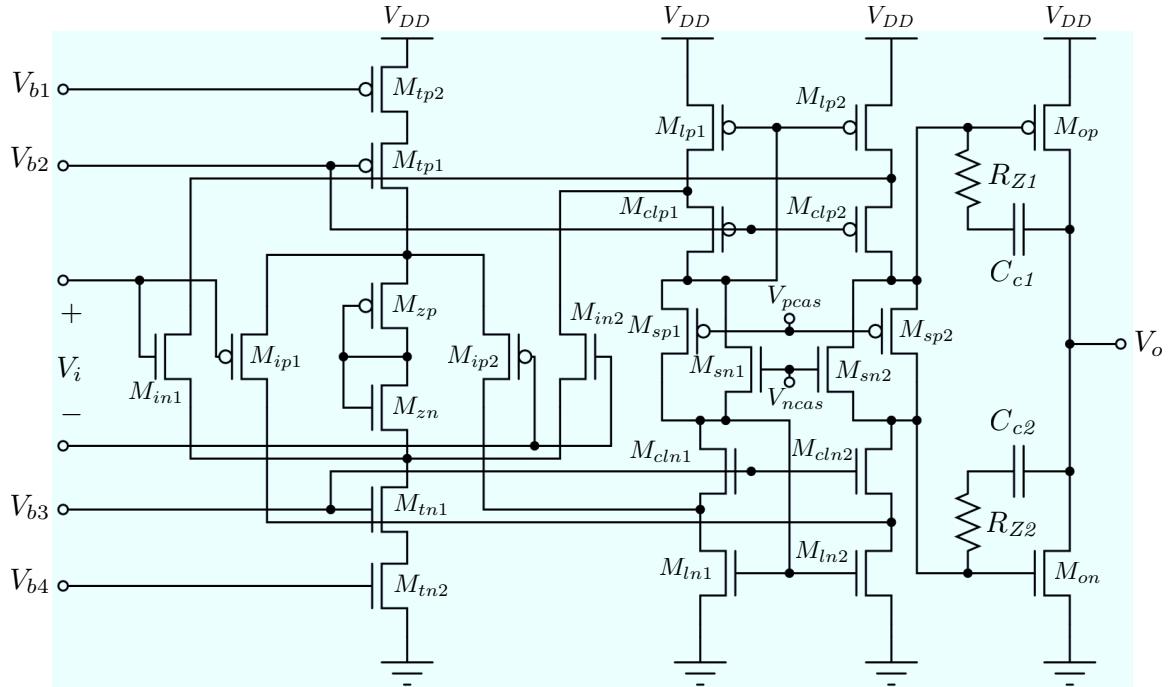


FIGURE 4.6. Rail-to-rail operational amplifier schematic.

#### 4.3.4 IC bias network

Previous version of the Bean uses a voltage distribution scheme to bias all the circuits on the IC, but it can cause big problems due to IR drop and process gradients, so a more common current distribution scheme was chosen for this design iteration (Murmann,

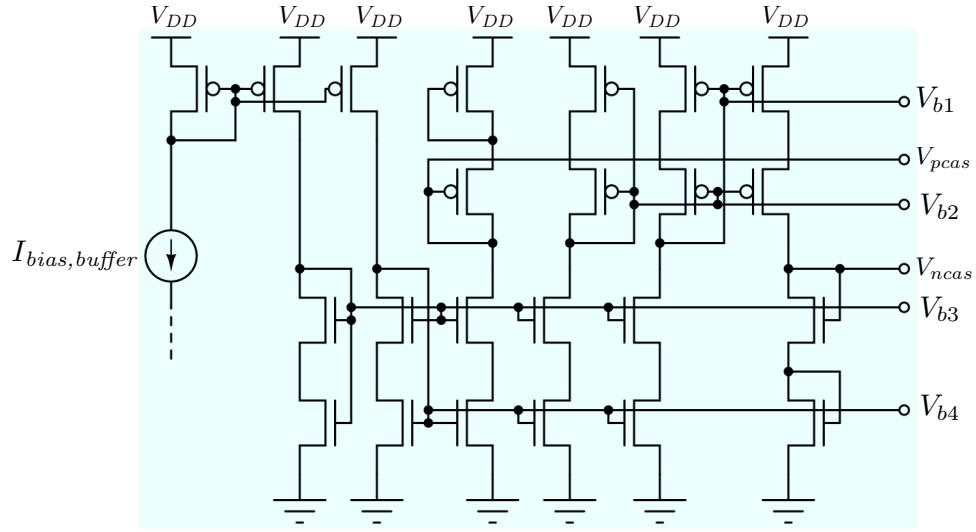


FIGURE 4.7. Op-amp bias network schematic.

2007). Main disadvantage of this architecture is the additional current consumption, but this drawback is marginal compared to the entire IC power budget and the obtained benefits. To achieve a good power supply rejection (PSR), a supply-insensitive bias network was chosen to implement the global bias cell, from which all the bias currents are generated. Fig. 4.8 shows a diagram of the current distribution bias scheme. For simplicity, only three current branches are illustrated, although five were used in the final design. Fig. 4.9 shows a schematic of a  $\beta$ -multiplier bias circuit, the architecture selected to implement the supply-insensitive bias network. This consists of a self-biased current-reference network, a start-up circuit, because the two possible operating points, and cascode current mirror. The  $\beta$ -multiplier is an example of a circuit that uses positive feedback. The addition of the resistor kills the closed loop gain (a positive feedback system can be stable if its closed loop gain is less than one). However, if the parasitic capacitance of this resistor is large, it will increase the loop gain and push the feedback system closer to instability. If the resistor, for example, is bonded out off-chip to set the current, it is likely that this bias circuit will oscillate (Baker, 2010).

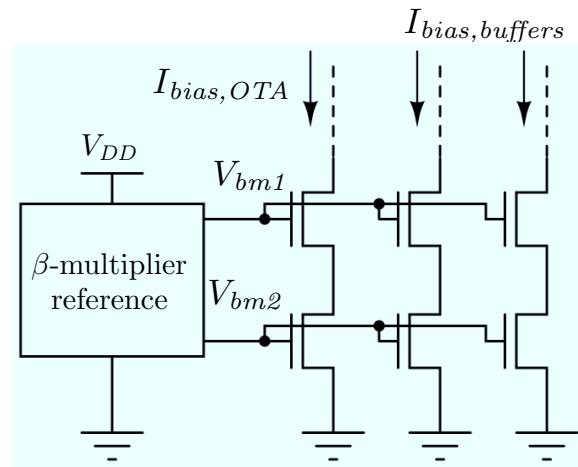


FIGURE 4.8. Current distribution bias scheme.

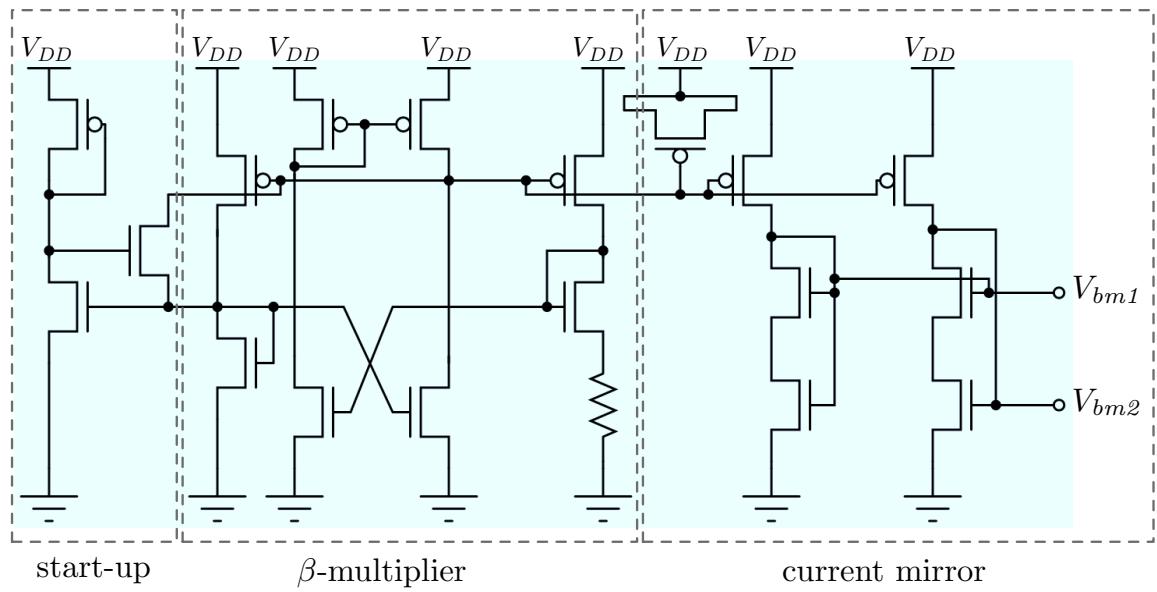


FIGURE 4.9.  $\beta$ -multiplier bias schematic.

## **5. RESULTS**

### **5.1 The Bean 2 prototype Implementation**

The Bean 2 prototype was designed on United Microelectronics Corporation (UMC) RFMM180 technology and send to fabricate through Europractice IC mini@sic program.

Fig. 5.1 shows the layout of the Bean 2 prototype, for a detailed description of the IC pinout, see Appendix A.

### **5.2 Filter simulation results**

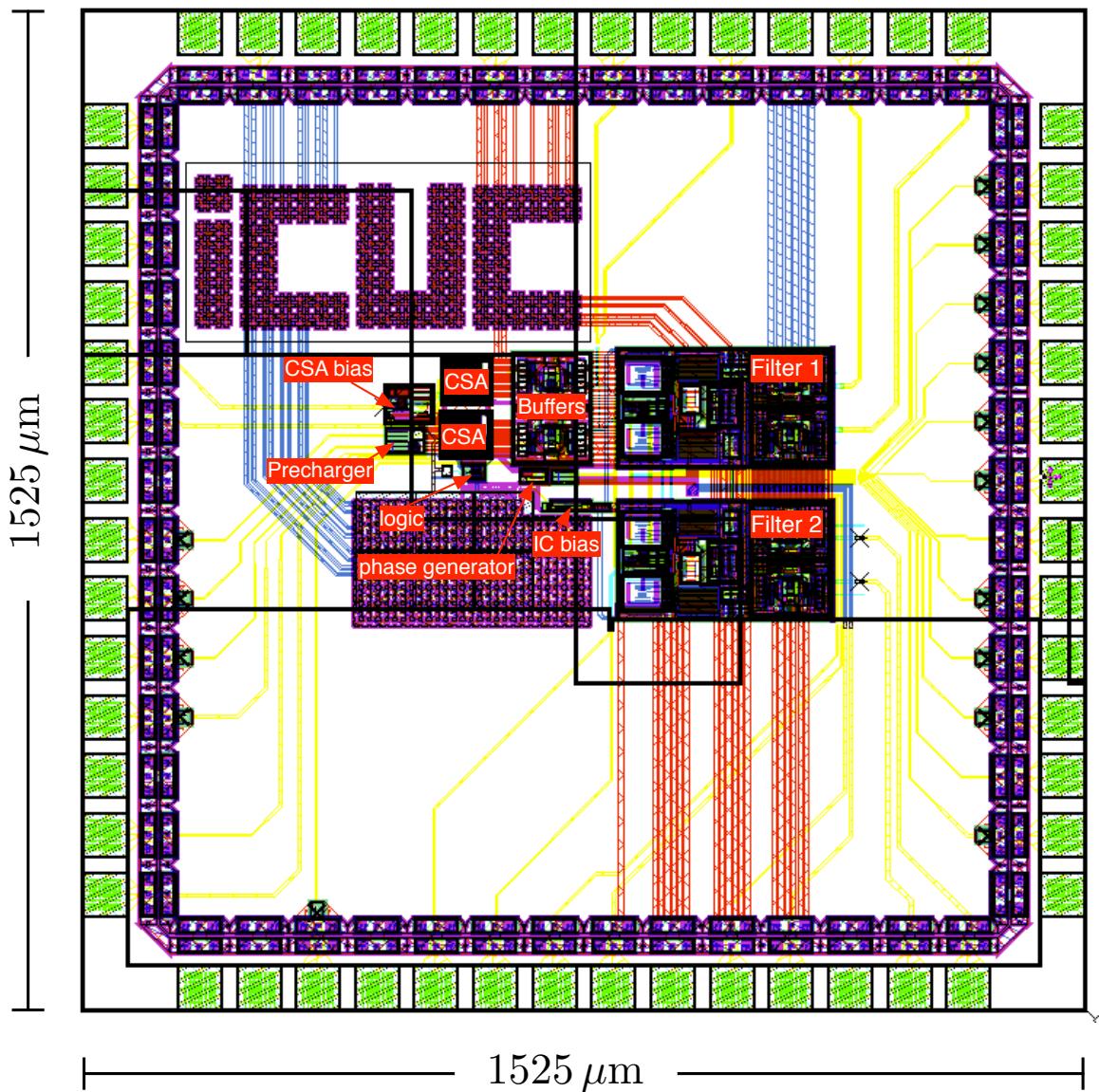


FIGURE 5.1. The Bean 2 prototype layout.

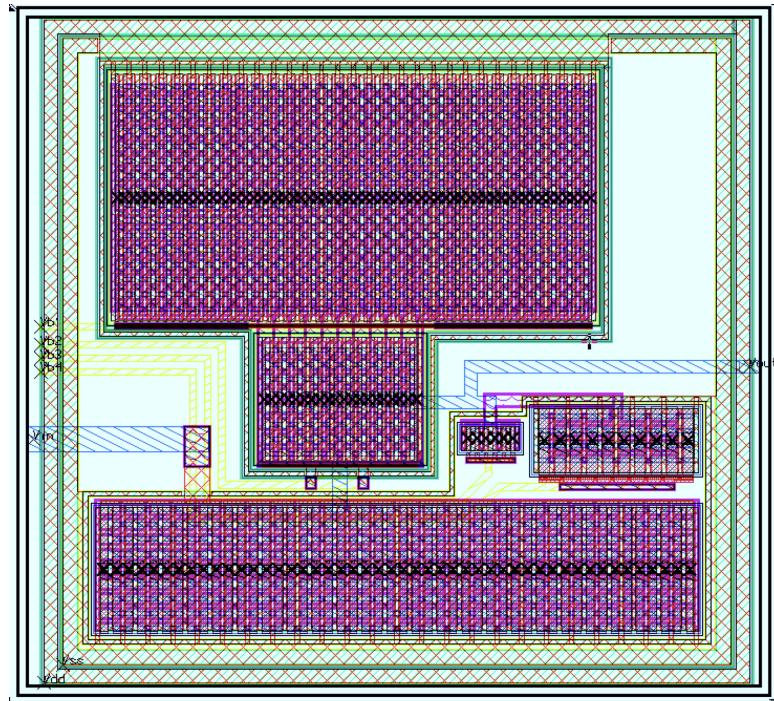


FIGURE 5.2. Charge-sensitive amplifier layout.

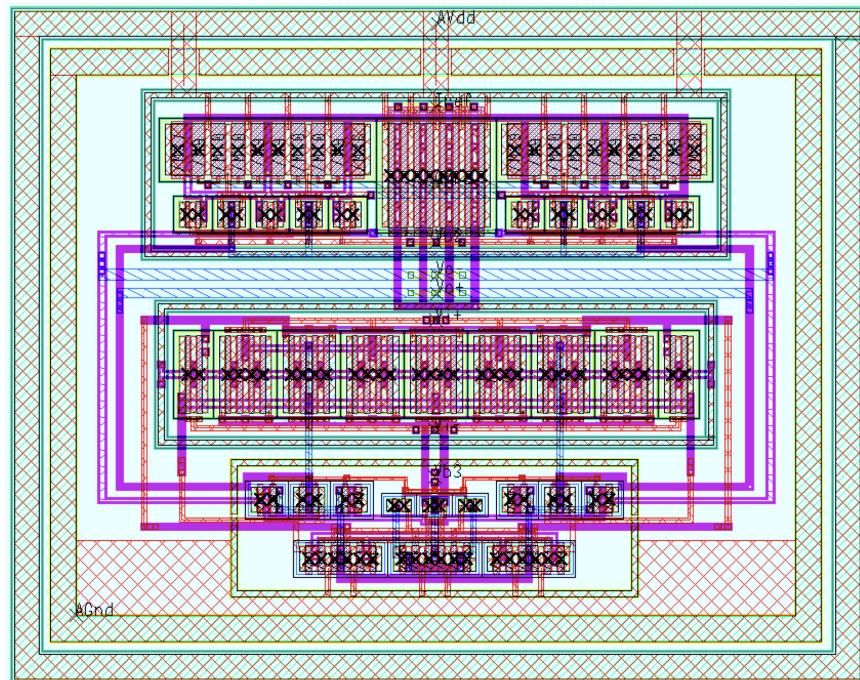


FIGURE 5.3. Recycling folded cascode OTA layout.

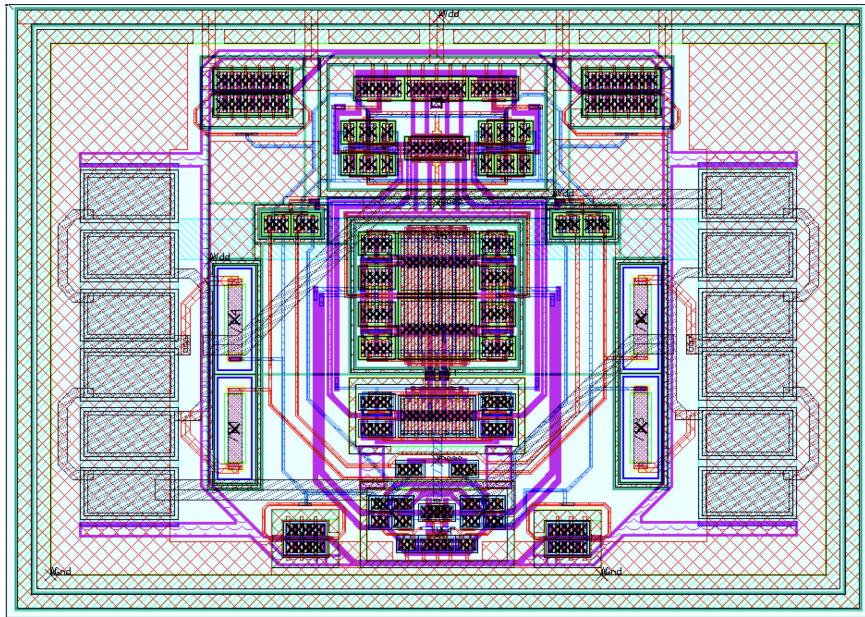


FIGURE 5.4. Rail-to-rail operational amplifier layout.

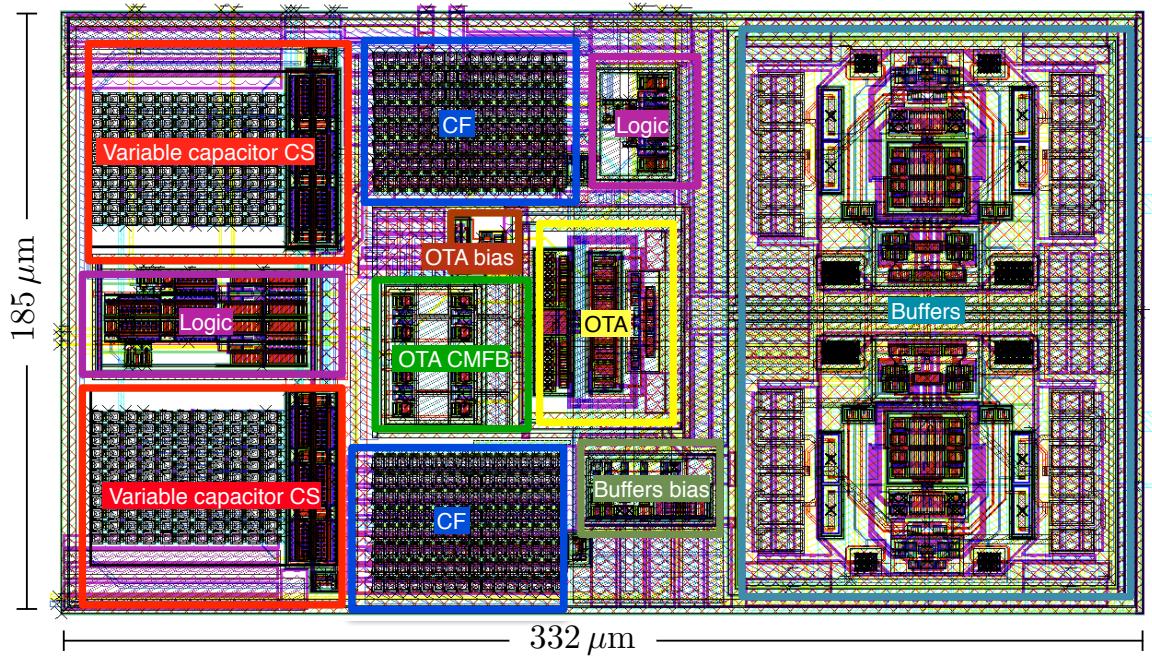


FIGURE 5.5. Filter Layout.

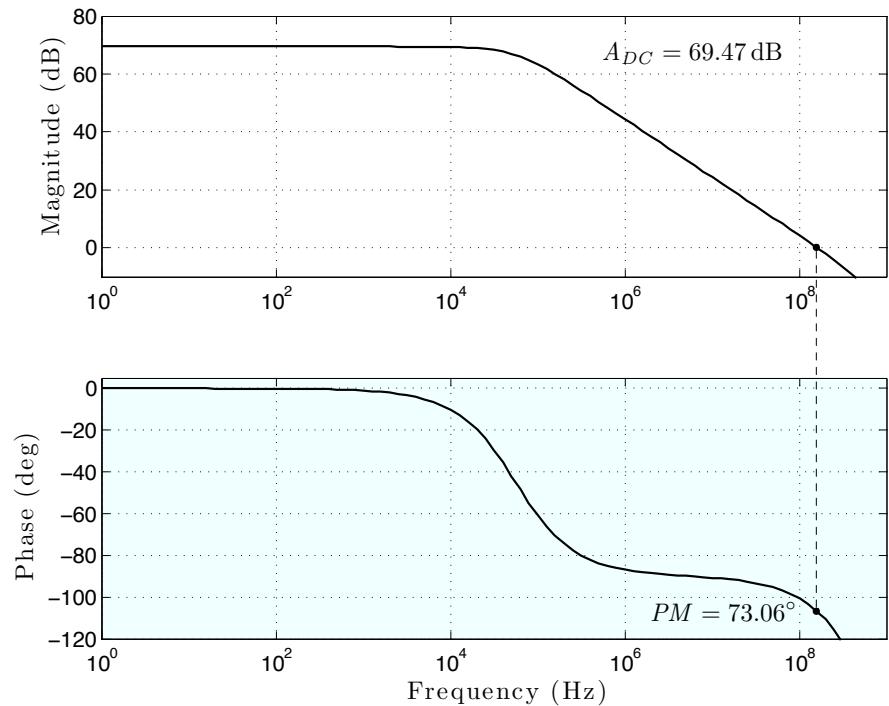


FIGURE 5.6. Bode plot for the OTA open-loop response.

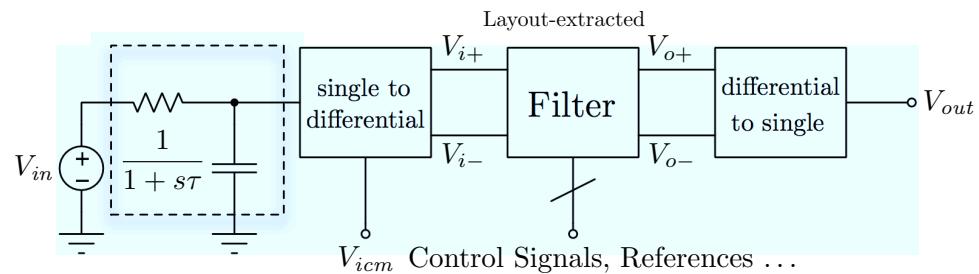


FIGURE 5.7. Weighting function test circuit.

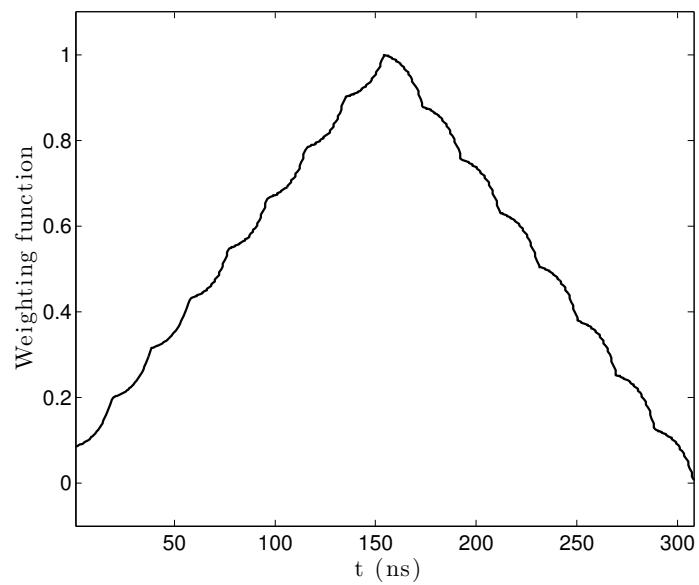


FIGURE 5.8. SPICE-simulated weighting function.  $\tau = 8$  ns,  $N = 16$  and  $T_s = 19.25$  ns.

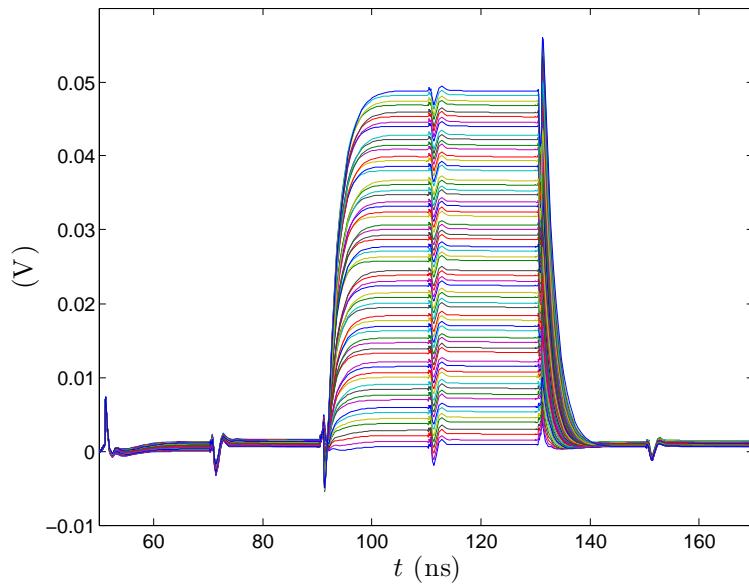


FIGURE 5.9. Filter output step response with the 64 programmable gains.  $V_{in} = 0.1$  V and  $T_s = 40$  ns.

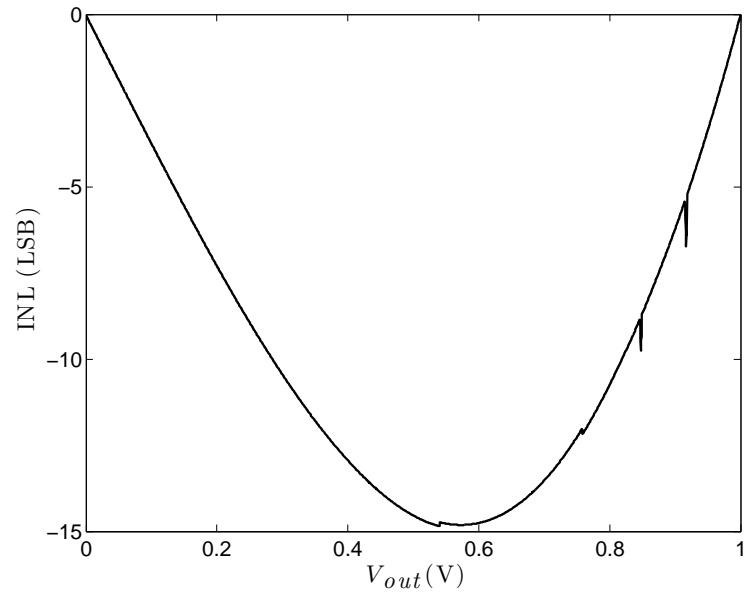


FIGURE 5.10. Filter linearity test results, full-scale input range.

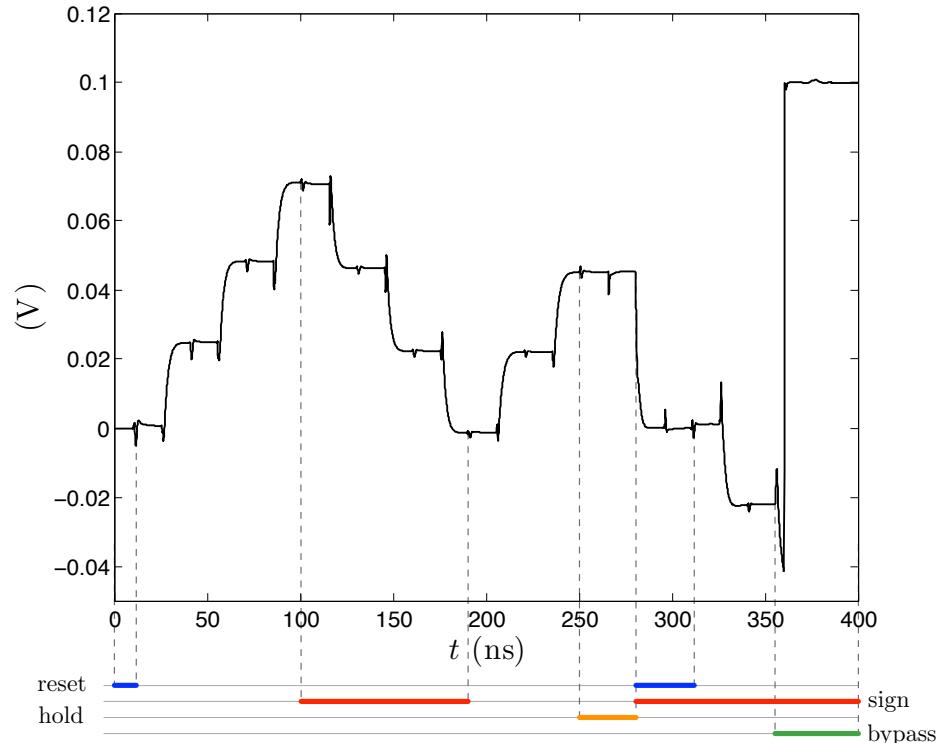


FIGURE 5.11. Filter control signals testing.  $V_{in} = 0.1$  V and gain =  $0.25$  V/V.

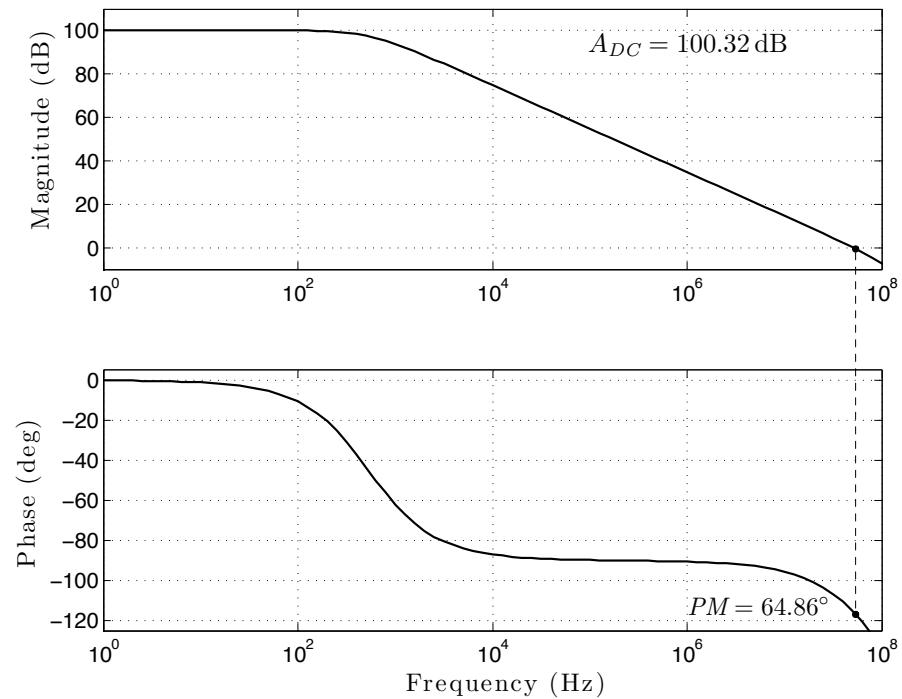


FIGURE 5.12. Bode plot for the buffer open-loop response.

## **6. CONCLUSION**

### **6.1 Summary**

This thesis deals with the use of discrete-time filters to lower the noise present in the detectors front-end circuits. Main contributions of this work are: the development of a new mathematical framework a design-oriented analysis of discrete-time filters in the discrete-time domain; and the design and implementation of a switched-capacitor filter for arbitrary weighting function synthesis to be included in the Bean 2 IC.

The noise analysis methodology introduced in this work allows to easily compute the optimal discrete-time filter that maximize the SNR of a typical detector front-end circuit, a difficult task to undertake using the traditional methods for continuous-time networks.

The SC filter for arbitrary weighting function synthesis for the Bean 2 IC has been also presented, along with post-layout simulations for functionality verification. The use of this filter, along with a proper characterization of the CSA and detector noise statistics, will allow to design an optimum filter based on the noise analysis presented in this work.

### **6.2 Future work**

## **APPENDIX**

## A. THE BEAN 2 PROTOTYPE PINOUT

The Bean 2 prototype has 48 pads and was bonded to an 64-lead package from Kyocera Corporation (KYO). The package KYO part number is QC064307WZ. The Bean bonding diagram is shown in Fig. A.1. Table A.1 shows the Bean 2 pinout.

Pin number	Pin name	Description
1	AGnd	Analog ground
2	AGnd	Analog ground
3	AGnd	Analog ground
4	NC	No connection
5	NC	No connection
6	res_bias_ext	IC bias external resistor
7	V_ref_prechar	Reference voltage CSA precharger
8	NC	No connection
9	clk_prech1	CSA precharger clk1
10	clk_prech2	CSA precharger clk2
11	NC	No connection
12	op_mode	Operation mode select
13	rst_csa	CSA reset
14	NC	No connection
15	cap_charge_ext	CSA precharger external capacitor
16	Vin_csa	Vin CSA
17	NC	No connection
18	clk	IC clock
19	AGnd	Analog ground
20	AGnd	Analog ground
21	Vi+_fil	Filter Vi+

<b>Pin number</b>	<b>Pin name</b>	<b>Description</b>
22	Vi-_fil	Filter Vi-
23	NC	No connection
24	Vo-_bp_fil	Filter bypass Vo-
25	Vo+_bp_fil	Filter bypass Vo+
26	NC	No connection
27	DVdd	Digital Vdd
28	DGnd	Digital Gnd
29	NC	No connection
30	Vo-_fil	Filter Vo+ (buffered)
31	Vo+_fil	Filter Vo- (buffered)
32	NC	No connection
33	out_s	Filter output selection
34	Vocm	Filter Vocm
35	hold	Filter hold signal
36	rst	Filter reset
37	sgn	Filter gain sign
38	Vi <sub>cm</sub>	Filter Vi <sub>cm</sub>
39	NC	No connection
40	AGnd	Analog ground
41	NC	No connection
42	NC	No connection
43	CS_b0	Filter CS capacitor bit 0
44	CS_b1	Filter CS capacitor bit 1
45	CS_b2	Filter CS capacitor bit 2
46	CS_b3	Filter CS capacitor bit 3
47	CS_b4	Filter CS capacitor bit 4

<b>Pin number</b>	<b>Pin name</b>	<b>Description</b>
48	CS_b5	Filter CS capacitor bit 5
49	AGnd	Analog ground
50	AGnd	Analog ground
51	Vo+_ch	Channel Vo+ (buffered)
52	Vo-_ch	Channel Vo- (buffered)
53	NC	No connection
54	Vout_csa	CSA Vout (buffered)
55	NC	No connection
56	baseline	CSA baseline (buffered)
57	NC	No connection
58	NC	No connection
59	NC	No connection
60	AGnd	Analog ground
61	AGnd	Analog ground
62	AGnd	Analog ground
63	NC	No connection
64	AVdd	Analog Vdd

TABLE A.1. The Bean 2 prototype pinout

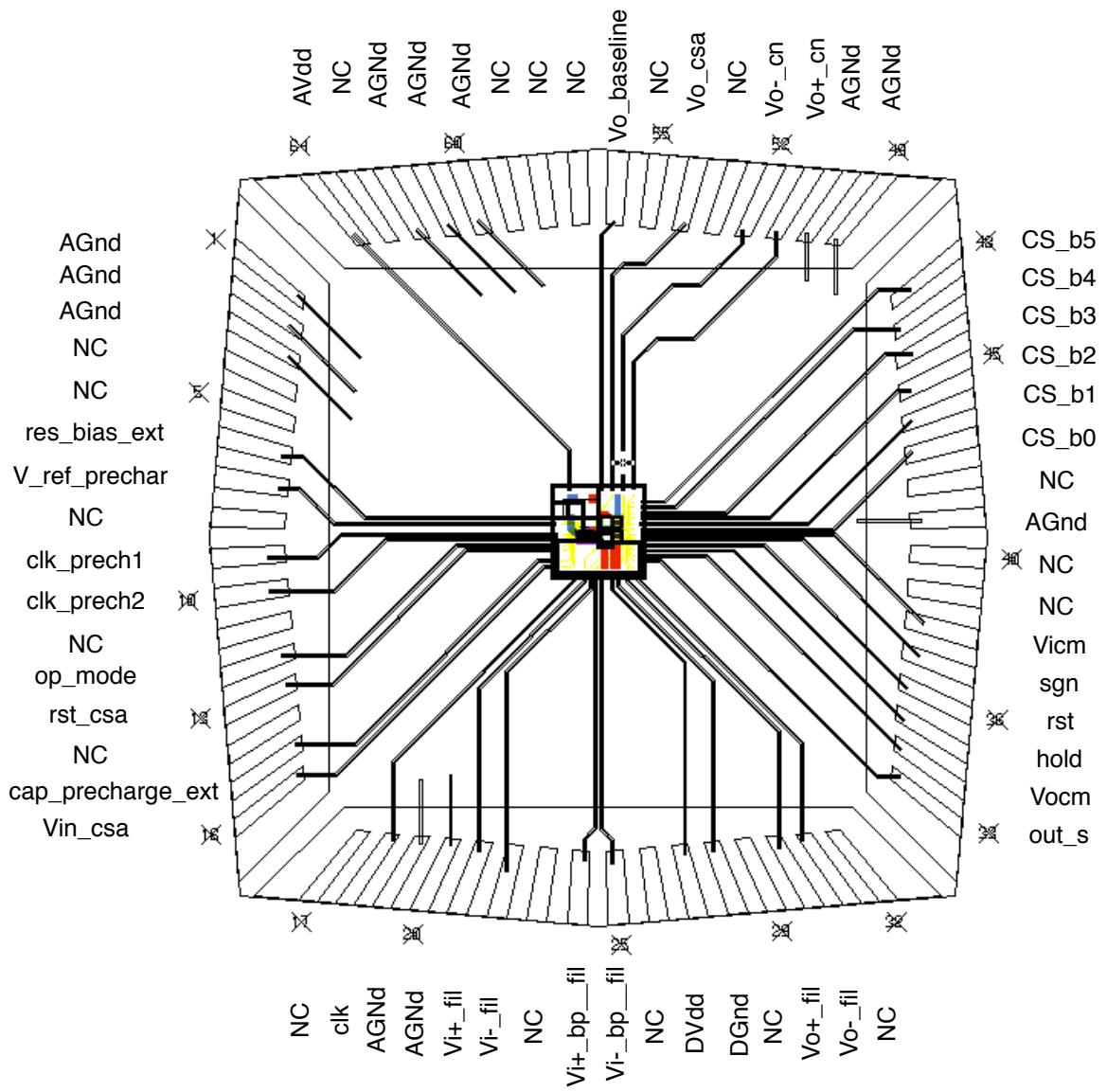


FIGURE A.1. The Bean 2 prototype bonding diagram.

## References

- Aad, G., et al. (2012). Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC. *Phys.Lett.*, *B716*, 1-29.
- Abusleme, A. (2011). *The Bean: A Pulse Processor for a Particle Physics Experiment* (Unpublished master's thesis). Stanford University.
- Abusleme, A., Dragone, A., Haller, G., & Wooley, B. (2012). Beamcal Instrumentation IC: Design, Implementation, and Test Results. *IEEE Trans. Nucl. Sci.*, *59*(3), 589-596.
- Alvarez, E., Avila, D., Campillo, H., Dragone, A., & Abusleme, A. (2012). Noise in Charge Amplifiers – A  $g_m/I_D$  Approach. *IEEE Transactions on Nuclear Science*, *59*, 2457–2462.
- Aspell, P., Barney, D., Bloch, P., Jarron, P., Lofstedt, B., Reynaud, S., & Tabbers, P. (2001). Delta: A Charge Sensitive Front-End Amplifier with Switched Gain for Low-Noise, Large Dynamic Range Silicon Detector Readout. *Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, *461*, 449–455.
- Assaad, R., & Silva-Martinez, J. (2009, Sept). The recycling folded cascode: A general enhancement of the folded cascode amplifier. *Solid-State Circuits, IEEE Journal of*, *44*(9), 2535-2542.
- Avila, D., Alvarez, E., & Abusleme, A. (2013, Dec). Noise analysis in pulse-processing discrete-time filters. *IEEE Trans. Nucl. Sci.*, *60*(6), 4634-4640.
- Baker, R. J. (2010). *Cmos circuit design, layout, and simulation* (3rd ed.). Wiley-IEEE Press.

- Bernardinis, F. D., Jordan, M. I., & Sangiovanni-Vincentelli, A. (2003). Support vector machines for analog circuit performance representation. In *in proceedings of dac* (pp. 964–969).
- Bertuccio, G., & Pullia, A. (1993). A method for the determination of the noise parameters in preamplifying systems for semiconductor radiation detectors. *Rev. Sci. Instrum.*, 64(11), 3294-3298.
- CERN. (2013). *How Detector Works*. Retrieved from <http://home.web.cern.ch/about/how-detector-works/>
- Chatrchyan, S., et al. (2012). Observation of a new boson at a mass of 125 GeV with the CMS experiment at the LHC. *Phys.Lett.*, B716, 30-61.
- De Geronimo, G., & O'Connor, P. (2005). MOSFET Optimization in Deep Submicron Technology for Charge Amplifiers. *IEEE Transactions on Nuclear Science*, 52(6), 3223–3232.
- De Geronimo, G., & O'Connor, P. (2005). MOSFET optimization in deep submicron technology for charge amplifiers. *IEEE Trans. Nucl. Sci.*, 52(6), 3223-3232.
- Fiorini, C., & Buttler, W. (2002). Multicorrelated double sampling readout of asynchronous events from multi-element semiconductor detectors. *IEEE Trans. Nucl. Sci.*, 49(3), 1566-1573.
- Gadomski, S., Hall, G., Høgh, T., Jalocha, P., Nygård, E., & Weilhammer, P. (1992, August). The deconvolution method of fast pulse shaping at hadron colliders. *Nuclear Instruments and Methods in Physics Research A*, 320, 217-227.
- Gatti, E., Geraci, A., & Ripamonti, G. (1996). Automatic synthesis of optimum filters with arbitrary constraints and noises: a new method. *Nucl. Instrum. and Meth.*, A381(1), 117-127.

Gatti, E., & Manfredi, P. (1986). Processing the signals from solid-state detectors in elementary-particle physics. *Riv. Nuovo Cim.*, 9, 1-146.

Gatti, E., & Manfredi, P. F. (1984, September). Present trends and realisations in readout electronics for semiconductor detectors in high energy physics. *Nuclear Instruments and Methods in Physics Research A*, 226, 142-155.

Gatti, E., Sampietro, M., & Manfredi, P. (1990). Optimum filters for detector charge measurements in presence of 1f noise. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 287(3), 513 - 520.

Geraci, A., & Gatti, E. (1995). Optimum filters for charge measurements in the presence of 1/f current noise. *Nucl. Instrum. and Meth.*, A361(2), 277-289.

Geraci, A., Zambusi, M., & Ripamonti, G. (1996). A comparative study of the energy resolution achievable with digital signal processors in X-ray spectroscopy. *IEEE Trans. Nucl. Sci.*, 43(2), 731-736.

Geronimo, G. D., O'Connor, P., Radeka, V., & Yu, B. (2001). Front-end electronics for imaging detectors. *Nucl. Instrum. and Meth.*, A471(12), 192-199.

Goulding, F. (1972). Pulse-shaping in low-noise nuclear amplifiers: A physical approach to noise analysis. *Nucl. Instrum. and Meth.*, 100(3), 493-504.

Haller, G., & Wooley, B. (1994). An Analog Memory Integrated Circuit for Waveform Sampling up to 900 MHz. *IEEE Transactions on Nuclear Science*, 41(4), 1203–1207.

Hogervorst, R., Tero, J. P., Eschauzier, R. G. H., & Huijsing, J. (1994, Dec). A compact power-efficient 3 v cmos rail-to-rail input/output operational amplifier for vlsi cell libraries. *Solid-State Circuits, IEEE Journal of*, 29(12), 1505-1513.

Hogervorst, R., Tero, J. P., & Huijsing, J. (1995, Sept). Compact cmos constant-gm rail-to-rail input stages with gm-control by an electronic zener diode. In *Solid-state circuits conference, 1995. esscirc '95. twenty-first european* (p. 78-81).

IBM. (n.d.). *ILOG CPLEX Optimizer*. Retrieved from <http://www.ilog.com/products/cplex/>

Jordanov, V. T. (2003). Real time digital pulse shaper with variable weighting function. *Nucl. Instrum. and Meth.*, A505(1), 347-351.

Kleinfelder, S., Chen, Y., Kwiatkowski, K., & Shah, A. (2004). High-Speed CMOS Image Sensor Circuits with In Situ Frame Storage. *IEEE Transactions on Nuclear Science*, 51(4), 1648–1656.

Lutz, G., Manfredi, P., Re, V., & Speziali, V. (1989). Limitations in the accuracy of detector charge measurements set by the 1/F noise in the front end amplifier. *Nucl.Instrum.Meth.*, A277, 194-203.

Murmann, B. (2007). Ee214: Analog integrated circuit design. *Stanford University*.

O'Connor, P., & De Geronimo, G. (1999). Prospects for Charge Sensitive Amplifiers in Scaled CMOS. In *Nuclear Science Symposium. 1999 IEEE Conference Record* (Vol. 1, pp. 88–93).

Porro, M., Herrmann, S., & Hornel, N. (2007). Multi correlated double sampling with exponential reset. In *IEEE nucl. sci. symp. conf. rec* (Vol. 26, p. 291-298).

Pullia, A. (1997). How to derive the optimum filter in presence of arbitrary noises, time-domain constraints, and shaped input signals: A new method. *Nucl. Instrum. and Meth.*, A397, 414-425.

Pullia, A. (1998). Impact of non-white noises in pulse amplitude measurements: a time-domain approach. *Nucl. Instrum. and Meth.*, A405(1), 121-125.

- Pullia, A., & Gatti, E. (2002). Optimal filters with constant-slope crossover and finite width for pulse-timing measurements. *IEEE Trans. Nucl. Sci.*, 49(3), 1170-1176.
- Pullia, A., & Riboldi, S. (2004). Time-domain Simulation of electronic noises. *IEEE Trans. Nucl. Sci.*, 51(4), 1817-1823.
- Radeka, V. (1968). Optimum Signal-Processing for Pulse-Amplitude Spectrometry in the Presence of High-Rate Effects and Noise. *IEEE Trans. Nucl. Sci.*, 15(3), 455-470.
- Radeka, V. (1984, September). Semiconductor position-sensitive detectors. *Nuclear Instruments and Methods in Physics Research A*, 226, 209-218.
- Radeka, V. (1988). Low-Noise Techniques in Detectors. *Ann. Rev. Nucl. Part. Sci.*, 38(1), 217-277.
- Radeka, V. (2011). Signal Processing for Particle Detectors. In C. Fabjan & H. Schopper (Eds.), *Detectors for Particles and Radiation. Part 1: Principles and Methods* (Vol. 21B1, p. 288-319). Springer Berlin Heidelberg.
- Sampietro, M., Bertuccio, G., Geraci, A., & Fazzi, A. (1995). A digital system for “optimum” resolution in x-ray spectroscopy. *Rev. Sci. Instrum.*, 66(2), 975-981.
- Sansen, W. (2006). *Analog design essentials*. Springer.
- Sansen, W., & Chang, Z. (1990). Limits of low noise performance of detector readout front ends in CMOS technology. *IEEE Trans. Circuits Syst.*, 37(11), 1375-1382.
- Silveira, F., Flandre, D., & Jespers, P. G. A. (1996, Sep). A gm/id based methodology for the design of cmos analog circuits and its application to the synthesis of a silicon-on-insulator micropower ota. *Solid-State Circuits, IEEE Journal of*, 31(9), 1314-1319.

- Snoeys, W., Campbell, M., Heijne, E. H. M., & Marchioro, A. (2000). Integrated Circuits for Particle Physics Experiments. In *2000 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)* (pp. 184-185, 455).
- Spieler, H. (2005). *Semiconductor detector systems*. Oxford University Press.
- Tuttle, K. (2013). Why particle physics matters. *Symmetry Magazine*.
- Van Der Ziel, A. (1970). Noise in solid-state devices and lasers. *Proc. of IEEE*, 58(8), 1178-1206.
- Vleugels, K. (2011). Ee315b: Vlsi data conversion circuits. *Stanford University*.