Final Exam
(Mathematics for Computer Science)

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Hardware Design

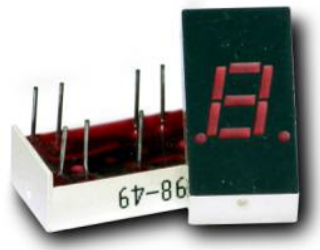
- Digital circuit based on boolean algebra

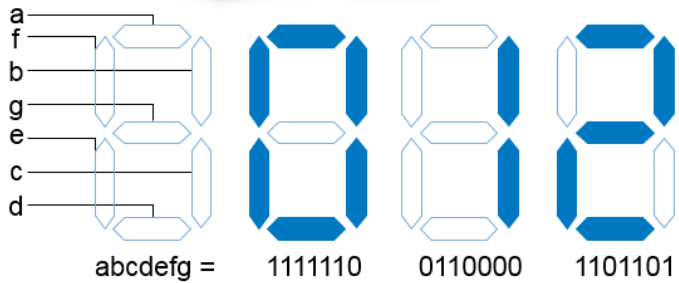
- **Reminder - You learned the below decoder.**

- Decoder Example:
  BCD(Binary Coded Decimal) to 7-Segment Display Decoder

TABLE 2-4 4-bit binary number to seven-segment display truth table

w	x	y	z	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0





Hardware Design

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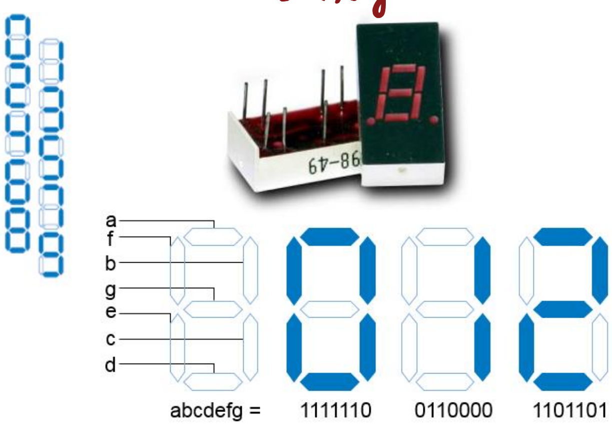
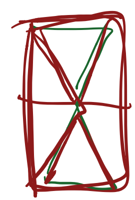
- **Step#1: Propose a way to represent hexadecimal number on ?-segment display.**

Way to represent decimal (0 ~ 9) number on 7-segment display	Way to represent hexadecimal (0 ~ F) number on ?-segment display
10진수를 표시하는 7seg	16진수를 표시하는 ?seg LED로 보이기. display 수가 적을수록 좋음 **Your proposal**



Hexadecimal Number
0
1
2
3
4
5
6
7
8
9
A
B
C
D
E
F



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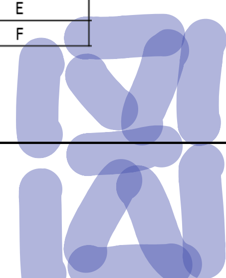

Hardware Design

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- **Step#2: Fill the below blank (?) with your definition based on your proposal.**

display

Hexadecimal Number	Input (4-bit)				Output (Your definition)			
	w	x	y	z	a	b	. . .	?
0	0	0	0	0	?	?	. . .	?
1	0	0	0	1	?	?	. . .	?
2	0	0	1	0	?	?	. . .	?
3	0	0	1	1	?	?	. . .	?
4	0	1	0	0	?	?	. . .	?
5	0	1	0	1	?	?	. . .	?
6	0	1	1	0	?	?	. . .	?
7	0	1	1	1	?	?	. . .	?
8	1	0	0	0	?	?	. . .	?
9	1	0	0	1	?	?	. . .	?
A	1	0	1	0	?	?	. . .	?
B	1	0	1	1	?	?	. . .	?
C	1	1	0	0	?	?	. . .	?
D	1	1	0	1	?	?	. . .	?
E	1	1	1	0	?	?	. . .	?
F	1	1	1	1	?	?	. . .	?

Hardware Design

- Digital circuit based on boolean algebra

- **Step#3: Design BCHD (Binary Coded HexaDecimal) to ? segment display decoder.**
  - Based on combinational logic design process

Hexadecimal Number	Input (4-bit)				Output (Your definition)			
	w	x	y	z	a	b	. . .	?
0	0	0	0	0	?	?	. . .	?
1	0	0	0	1	?	?	. . .	?
2	0	0	1	0	?	?	. . .	?
3	0	0	1	1	?	?	. . .	?
4	0	1	0	0	?	?	. . .	?
5	0	1	0	1	?	?	. . .	?
6	0	1	1	0	?	?	. . .	?
7	0	1	1	1	?	?	. . .	?
8	1	0	0	0	?	?	. . .	?
9	1	0	0	1	?	?	. . .	?
A	1	0	1	0	?	?	. . .	?
B	1	0	1	1	?	?	. . .	?
C	1	1	0	0	?	?	. . .	?
D	1	1	0	1	?	?	. . .	?
E	1	1	1	0	?	?	. . .	?
F	1	1	1	1	?	?	. . .	?

Combinational Logic Design Process

Step	Description
Step 1 **Capture** the function	Create a truth table or equations, whichever is most natural for the given problem, to describe the desired behavior of the combinational logic.
Step 2 **Convert** to equations	This step is only necessary if you captured the function using a truth table instead of equations. Create an equation for each output by ORing all the minterms – canonical form. Simplify the equations if desired.
Step 3 **Implement** as a gate-based circuit	For each output, create a circuit corresponding to the output's equation.

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output 하나씩 만들어보자.

- **Step#3: Design BCHD (Binary Coded HexaDecimal) to ? segment display decoder.**
  - For example

Output 'a'

Combinational logic design process

Step#1

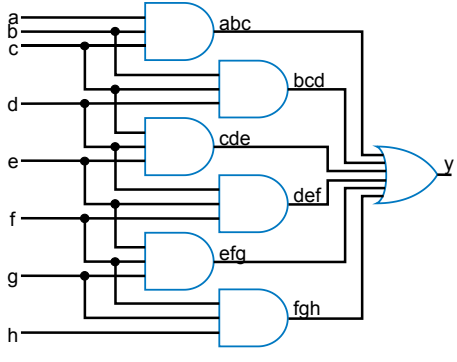
Hexadecimal Number	Input (4-bit)				
	w	x	y	z	a
0	0	0	0	0	?
1	0	0	0	1	?
2	0	0	1	0	?
3	0	0	1	1	?
4	0	1	0	0	?
5	0	1	0	1	?
6	0	1	1	0	?
7	0	1	1	1	?
8	1	0	0	0	?
9	1	0	0	1	?
A	1	0	1	0	?
B	1	0	1	1	?
C	1	1	0	0	?
D	1	1	0	1	?
E	1	1	1	0	?
F	1	1	1	1	?

Step#2

- Four Variables K-Maps
  - The initial canonical form A'B'C'D'+ A'B'C'D+ A'B'CD' + A'BC'D'+A'BC'D+ AB'C'D'+AB'CD'.
  - It is minimized to B'D' + A'C' .

AB \ CD	00	01	11	10
00	1	1		1
01	1	1		
11				
10	1			1

Step#3



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- **Step#4: Explain meaning of the designed BCHD (Binary Coded HexaDecimal) to ? segment display decoder.**
  - Based on the below flow

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