Invited Online Talk

Optimizing HPC System Software for Large-Scale Deep Learning

Xiaodong Yu

Time: Monday, 07/31/2023, 3:00 PM — 4:00 PM (CST)

Zoom Link: https://unt.zoom.us/j/85913977559

Abstract: The scale of the deep neural networks (DNN) and the training datasets keep rapidly expanding, in both AI-driven industrial and scientific applications. Although larger-scale deep learning consistently produces better results, it also costs significantly longer training time. Modern HPC platforms consist of thousands of computing nodes providing tremendous processing powers for training. However, scaling large-scale deep learning onto more nodes does not necessarily speed up the training, as the overall performance is gated by the support of system software.

In this talk, I will first demonstrate the benchmarking result of training scientific DNN models with large-scale datasets on multip-node multi-GPU platforms. The result indicates that, with the default I/O subsystem, data loading from the file systems can take up to 80% of the training time. It also shows the communication cost using the current MPI is very high since the messages to pass are huge. Both these two overheads significantly diminish the computing resource advantage of distributed training. Accordingly, I will present two designs and optimizations for system software to improve the overall training performance. One is a novel data-loading framework for CNN training called SOLAR, which can achieve up to 10.9X speedup compared to the loading relying only on the default I/O subsystem. The other is an ultrafast lossy compression utility, SZx, that can efficiently shrink the MPI message size with light overhead. SZx is up to 16X faster than the state-of-the-art lossy compression utilities and can reduce the communication cost of deep learning by a factor of 2. I will also introduce my ongoing work on emerging AI accelerators.

Bio: Dr. Xiaodong Yu is an assistant computer scientist in the Mathematics and Computer Science (MCS) division at Argonne National Laboratory. He is also a scientist at large through the Consortium for Advanced Science and Engineering (CASE) at the University of Chicago. His research interests broadly lie in parallel and distributed algorithms, systems, and architecture. He is the PI of a Laboratory Directed Research and Development (LDRD) project and the technical lead and senior personnel of three DOE-funded projects. He obtained his Ph.D. in Computer Science from Virginia Tech in 2019. His research works have been published in multiple top-tier HPC conferences, including HPDC, ICS, and IPDPS. He has served as a member of the organizing committee and the technical program committee for conferences, including ISPASS, SiPS, SC, HotI, and HPCC. He is also a member of the TPDS review board.