EE2026: DIGITAL DESIGN

Academic Year 2020-2021, Semester 2

LAB 4: Sequential Circuits in Verilog - Part 2

OVERVIEW

This lab is a continuation of Lab 3. In this Lab 4, more applications of sequential circuits will be explored, and this will be the last lab practice before the EE2026 project.

The pre-requisites for this lab are:

- Knowing how to obtain slower clock frequencies from a faster one.
- Brief understanding of the purpose of a D-Flip-Flop (D-FF) in a sequential circuit.

This lab will cover the following:

- Schematic and design of a single pulse circuit, by using two D-FFs with a clock signal.
- Schematic and design of a debounced single pulse circuit, by using two D-FFs with a slow clock signal.
- Incrementing a counter value by 1 when a pushbutton is pressed.
- Multiplying a counter value by 2 when a pushbutton is pressed.

Tasks for this lab include:

- Simulating a single pulse circuit, whereby the D-FFs use a 100 MHz clock.
- Implementing a debounced single pulse circuit, by using a 3 Hz clock, on the Bays 3 development board.
- Observing patterns on the physical LED array, through counters that use the debounced single pulse signal.

GRADED ASSIGNMENT [LUMINUS SUBMISSION: MONDAY 15th MARCH 2021, NOON]:

This is the final lab assignment to test whether you have properly mastered the technical contents from your three previous lab assignments. In this lab 4 assignment, the focus will be more on logic.

You are encouraged to complete this assignment before the start of Week 8 (Monday 8th March 2021), as the focus will be on the EE2026 project from there on.

Further details are available at the end of this lab manual.

CREATING A SINGLE PULSE OUTPUT

In this section, a single pulse output circuit will be created. The circuit from *Figure 4.1*, consisting of two D-FFs and an AND gate, can be used to generate a single pulse output signal. The latter will be a synchronised logic true signal that lasts for the duration of one clock cycle.

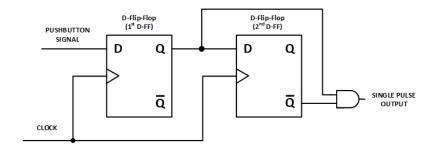


Figure 4.1: Single pulse circuit

The waveform for the single pulse circuit is as shown in Figure 4.2

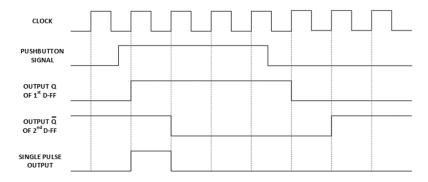


Figure 4.2: Waveform from a single pulse circuit

UNDERSTANDING | TASK 1

Through behavioural modelling in Verilog, the code for a positive-edge triggered D-flip-flop can be created:

Verilog code for a positive-edge triggered D-flip-flop

```
module my_dff(input DFF_CLOCK, D, output reg Q = 0);
    always @ (posedge DFF_CLOCK) begin
        Q <= D;
end</pre>
```

endmodule

Using structural, dataflow and/or behavioural modelling, create the Verilog design for the circuit shown in *Figure 4.1*. Create the simulation for the single pulse design module, with a simulated 100 MHz clock and appropriate stimuli, to confirm that a single pulse can be obtained. Take note of the time scale in the simulation window, and determine the duration of the single pulse output.

CREATING A DEBOUNCED SINGLE PULSE OUTPUT [THINK HOW TO DO THIS BEFORE THE LAB!]

On a physical device, the single pulse circuit can also be used to debounce mechanical switch signals. A slower clock, whose time period is longer than the bouncing of the switch signal, is required. Feeding this slower clock signal to the two D-FFs of a single pulse circuit will create a debounced single pulse output, as illustrated in *Figure 4.3*

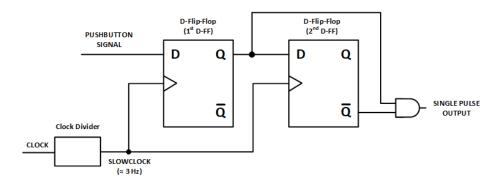


Figure 4.3: Debounced single pulse circuit

The waveform for the debounced single pulse circuit is as shown in Figure 4.4

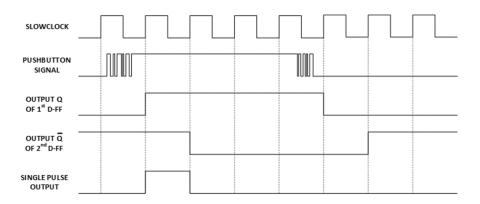


Figure 4.4: Waveform from a debounced single pulse circuit

UNDERSTANDING | TASK 2

Implement the circuit in *Figure 4.3* on the Basys 3 development board, by linking the debounced single pulse output to an LED. Press and hold the pushbutton to see if a single pulse of 1 clock cycle is obtained.

How much of simulated time would be required in order to see the single pulse output in the simulation waveform window?

Can you think of other ways of implementing a debounced single pulse output?

APPLYING THE DEBOUNCED SINGLE PULSE

From UNDERSTANDING | TASK 2, it is noted that no matter how long the pushbutton is pressed and held, a single synchronous pulse of only one clock cycle is created. This allows for the creation of a counter whose value can be made to increase by 1 each time a pushbutton is pressed, as such press would result in a positive edge of a single pulse.

UNDERSTANDING | TASK 3

Design an 8-bit counter that makes use of the debounced single pulse output, in order to increase its value by 1 each time the pushbutton is pressed, and for no matter how long the pushbutton is held. Implement the design on the Basys 3 development board, and observe how the physical LED array pattern changes whenever the pushbutton is pressed (and optionally held for a long time). Consider using the code below to detect the rising edge of the single pulse signal:

Partial Verilog code for a count that increments by one at the positive edge of the synchronised single pulse signal

```
// Initialise the initial 8-bit counter value to 8'b0000_0000
always @ (posedge SLOWCLOCK) begin
    if (SINGLE_PULSE_OUTPUT == 1) begin
        my_counter <= my_counter + 1;
    end
end</pre>
```

Important: The clock used in the sensitivity list must be exactly the same clock that was used to create the single pulse output

UNDERSTANDING | TASK 4

Shifting the values in a register to the left multiplies the register value by the base value. Create another design for a 16-bit counter, whereby pressing the pushbutton multiplies the value by 2 (Binary / Base-2 system). Implement the design on the Basys 3 development board. You may use the Verilog code template given below:

Partial Verilog code for a count that multiplies by 2 at the positive edge of the synchronised single pulse signal

```
// Initialise the initial 16-bit counter value to 16'h000C;
always @ (posedge SLOWCLOCK) begin
    if (SINGLE_PULSE_OUTPUT == 1) begin
        my_counter <= my_counter << 1;
    end
end</pre>
```

Record the values that you see from the LED array in the table below:

	Value from the Physical LED Array	Unsigned Decimal
Original Value	0000 0000 0000 1100	12
1 st Pushbutton Press		
2 nd Pushbutton Press		
3 rd Pushbutton Press		
4 th Pushbutton Press		
5 th Pushbutton Press		
6 th Pushbutton Press		

What kind of pattern do you notice in the values?

What happens for pushbutton presses after the 13th and 14th ones?

UNDERSTANDING | TASK 5

Change your SLOWCLOCK to a 12 Hz clock. What do you notice when the pushbutton is pressed for the counter?

Change your SLOWCLOCK to a 25 MHz clock? What do you notice when the pushbutton is pressed for the counter?

GRADED POST-LAB ASSIGNMENT

Complete as much as possible, **in one working bitstream**, within the given deadline. It is much better to have a working program with some completed functionalities, instead of submitting a program without a working bitstream.

You may need a few of the operators listed below for the assignment (as well as for the upcoming EE2026 project):

	Bitwise Operators		
~	~m	invert each bit of m	
&	m & n	AND each bit of m with each bit of n	
	m n	OR each bit of m with each bit of n	
٨	m ^ n	exclusive-OR each bit of m with n	
~^ or ^~	m ~^ n	exclusive-NOR each bit of m with n	
<<	m << n	shift m left n-times and fill with zeros	
>>	m >> n	shift m right n-times and fill with zeros	
Unary Reduction Operators			
&	&m	AND all bits in m together (1-bit result)	
~&	~ & m	NAND all bits in m together (1-bit result)	
	m	OR all bits in m together (1-bit result)	
~	~ m	NOR all bits in m together (1-bit result)	
۸	^m	exclusive-OR all bits in m (1-bit result)	
~^ or ^~	~^m	exclusive-NOR all bits in m (1-bit result)	
		Logical Operators	
!	! m	is m not true? (1-bit True/False result)	
&&	m && n	are both m and n true? (1-bit True/False result)	
	m n	are either m or n true? (1-bit True/False result)	
Equalit	y and Rela	tional Operators (return X if an operand has X or Z)	
==	m == n	is m equal to n? (1-bit True/False result)	
!=	m != n	is m not equal to n? (1-bit True/False result)	
<	m < n	is m less than n? (1-bit True/False result)	
>	m > n	is m greater than n? (1-bit True/False result)	
<=	m <= n	is m less than or equal to n? (1-bit True/False result)	
>=	m >= n	is m greater than or equal to n? (1-bit True/False result)	
	Identity O	perators (compare logic values 0, 1, X, and Z)	
===	m === n	is m identical to n? (1-bit True/False results)	
!==	m !== n	is m not identical to n? (1-bit True/False result)	
		Miscellaneous Operators	
?:	sel?m:n	conditional operator; if sel is true, return m: else return n	
{}	{m,n}	concatenate m to n, creating a larger vector	
{{}}	{n{ }}	replicate inner concatenation n-times	
->	-> m	trigger an event on an event data type	

Arithmetic Operators		
+	m + n	add n to m
-	m - n	subtract n from m
-	-m	negate m (2's complement)
*	m * n	multiply m by n
/	m / n	divide m by n
%	m % n	modulus of m / n
**	m ** n	m to the power n (new in Verilog-2001)
<<<	m <<< n	shift m left n-times, filling with 0 (new in Verilog-2001)
>>>	m >>> n	shift m right n-times; fill with value of sign bit if expression is signed, otherwise fill with 0 (Verilog-2001)

It is required to complete and fully understand all the five UNDERSTANDING | TASK before starting this assignment. The accuracy and responsiveness of the pushbuttons will be tested. High accuracy and high responsiveness are required.

SUB-SYSTEM A [Secured Access Fingerprint Entry]

Before the start of your program, switches SW0 to SW15 are OFF. When the program starts, LD0 to LD15 are OFF, and the seven segment displays do not show any characters (All 7 segments and decimal point segment are off).

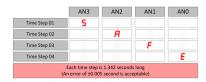
The user is then allowed to scan a fingerprint by pressing and holding the centre pushbutton (BTNC) on the Basys 3 development board. While BTNC is being held, it is required to light up the 16 LEDs in increasing order (from LD0 to LD15), with each additional LED turning ON at a time interval, t_{on} . The latter is dependent on the **4**th **rightmost numerical value** of your student matriculation number, and as indicated in **Table A**.

4th (Fourth) rightmost numerical value of your student matriculation number	Time interval to turn ON additional led, t_{on} (A max error of ± 0.01 second is acceptable)
0 or 3 or 6 or 9	0.168 second
1 or 4 or 7	0.336 second
2 or 5 or 8	0.671 second

Table A

If the user releases BTNC before LD15 is turned ON, all leds should turn OFF, and the user can restart the fingerprint scanning process again from beginning.

When LD0 to LD15 are all ON, but the user does not release BTNC, nothing else should happen. Following that, when the user releases BTNC, it is required to clearly observe the following sequence of 4 characters on specific seven-segment displays at the specified time steps (Each time step is 1.342 seconds long):



After Time Step 04 has shown the character "E", it is required to be able to clearly observe the following:



The word "SAFE" indicates that the fingerprint scan is successful. For the next 5.37 seconds, "SAFE" will remain being display. After that 5.37 seconds are over, the seven segment displays should be replaced with the four rightmost numerical value of your student matriculation number. For example, if a student has matriculation number A0123456Y, then the following should be seen:



When that 4 digits number is being displayed, the user can now physically open the doors to the rooms of a certain Digital Electronics Lab. This is done by manually turning ON SW3, SW2, SW1 and SW0 on the Basys 3 development board. Assume that the user will not turn ON/OFF the switches before that 4 digits number is being displayed on the seven segment displays.

Switching ON/OFF these switches (SW3 to SW0) has another effect in this SAFE sub-system only, as described below:

- Turning ON SW3 will turn off the segments of AN3
- Turning ON SW2 will turn off the segments of AN2
- Turning ON SW1 will turn off the segments of AN1
- > Turning ON SW0 will turn off the segments of AN0
- > Turning OFF SW3 will show the 4th rightmost numerical value of your student matriculation number
- > Turning OFF SW2 will show the 3rd rightmost numerical value of your student matriculation number
- Turning OFF SW1 will show the 2nd rightmost numerical value of your student matriculation number
- > Turning OFF SW0 will show the 1st rightmost numerical value of your student matriculation number

The DISTANCE sub-system is triggered when the four switches from SW0 to SW3 are simultaneously ON. The user will not toggle any of these switches in the DISTANCE sub-system.

SUB-SYSTEM B [Digital Integrated System for Transgression in Admittance and Notifications for Crowded Environments]

At the start of this DISTANCE sub-system, AN3 to AN1 will not show anything.

ANO must show $n_{chances}$, which is dependent on the 1st rightmost numerical value of your student matriculation number, and as indicated in Table B.

1st (First) rightmost numerical value of your student matriculation number	n _{chances} at beginning of DISTANCE (Hexadecimal value)	penalty _{crowding} (Decimal value. If rule (4) is broken)
0	6	2
1	7	4
2	8	3
3	9	6
4	A	6
5	Ь	8
6	E	7
7	4	9
8	E	8
9	F	9

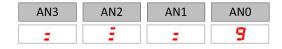
Table B

Throughout this DISTANCE sub-system, it is ALWAYS possible to fully reset the state to the very beginning of this DISTANCE subsystem by pressing and immediately releasing the up pushbutton (BTNU) on the Basys 3 development board.

In this DISTANCE sub-system, AN3 to AN1 represent separate rooms in the Digital Electronics Lab. Whenever a person enters the room, one additional horizontal bar is to be lit up, up to a maximum of 3 horizontal bars. The following actions indicate that a person is entering a room:

BTNL (Left pushbutton): One additional person is entering room AN3
BTNC (Centre pushbutton): One additional person is entering room AN2
BTNR (Right pushbutton): One additional person is entering room AN1

An example is shown below, with 2 persons inside room AN3, 3 persons inside room AN2, and 2 persons inside room AN1:



ANO is the $n_{chances}$ value indicated previously in Table B

Following the law regarding the COVID-19 safe management practices in preventing overcrowding, and to distribute the amount of people inside the rooms evenly, this DISTANCE subsystem must work based on the following rules:

- (1) A person can only enter a room if the difference in number of persons inside the room will not be more than 1 (Difference can be 1) after entering the room, when compared to the other rooms
- (2) No two persons can enter the same room one after the other
- (3) The safe capacity of any room is 3 persons. If an additional person is trying to enter, it should be counted as breaching the rule, and the person will automatically be removed from the room immediately (This extra person will not be shown on the seven segments)
- (4) People must be able to enter the rooms quickly. The worst scenario of having to fill in 9 people within 2.68 seconds to prevent overcrowding outside the rooms is required. Therefore, as soon as this DISTANCE sub-system is entered, if 9 persons have not entered the rooms within 3.00 seconds (An error of ±0.25 second is acceptable), the value of ANO must decrease by *penaltycrowding*. This rule only happens once each time this DISTANCE sub-system is entered or reset (When BTNU is pressed and released). This rule is even active during the cooldown period if the latter is currently in progress

Each time any of the above rules numbered (1), (2) and (3) are broken, ANO must decrease its current value by 1, to indicate the amount of chances left before severe action is taken. Also, whenever any of the rules (1), (2) and (3) are broken, there is a cooldown period of 10.74 seconds (An error of ±0.25 second is acceptable). During the cooldown period, the following happens:

- The room where the person was trying to enter should create a notification. This will be in the form of the horizontal bars(s) in that specific room blinking. The blinking frequency should be 1.49 Hz
- No persons will be allowed in any of the rooms until the blinking notification has stopped. In other words, none of these pushbuttons should work: BTNL, BTNC, BTNR

If ANO reaches a value of 0 (The value of 0 will not be seen), the following message appears on the seven segments display:



No further observations are required when "FAIL" is shown on the seven segments, as the program ends there. However, remember that throughout this DISTANCE sub-system, including after seeing the word "FAIL", it is ALWAYS possible to fully reset the state to the very beginning of this DISTANCE sub-system by pressing and immediately releasing the up pushbutton (BTNU).

Be reminded to turn OFF switches SW15 to SW0 if you need to reload the bitstream for this SAFE-DISTANCE.

LUMINUS SUBMISSION INSTRUCTIONS

- Complete as much required functionalities <u>as possible within the given deadline</u>, and ensure that your bitstream has been successfully generated and tested on your Basys 3 development board <u>BEFORE</u> archiving your Vivado workspace for LumiNUS upload. No working bitstream is equivalent to no marks (It is best to have some working functionalities / requirements, instead of not having any bitstream at all while trying all requirements)
- It is compulsory to archive your project in a compressed form without any simulation waveforms. In the uploaded archive, the codes (.v files) are important, not the waveforms (.wdb files). The archive size should not exceed 4 MB in size for lab 4. Follow the instructions given in the pdf: "Archive Project in Vivado 2018.02"
- <u>After</u> following the instructions in "Archive Project in Vivado 2018.02", rename your project archive as indicated in the appendix of this lab manual
- There are no report submissions for this lab assignment
- Upload to LumiNUS EE2026 -> Files -> Lab and Project Materials and Submissions -> Lab 4 Submission
- Download your LumiNUS archive after uploading. Click and drag the single folder within that archive to desktop, and then open the Vivado project in that extracted folder to see if it can be opened. Check if you can also run your bitstream correctly. No project files and no working bitstream is equivalent to losing all marks
- The LumiNUS upload must be completed by Monday 15th March 2021, 12:00 P.M. (Noon). Do not plan to upload during the
 grace period of 2 hours
- Late submissions for lab 4 are not accepted. Complete as much required functionalities as possible within the given deadline and in one working program

Plagiarism is penalised with a 100% penalty for all SOURCES and RECIPIENTS

All past and future submissions, and marks, will be reviewed in greater detail, for any person found to have plagiarised

REMEMBER TO NAME YOUR SUBMISSION IN THE REQUIRED FORMAT

ALL THE SUBMISSION INSTRUCTIONS LISTED ABOVE WILL AFFECT YOUR GRADES!

APPENDIX (COMPULSORY renaming before just LumiNUS upload):

It is **compulsory to rename your project archive**, just before the LumiNUS upload, as listed in the table below. Do not change any other part of the naming. Simply **copy** the naming from the table below, and **paste** it while renaming your project archive. Penalties will be incurred if your submission cannot be found according to the exact naming template below.

Name	Archive Naming
Aaron Chan Siang Joo	L4_Tue_PM_Aaron Chan Siang Joo_426_Archive
Aditi Chadha	L4_Tue_AM_Aditi Chadha_898_Archive
Aiden Thaw @ Aung Kham Thaw	L4_Tue_PM_Aiden Thaw Aung Kham Th_186_Archive
Alvin Lim Jun	L4 Tue AM Alvin Lim Jun 284 Archive L4 Mon PM Alvin Pang Zi Xiong 475 Archive
Alvin Pang Zi Xiong Ameer Khalid	L4 Tue PM Ameer Khalid 328 Archive
Anderson Leong Ke Sheng	L4 Tue PM Anderson Leong Ke Sheng 152 Archive
Andy Chua Xun Ze	L4 Tue PM Andy Chua Xun Ze 384 Archive
ANG JIA JUN, DARYL	L4 Tue PM ANG JIA JUN DARYL 485 Archive
Ang Qi Xuan	L4 Mon PM Ang Qi Xuan 052 Archive
Ang Yong Siang Alwin	L4 Tue AM Ang Yong Siang Alwin 771 Archive
Anna Zhang Runyu	L4 Tue PM Anna Zhang Runyu 999 Archive
Antriksh Verma	L4 Tue AM Antriksh Verma 149 Archive
Anvitha Rajaram	L4_Tue_AM_Anvitha Rajaram_434_Archive
Ariel Ong Xing Er	L4_Tue_PM_Ariel Ong Xing Er_560_Archive
Bellakka Krishnamurthy Prajwal	L4_Tue_AM_Bellakka Krishnamurthy Pr_862_Archive
Boo Qian Wei, Adeline	L4_Tue_AM_Boo Qian Wei Adeline_207_Archive
Braden Teo Wei Ren	L4_Tue_AM_Braden Teo Wei Ren_238_Archive
Brendan Lau Siew Zhi	L4_Tue_AM_Brendan Lau Siew Zhi_596_Archive
Bryan Elmer Mulijono	L4_Tue_AM_Bryan Elmer Mulijono_447_Archive
Bryan Wong Hong Liang	L4_Tue_AM_Bryan Wong Hong Liang_051_Archive
Bui Quang Huy	L4_Tue_PM_Bui Quang Huy_362_Archive
Chai Zong Lun	L4_Tue_AM_Chai Zong Lun_784_Archive
Chan Keng Jit	L4_Tue_AM_Chan Keng Jit_501_Archive
Chan Yew Kun	L4_Tue_PM_Chan Yew Kun_985_Archive
Chan Zhao Yong	L4_Thu_PM_Chan Zhao Yong_518_Archive
Chan Zhi Jie Ryan	L4 Tue PM Chan Zhi Jie Ryan 415 Archive
Chen Hsin	L4 Tue PM Chen Hsin 602 Archive
CHEN SILIN	L4_Tue_AM_CHEN_SILIN_445_Archive
CHEN YUHAN	L4 Tue PM CHEN YUHAN 520 Archive
Cheng Siyuan Chew Yi Jie	L4 Tue AM Cheng Siyuan_728_Archive L4 Tue AM Chew Yi Jie 632 Archive
Chia Shao Xian	L4 Wed PM Chia Shao Xian 447 Archive
Chong Jia An	L4 Tue PM Chong Jia An 190 Archive
Chong Xuan Liang	L4 Thu AM Chong Xuan Liang 171 Archive
Christopher Nge Jing Qi	L4 Thu AM Christopher Nge Jing Qi 145 Archive
Christopher Tze-Wen Langton	L4 Thu AM Christopher TzeWen Langt 265 Archive
CHUA WAN NING	L4 Tue PM CHUA WAN NING 189 Archive
Chua Xiong Wei	L4 Thu AM Chua Xiong Wei 484 Archive
Chun Min Gyu	L4 Wed PM Chun Min Gyu 249 Archive
Chung Ying Qiao Winnie	L4 Tue PM Chung Ying Qiao Winnie 324 Archive
Conrad Ephraim Wee Cher Jae	L4 Thu AM Conrad Ephraim Wee Cher J 123 Archive
Cordell Chan Yi Hng	L4 Tue PM Cordell Chan Yi Hng 253 Archive
CUI MINJING	L4_Thu_AM_CUI MINJING_441_Archive
Cui Xinyu	L4_Tue_PM_Cui Xinyu_116_Archive
Damien Lim Yu Hao	L4_Thu_AM_Damien Lim Yu Hao_933_Archive
Darren Khoo Kah Weng	L4_Thu_AM_Darren Khoo Kah Weng_516_Archive
Darryl See	L4_Tue_PM_Darryl See_317_Archive
Desmond Eng Kian Wee	L4_Wed_PM_Desmond Eng Kian Wee_095_Archive
Donovan Sim Jing Yi	L4_Tue_PM_Donovan Sim Jing Yi_402_Archive
Du Yantang	L4_Tue_PM_Du Yantang_744_Archive
Edly Irsyad B Elham	L4_Thu_AM_Edly Irsyad B Elham_555_Archive
Elumalai Oviya Dharshini	L4_Thu_AM_Elumalai Oviya Dharshini_353_Archive
Eric Bryan	L4 Thu AM Eric Bryan 789 Archive
Eugene Chong Zhi Liang	L4_Thu_AM_Eugene Chong Zhi Liang_525_Archive
Fan Shixi	L4 Thu AM FOONC VIN VI 018 Archive
FOONG XIN YU Fu Zhehui	L4_Thu_AM_FOONG_XIN_YU_018_Archive
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GOH SHAU HUI GEORGE	L4 Tue PM GOH SHAU HUI GEORGE 353 Archive
Goh Wei Yang	L4 Tue PM Goh Wei Yang 254 Archive
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Hoang Trong Tan	L4_Thu_AM_Hoang Trong Tan_425_Archive
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Hong Xingwen	L4_Tue_PM_Hong_Xingwen_861_Archive
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Huang Che Yen	L4 Thu AM Huang Che Yen 597 Archive
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Khoo Jia Le Isaac	L4_Thu_AM_Khoo Jia Le Isaac_733_Archive
Khor Sheng Hou	L4_Thu_PM_Khor Sheng Hou_443_Archive
Kishor Kumar Haribaskar	L4_Thu_AM_Kishor Kumar Haribaskar_481_Archive
Koh Meng Kiat, Kenneth	L4_Tue_AM_Koh Meng Kiat Kenneth_512_Archive
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YIP WAYNE YU HAIHONG Yue Junfeng Yuk Yeon Soo Zeng Jiexiong ZHANG HAOYU ZHAO LUOYUANG Zhao Yibo Zhao Ziqi	L4 Wed PM YU HAIHONG 470 Archive L4 Thu AM_Yue Junfeng 802 Archive L4 Wed PM Yuk Yeon Soo 243 Archive L4 Mon_PM Zeng Jiexiong 052 Archive L4 Thu AM_ZHANG HAOYU 783 Archive L4 Mon_PM ZHAO LUOYUANG 466 Archive L4 Wed_PM Zhao Yibo_863 Archive L4 Wed_PM Zhao Ziqi_275 Archive
YIP WAYNE YU HAIHONG Yue Junfeng Yuk Yeon Soo Zeng Jiexiong ZHANG HAOYU ZHAO LUOYUANG Zhao Yibo Zhao Ziqi ZHONG XINGHAN	L4 Wed PM YU HAIHONG 470 Archive L4 Thu AM_Yue Junfeng 802 Archive L4 Wed PM Yuk Yeon Soo 243 Archive L4 Mon PM Zeng Jiexiong 052 Archive L4 Thu AM_ZHANG HAOYU 783 Archive L4 Mon PM ZHAO LUOYUANG 466 Archive L4 Wed PM Zhao Yibo 863 Archive L4 Wed PM Zhao Ziqi 275 Archive L4 Mon PM ZHONG XINGHAN 468 Archive
YIP WAYNE YU HAIHONG Yue Junfeng Yuk Yeon Soo Zeng Jiexiong ZHANG HAOYU ZHAO LUOYUANG Zhao Yibo Zhao Ziqi ZHONG XINGHAN ZHOU CHENGXU	L4 Wed PM YU HAIHONG 470 Archive L4 Thu AM Yue Junfeng 802 Archive L4 Wed PM Yuk Yeon Soo 243 Archive L4 Mon PM Zeng Jiexiong 052 Archive L4 Thu AM ZHANG HAOYU 783 Archive L4 Mon PM ZHANG HAOYU 783 Archive L4 Mon PM ZHAO LUOYUANG 466 Archive L4 Wed PM Zhao Yibo 863 Archive L4 Wed PM Zhao Ziqi 275 Archive L4 Mon PM ZHONG XINGHAN 468 Archive L4 Mon PM ZHONG XINGHAN 468 Archive L4 Mon PM ZHOU CHENGXU 492 Archive
YIP WAYNE YU HAIHONG Yue Junfeng Yuk Yeon Soo Zeng Jiexiong ZHANG HAOYU ZHAO LUOYUANG Zhao Yibo Zhao Ziqi ZHONG XINGHAN ZHOU CHENGXU ZHOU YUHAN	L4 Wed PM YU HAIHONG 470 Archive L4 Thu AM_Yue Junfeng 802 Archive L4 Wed PM Yuk Yeon Soo 243 Archive L4 Mon PM Zeng Jiexiong 052 Archive L4 Mon PM ZHANG HAOVU 783 Archive L4 Mon PM_ZHANG HAOVU 783 Archive L4 Mon PM_ZHAO LUOYUANG 466 Archive L4 Wed PM_Zhao Yibo 863 Archive L4 Wed PM_Zhao Ziqi 275 Archive L4 Mon PM_ZHONG XINGHAN 468 Archive L4 Mon PM_ZHOU CHENGXU 492 Archive L4 Wed PM_ZHOU CHENGXU 492 Archive L4 Wed PM_ZHOU YUHAN 530 Archive
YIP WAYNE YU HAIHONG Yue Junfeng Yuk Yeon Soo Zeng Jiexiong ZHANG HAOYU ZHAO LUOYUANG Zhao Yibo Zhao Ziqi ZHONG XINGHAN ZHOU CHENGXU	L4 Wed PM YU HAIHONG 470 Archive L4 Thu AM Yue Junfeng 802 Archive L4 Wed PM Yuk Yeon Soo 243 Archive L4 Mon PM Zeng Jiexiong 052 Archive L4 Thu AM ZHANG HAOYU 783 Archive L4 Mon PM ZHANG HAOYU 783 Archive L4 Mon PM ZHAO LUOYUANG 466 Archive L4 Wed PM Zhao Yibo 863 Archive L4 Wed PM Zhao Ziqi 275 Archive L4 Mon PM ZHONG XINGHAN 468 Archive L4 Mon PM ZHONG XINGHAN 468 Archive L4 Mon PM ZHOU CHENGXU 492 Archive