

EE2026: DIGITAL DESIGN

Academic Year 2020-2021, Semester 2

LAB 2: Combinational Circuits in Verilog

OVERVIEW:

A combinational circuit is one where the outputs depend only on the current inputs. In this lab, we will be designing some combinational circuits that are able to perform addition.

The pre-requisite for this lab requires one to be able to:

- Create a Verilog project and design source in Vivado.
- Create a testbench to simulate the design source.
- Generate the RTL schematic and the synthesised circuit schematic of design source.
- Map and implement a design on the Basys 3 development board.
- Understand well the contents of Lectures 1, 2, and especially 3: Introduction to Verilog.

This lab will cover the following:

- Designing a one-bit full adder circuit using the dataflow modelling method.
- Designing a two-bit parallel adder circuit using the structural modelling method.

Tasks for this lab include:

- Designing the Verilog code of a one-bit full adder.
- Designing, simulating and implementing a four-bit parallel adder on the FPGA.
- Understanding a 1-bit two-to-one multiplexer that can be used in the graded post-lab assignment.

GRADED ASSIGNMENT [LUMINUS SUBMISSION: MONDAY 15th FEBRUARY 2021, NOON]:

- Designing, simulating and implementing an n-bit subtractor with overflow detection, on the Basys 3 development board

Further details are available at the end of this lab manual

ONE-BIT-FULL ADDER:

Consider the binary addition shown in **Figure 2.1**. To design a circuit that would perform the addition of two one-bit values, the circuit would need to have three input bits and two output bits.



Figure 2.1: Binary Addition and functional block diagram of the one-bit full adder

Such a circuit is called a one-bit full adder. It adds two bits (**A**, **B**) and the carry (**C_{in}**) from a previous stage of addition, and produces a sum (**S**) and a carry (**C_{out}**), as illustrated through a truth table in **Figure 2.2**. By simplifying the truth table, the Boolean expressions for **S** and **C_{out}** can be obtained.

A	B	C _{in}	S	C _{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$S = A \oplus B \oplus C_{in}$$

$$C_{out} = AB + C_{in} (A \oplus B)$$

Figure 2.2: Truth table and boolean expressions of the one-bit full adder

Note: A half adder, in contrast to a full adder, does not involve a carry input. Thus, for a half adder, $S = A \oplus B$, and $C_{out} = AB$

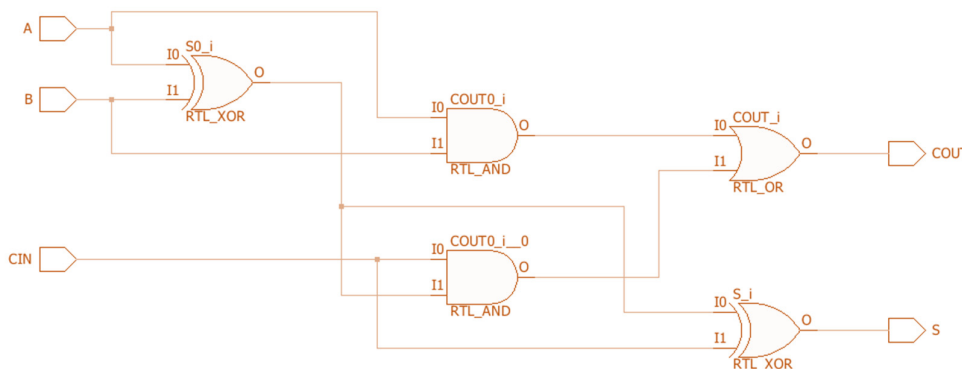
UNDERSTANDING | TASK 1

Using the dataflow method, complete the Verilog code for the one-bit full adder. Verify that the RTL schematic is as shown.

Verilog skeleton code for the one-bit-full adder:

```
module my_full_adder(input A, B, CIN, output S, COUT);
    assign S =
    assign COUT =
endmodule
```

RTL schematic for the one-bit full adder:



TWO-BIT FULL ADDER:

By cascading one-bit full adder blocks, the one-bit adder can be reused and parallel adders that add multiple bits can be created through the structural modelling method. A two-bit ripple-carry adder is illustrated in *Figure 2.3*.

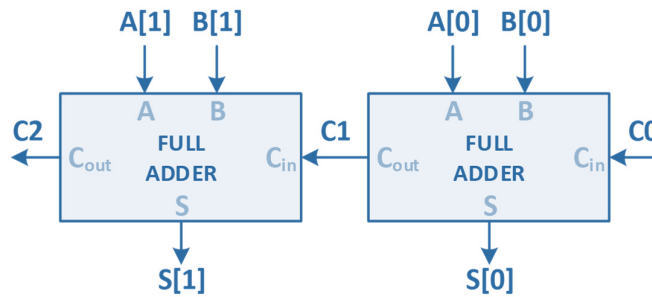


Figure 2.3: Functional block diagram of the two-bit ripple-carry adder

With the code for a one-bit full adder, a new module is created and two full adder blocks (fa0, fa1) are instantiated. By specifying the inputs and outputs to these blocks, the connection **C1** between them is made. Note that the order of signals during instantiation should respect the order in which they were declared in the one-bit full adder module **my_full_adder**.

This approach to hardware description is called structural modelling, whereby a more abstract module (for example, **my_2_bit_adder**) is built from simpler components describing gate-level hardware (such as **my_full_adder**).

Verilog code for two-bit ripple-carry adder, using structural modelling:

```
module my_2_bit_adder(input [1:0] A, input [1:0] B, input C0,
                    output [1:0] S, output C2);

    wire C1;

    my_full_adder fa0 (A[0], B[0], C0, S[0], C1);
    my_full_adder fa1 (A[1], B[1], C1, S[1], C2);

endmodule
```

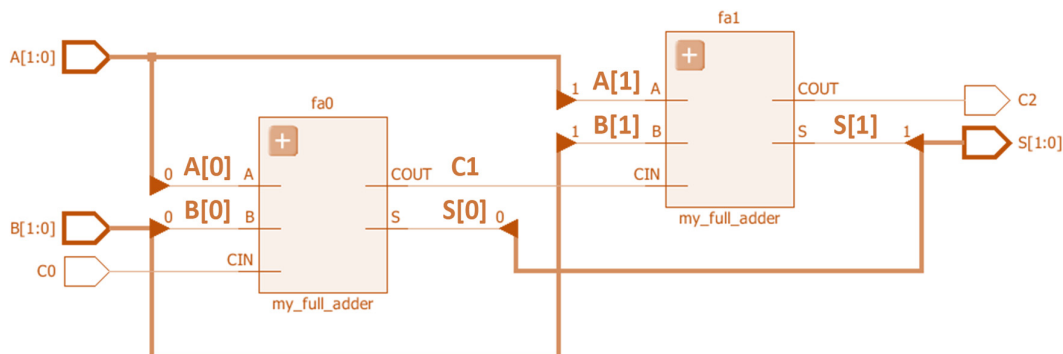
[Note] Two-bit port declaration for A, B, S:

Instead of having multiple input and output ports (A1, A0, B1, B0, S1, S0), multi-bit vector ports are defined.

Example: `input [5:0] apple`

Input port name is **apple**, with size of 6 bits. apple[5] refers to the MSB, apple[0] refers to the LSB.

RTL schematic for the two-bit ripple-carry adder:



FOUR-BIT FULL ADDER:

The functional block diagram of a four-bit ripple-carry adder is shown in *Figure 2.4*.

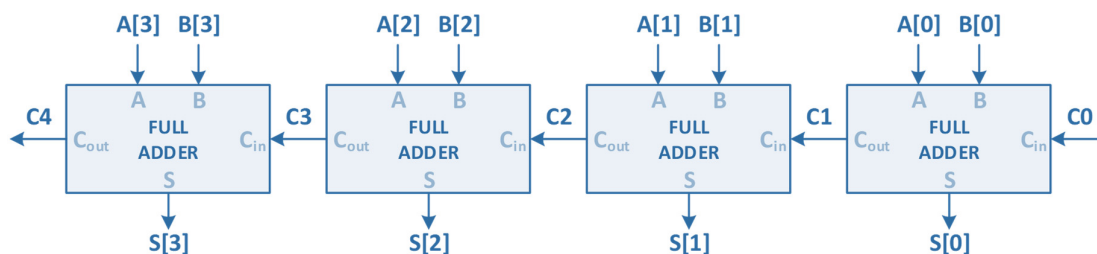


Figure 2.4: Functional block diagram of a four-bit ripple-carry adder

UNDERSTANDING | TASK 2

Start by adding a new design source for the four-bit full adder.

1. By using the structural modelling method, design a four-bit ripple-carry adder.
2. Generate the RTL schematic and check that connections between the blocks are correct.
3. Simulate your code with the following three sets of input values, and check that the simulation outputs are correct:

$$\begin{array}{r} A: \quad 0 \ 0 \ 1 \ 1 \\ B: + \ 0 \ 0 \ 1 \ 1 \\ \hline \square \ \square \ \square \ \square \end{array}$$

$$\begin{array}{r} A: \quad 1 \ 0 \ 1 \ 1 \\ B: + \ 0 \ 1 \ 1 \ 1 \\ \hline \square \ \square \ \square \ \square \end{array}$$

$$\begin{array}{r} A: \quad 1 \ 1 \ 1 \ 1 \\ B: + \ 1 \ 1 \ 1 \ 1 \\ \hline \square \ \square \ \square \ \square \end{array}$$

[Note] Brief guidelines for multi-bit vector ports in the testbench:

- The port size should be indicated when declaring the signals. Inputs to the module being tested are declared using **reg**, whereas outputs from the module being tested are declared using **wire**:
`reg [3:0] A; wire [3:0] S;`
- The parameters for the module being tested do not need the port size of the signals:
`my_4_bit_adder module_alias (A, B, CARRY_IN, S, CARRY_OUT);`
- The testbench stimuli for multi-bit vector ports can be written as:
`A = 4'b0011; B = 4'b0011; CARRY_IN = 1'b0;`

4. Synthesise and implement your code on the FPGA, using appropriate switches and LEDs on the Basys 3 development board to represent the inputs and outputs.

This task is considered completed and understood if you have the following items related to the four-bit full adder:

- The RTL schematic of your design (item 2 of this task)
- The simulation waveform results of the three testbench stimuli (item 3 of this task)
- The four-bit ripple-carry adder on the Basys 3 development board (item 4 of this task)

UNDERSTANDING | TASK 3

Instead of using four one-bit adder blocks, can you think of an alternative way (still using structural modelling) in creating the four-bit ripple-carry adder? Consider doing the same things as indicated in **UNDERSTANDING | TASK 2** by using such alternative way. This task is meant as practice for you to improve your Vivado skills and Verilog understanding, and will not be explained.

1-BIT TWO-TO-ONE MULTIPLEXER (POST-LAB NON-GRADED – NO SUBMISSION FOR THIS):

A multiplexer (MUX) is a combinational circuit that connects one of its input signals to the output, based on the control signal. A simple 1-bit two-to-one mux, with inputs **A**, **B**, control signal **S**, and output **Z**, is illustrated as a functional block diagram, together with its simplified truth table, in **Figure 2.5**.

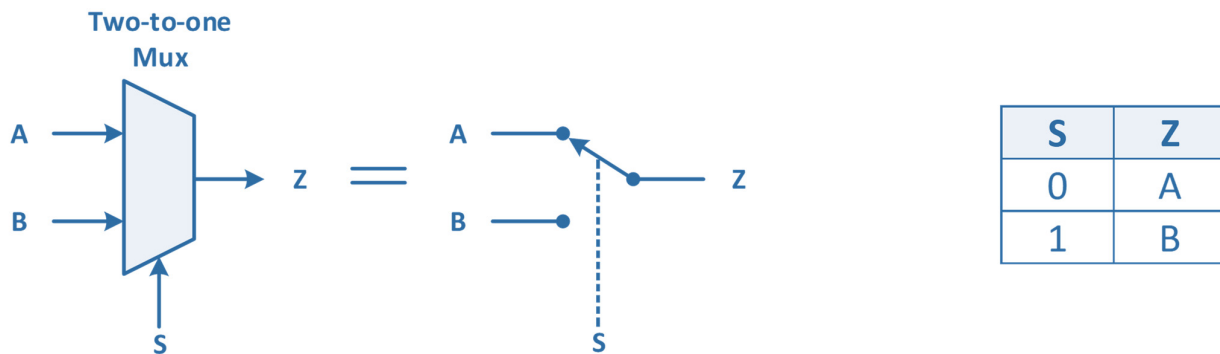


Figure 2.5: Functional block diagram and truth table of a 1-bit two-to-one multiplexer

UNDERSTANDING | TASK 4

A quick way to implement the Verilog code for a 1-bit two-to-one multiplexer is using the conditional syntax:

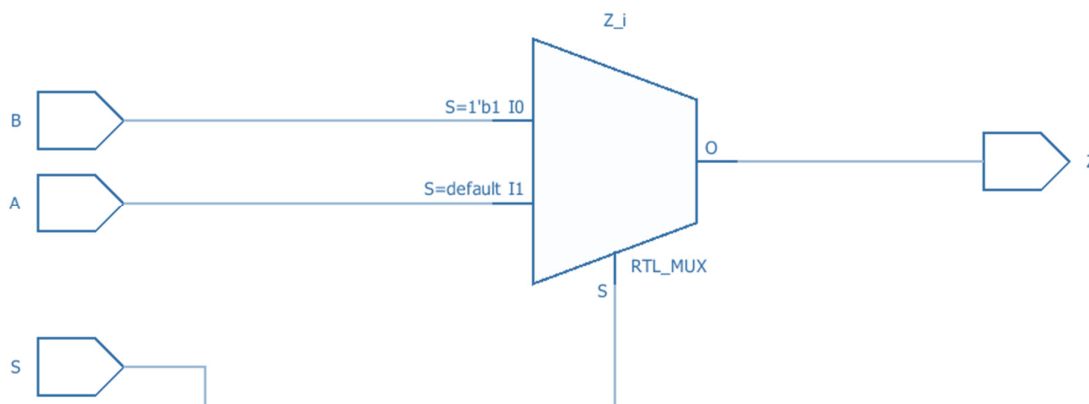
condition ? expression1 : expression2;

Notice in the schematic, how the code is automatically recognised as a MUX.

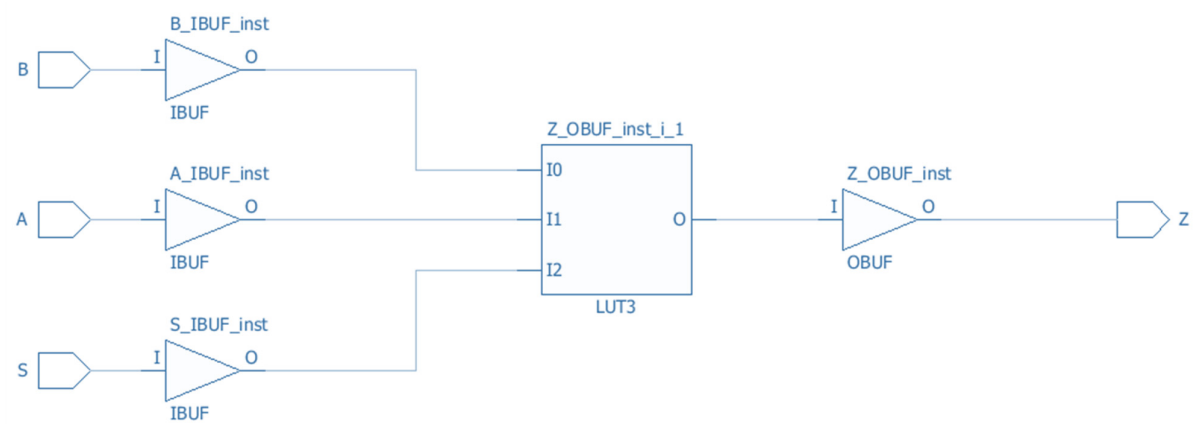
Verilog code for 1-bit two-to-one mux, using the dataflow method

```
module my_2_to_1_mux (input A, B, S, output Z);  
    assign Z = S ? B : A; // assign B to Z if S = 1 or assign A to Z if S = 0;  
endmodule
```

RTL schematic for the 1-bit two-to-one mux



Synthesised design schematic for the 1-bit two-to-one mux



Fill in the truth table for the **LUT3**, as extracted from the synthesised design schematic for the 1-bit two-to-one mux:

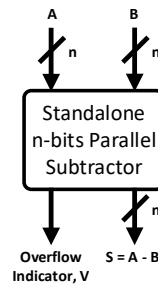
Explain how the truth table for the **LUT3** matches that of the truth table indicated in **Figure 2.5**:

GRADED POST-LAB ASSIGNMENT – THE STANDALONE SUBTRACTOR:

ASSIGNMENT

When your program starts, regardless of the switches SW0 to SW15 and leds LD0 to LD15, it is required for the seven segment displays to show the character as required from the previous lab 1 graded assignment. The anodes that are required to be enabled are also as indicated in that lab.

Then, based on your student matriculation number, you are required to create an n-bit parallel subtractor with overflow indicator (Henceforth, simply called the n-bit parallel subtractor), by combining several n-bit parallel adders. The overflow indicator is a one-bit value that indicates whether the result S is correctly represented in that specific n-bit number system. The n-bit parallel subtractor will be a standalone device, with no other subtractors connected to it and no other subtractors to connect to. The block diagram is shown below:



The RTL schematics of the n-bit parallel subtractor will need to be produced, the system simulated, and finally implemented on the Basys 3 development board.

REQUIREMENT BASED ON YOUR STUDENT MATRICULATION NUMBER

Based on the **second** rightmost numerical digit of your student matriculation number, create the following n-bit parallel adders:

Second rightmost numerical digit of your student matriculation number	Required n-bit parallel adders. Each one of these two n-bits parallel adders must be made up of multiple 1-bit adders	
0	2-bit parallel adder	3-bit parallel adder
1	3-bit parallel adder	2-bit parallel adder
2	2-bit parallel adder	4-bit parallel adder
3	4-bit parallel adder	2-bit parallel adder
4	3-bit parallel adder	4-bit parallel adder
5	4-bit parallel adder	3-bit parallel adder
6	3-bit parallel adder	5-bit parallel adder
7	5-bit parallel adder	3-bit parallel adder
8	2-bit parallel adder	5-bit parallel adder
9	5-bit parallel adder	2-bit parallel adder

After doing so, **make use of both n-bit parallel adders** to create your n-bit parallel subtractor, based on the **second** rightmost numerical digit of your student matriculation number. If required, you may assume that the user **will not input any carry-in value to the n-bit parallel subtractor.**

The bits given to the subtractor must be divided between the two n-bit parallel adders in the following manner:

Second rightmost numerical digit of your student matriculation number	Most significant bits of the subtractor must be given to the following adder	Least significant bits of the subtractor must be given to the following adder
0	2-bit parallel adder	3-bit parallel adder
1	3-bit parallel adder	2-bit parallel adder
2	2-bit parallel adder	4-bit parallel adder
3	4-bit parallel adder	2-bit parallel adder
4	3-bit parallel adder	4-bit parallel adder
5	4-bit parallel adder	3-bit parallel adder
6	3-bit parallel adder	5-bit parallel adder
7	5-bit parallel adder	3-bit parallel adder
8	2-bit parallel adder	5-bit parallel adder
9	5-bit parallel adder	2-bit parallel adder

Furthermore, it is compulsory to use the specified complement representation of the binary values, as indicated in the table below:

Second rightmost numerical digit of your student matriculation number	Required n-bit parallel subtractor
0	5-bit subtractor. Bits are in 2's complement
2	6-bit subtractor. Bits are in 2's complement
4	7-bit subtractor. Bits are in 2's complement
6	8-bit subtractor. Bits are in 2's complement
8	7-bit subtractor. Bits are in 2's complement
1	5-bit subtractor. Bits are in 1's complement
3	6-bit subtractor. Bits are in 1's complement
5	7-bit subtractor. Bits are in 1's complement
7	8-bit subtractor. Bits are in 1's complement
9	7-bit subtractor. Bits are in 1's complement

Example 1: If a student has matriculation number A1234567N, the second rightmost numerical digit is '6'. Thus, the student is required to create an 8-bit parallel subtractor, whereby all the bits are considered to be in 2's complement representation. That 8-bit subtractor must consist, at minimum, of these two parallel adders: A 3-bit parallel adder for the most significant bits, and a 5-bit parallel adder for the least significant bits.

Example 2: If a student has matriculation number A6543210Y, the second rightmost numerical digit is '1'. Thus, the student is required to create a 5-bit parallel subtractor, whereby all the bits are considered to be in 1's complement representation. That 5-bit subtractor must consist, at minimum, of these two parallel adders: A 3-bit parallel adder for the most significant bits, and a 2-bit parallel adder for the least significant bits.

SIMULATION REQUIREMENT:

You are also required to **simulate any five unique test cases as chosen by you**, for your n-bit subtractor circuit, to verify that the outputs, S and V, are as desired. If the number of unique test cases is less than five, full marks will not be achievable.

A screenshot (PrintScreen) of the simulation waveform pattern from the Vivado simulation window must be obtained, and then pasted on a 1-page landscape page. Marks are only given **if the simulation waveforms are clear, and all the five values are clearly visible in binary representations.**

RTL ANALYSIS SCHEMATIC REQUIREMENT:

A screenshot (PrintScreen) of the RTL analysis schematic from Vivado must be obtained, and pasted on a 1-page landscape page. You are not allowed to do any editing to the RTL analysis schematic screenshot.

For marks to be awarded, the following conditions must be met for the RTL analysis schematics (The images being shown here is for a 9-bit subtractor system, where a 4-bit parallel adder was used for the 4 most significant bits, and a 5-bit parallel adder was used for the 5 least significant bits):

- (1) None of the modules are expanded (That is, screenshot the updated and properly zoomed schematics directly after clicking on RTL Analysis -> Schematics). Furthermore, **a minimum of two n-bit parallel adder modules** (Based on your second rightmost numerical digit of your student matriculation number) **must be seen without any modules in the schematics being expanded.**

- (2) All inputs of the subtractor must be clear, including the numerical values between the square brackets. For example:



- (3) All outputs of the subtractor must be clear, including the numerical values between the square brackets. For example:



- (4) All inputs to, and outputs from, the n-bit parallel adder modules must be clear, including the numerical values between the square brackets. For example, in a 9-bit subtractor, there are at least two n-bit parallel adders (Based on your second rightmost numerical digit of your student matriculation number) being used:



DOCUMENT UPLOAD REQUIREMENTS:

- (1) Your name and matriculation number on the first page of the document.
- (2) The screenshot (PrintScreen) of the simulation waveform pattern from the Vivado simulation window on the first page of the document.
- (3) The screenshot (PrintScreen) of the RTL analysis schematic from Vivado on the second page of the document.

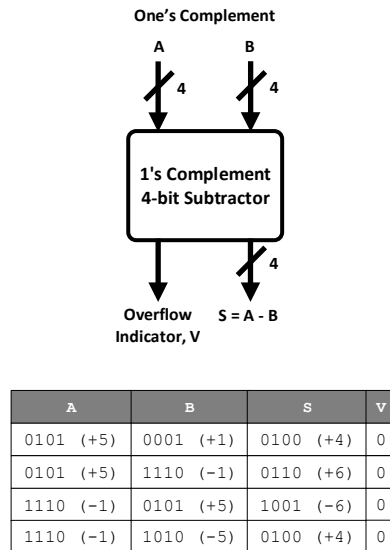
Print the two pages landscape document as a **single PDF** for LumiNUS upload. The PDF file **must follow the naming template** indicated in the LumiNUS submission instruction at the end of this lab manual.

EXAMPLE OF OUTPUTS FOR A 4-BIT PARALLEL SUBTRACTOR

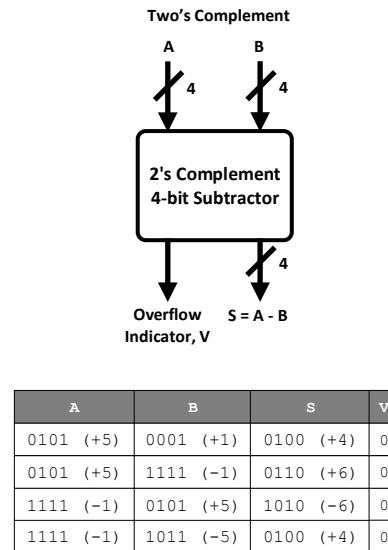
Assume that the two inputs to the subtractor are A and B. The output from the subtractor is sum S and overflow indicator V. In this example, we assume all the inputs and output S are 4 bits.

Since $A - B = A + (-B)$, by adding A to $-B$, the answer to $A - B$ can be obtained. The bits for A, B and S are either in 1's complement, or 2's complement, depending on your matriculation number as set out in the requirement table earlier.

Examples on the expected output S and V, for some input values of A and B



The overflow, V, is 0 here because the result S can correctly be represented in 1's complement in the 4-bit system



The overflow, V, is 0 here because the result S can correctly be represented in 2's complement in the 4-bit system

FURTHER REQUIREMENTS AND RESTRICTIONS: OPERATORS, SWITCHES AND LEDS

- It is compulsory to use the following switches to represent inputs A and B of the n-bit parallel subtractor:
 - The input A must use consecutive switches on the Basys 3 Development board, with the **least significant bit A[0] linked to SW0**. Similarly, A[1] should be linked to SW1, A[2] to SW2, and so on.
 - The input B must use consecutive switches on the Basys 3 Development board, with the **least significant bit B[0] linked to SW8**. Similarly, B[1] should be linked to SW9, B[2] to SW10, and so on.
 - Switches not used by A or B must NOT be used or linked to any other signals under any circumstances.** For example, in a 4-bit parallel subtractor, SW4 to SW7, and SW12 and SW15, should not be linked to any signals, nor used in any circumstances.
- It is compulsory to use the following LEDs to represent output S of the n-bit parallel subtractor:
 - The output S must use consecutive LEDs on the Basys 3 development board, with the **least significant bit S[0] linked to LD0**. Similarly, S[1] should be linked to LD1, S[2] should be linked to LD2, and so on.
 - LD15 must be used for the overflow indicator V**
 - LEDs not used by S must NOT be used or linked to any other signals under any circumstances.** For example, in a 4-bit parallel subtractor, LD4 to LD14, should not be linked to any signals, nor used in any circumstances.
- The addition and subtraction operators (+, -) are **not allowed** within the code.

HINT:

Review EE2026 Tutorial 2 and complete the MUX task before attempting this assignment

LUMINUS SUBMISSION INSTRUCTIONS

- Complete as much required functionalities as possible within the given deadline, and ensure that your bitstream has been successfully generated and tested on your Basys 3 development board **BEFORE** archiving your Vivado workspace for LumiNUS upload. No working bitstream is equivalent to no marks (It is best to have some working functionalities / requirements, instead of not having any bitstream at all while trying all requirements)
- It is compulsory to archive your project in a compressed form without any simulation waveforms. In the uploaded archive, the codes (.v files) are important, not the waveforms (.wdb files). **The archive size should not exceed 2 MB in size for lab 2.** Follow the instructions given in the pdf: “Archive Project in Vivado 2018.02”
- **After** following the instructions in “Archive Project in Vivado 2018.02”, rename your project archive as indicated in the appendix of this lab manual.
- Separately from the project archive, **the single PDF document** (Simulation waveform + RTL analysis schematic of the subtractor) is to be named as indicated in the appendix of this lab manual.
- Upload to LumiNUS EE2026 -> Files -> Lab and Project - Materials and Submissions -> Lab 2 Submission
- Download your LumiNUS archive after uploading. **Unzip the project folder within, open the program, and check if you can run your bitstream correctly.** No project files and no working bitstream is equivalent to losing all marks
- The LumiNUS upload must be completed by **Monday 15th February 2021, 12:00 P.M. (Noon)**. Do not plan to upload during the grace period of 2 hours
- A penalty of 25% applies for late submissions of up to 1 week.
- The late submission folder closes 1 week after the original deadline. **Late submissions are not accepted and not graded if a submission is found within the on-time folder, or if grading has already started on an earlier submitted file.** The late submission folder will be located at: LumiNUS EE2026 -> Files -> Lab and Project - Materials and Submissions -> Lab 2 Submission (Late Submission)

Plagiarism is penalised with a 100% penalty for all SOURCES and RECIPIENTS

All past and future submissions, and marks, will be reviewed in greater detail, for any person found to have plagiarised

ALL THE SUBMISSION INSTRUCTIONS LISTED ABOVE WILL AFFECT YOUR GRADES!

GRADING PROCESS

- During subsequent lab sessions, our graders will be providing you updates on the grading of your submission
- Submissions not following all the **LUMINUS SUBMISSION INSTRUCTIONS** (listed above) will not be graded immediately, and will instead be reviewed towards the end of the semester. **You will not be able to see your results during the labs in such situations**

APPENDIX (COMPULSORY renaming before just LumiNUS upload):

It is **compulsory to rename your project archive and PDF report**, just before the LumiNUS upload, as listed in the table below. Do not change any other part of the naming. Simply **copy** the naming from the table below, and **paste** it while renaming your project archive and report. Penalties will be incurred if your submission cannot be found according to the exact naming template below.

Archive Naming	Report Naming
L2_Tue_PM Aaron Chan Siang Joo_426_Archive	L2_Tue_PM Aaron Chan Siang Joo_426_Report
L2_Tue_AM Aditi Chadha_898_Archive	L2_Tue_AM Aditi Chadha_898_Report
L2_Tue_PM Aiden Thaw Aung Kham Th_186_Archive	L2_Tue_PM Aiden Thaw Aung Kham Th_186_Report
L2_Tue_AM Alvin Lim Jun_284_Archive	L2_Tue_AM Alvin Lim Jun_284_Report
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L2_Mon_PM Ang Qi Xuan_052_Archive	L2_Mon_PM Ang Qi Xuan_052_Report
L2_Tue_AM Ang Yong Siang Alwin_771_Archive	L2_Tue_AM Ang Yong Siang Alwin_771_Report
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L2_Tue_PM Ariel Ong Xing Er_560_Archive	L2_Tue_PM Ariel Ong Xing Er_560_Report
L2_Tue_AM Bellakka Krishnamurthy Pr_862_Archive	L2_Tue_AM Bellakka Krishnamurthy Pr_862_Report
L2_Tue_AM Boo Qian Wei Adeline_207_Archive	L2_Tue_AM Boo Qian Wei Adeline_207_Report
L2_Tue_AM Braden Teo Wei Ren_238_Archive	L2_Tue_AM Braden Teo Wei Ren_238_Report
L2_Tue_AM Brendan Lau Siew Zhi_596_Archive	L2_Tue_AM Brendan Lau Siew Zhi_596_Report
L2_Tue_AM Bryan Elmer Mulijono_447_Archive	L2_Tue_AM Bryan Elmer Mulijono_447_Report
L2_Tue_AM Bryan Wong Hong Liang_051_Archive	L2_Tue_AM Bryan Wong Hong Liang_051_Report
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L2_Tue_AM Chan Keng Jit_501_Archive	L2_Tue_AM Chan Keng Jit_501_Report
L2_Tue_PM Chan Yew Kun_985_Archive	L2_Tue_PM Chan Yew Kun_985_Report
L2_Thu_PM Chan Zhao Yong_518_Archive	L2_Thu_PM Chan Zhao Yong_518_Report
L2_Tue_PM Chan Zhi Jie Ryan_415_Archive	L2_Tue_PM Chan Zhi Jie Ryan_415_Report
L2_Tue_PM Chen Hsin_602_Archive	L2_Tue_PM Chen Hsin_602_Report
L2_Tue_AM CHEN SILIN_445_Archive	L2_Tue_AM CHEN SILIN_445_Report
L2_Tue_PM CHEN YUHAN_520_Archive	L2_Tue_PM CHEN YUHAN_520_Report
L2_Tue_AM Cheng Siyuan_728_Archive	L2_Tue_AM Cheng Siyuan_728_Report
L2_Tue_AM Chew Yi Jie_632_Archive	L2_Tue_AM Chew Yi Jie_632_Report
L2_Wed_PM Chia Shao Xian_447_Archive	L2_Wed_PM Chia Shao Xian_447_Report
L2_Tue_PM Chong Jia An_190_Archive	L2_Tue_PM Chong Jia An_190_Report
L2_Thu_AM Chong Xuan Liang_171_Archive	L2_Thu_AM Chong Xuan Liang_171_Report
L2_Thu_AM Christopher Nge Jing Qi_145_Archive	L2_Thu_AM Christopher Nge Jing Qi_145_Report
L2_Thu_AM Christopher TzeWen Langt_265_Archive	L2_Thu_AM Christopher TzeWen Langt_265_Report
L2_Tue_PM CHUA WAN NING_189_Archive	L2_Tue_PM CHUA WAN NING_189_Report
L2_Thu_AM Chua Xiong Wei_484_Archive	L2_Thu_AM Chua Xiong Wei_484_Report
L2_Wed_PM Chun Min Gyu_249_Archive	L2_Wed_PM Chun Min Gyu_249_Report
L2_Tue_PM Chung Ying Qiao Winnie_324_Archive	L2_Tue_PM Chung Ying Qiao Winnie_324_Report
L2_Thu_AM Conrad Ephraim Wee Cher J_123_Archive	L2_Thu_AM Conrad Ephraim Wee Cher J_123_Report
L2_Tue_PM Cordell Chan Yi Hng_253_Archive	L2_Tue_PM Cordell Chan Yi Hng_253_Report
L2_Thu_AM CUI MINJING_441_Archive	L2_Thu_AM CUI MINJING_441_Report
L2_Tue_PM Cui Xinyu_116_Archive	L2_Tue_PM Cui Xinyu_116_Report
L2_Thu_AM Damien Lim Yu Hao_933_Archive	L2_Thu_AM Damien Lim Yu Hao_933_Report
L2_Thu_AM Darren Khoo Kah Weng_516_Archive	L2_Thu_AM Darren Khoo Kah Weng_516_Report
L2_Tue_PM Darryl See_317_Archive	L2_Tue_PM Darryl See_317_Report
L2_Wed_PM Desmond Eng Kian Wee_095_Archive	L2_Wed_PM Desmond Eng Kian Wee_095_Report
L2_Tue_PM Donovan Sim Jing Yi_402_Archive	L2_Tue_PM Donovan Sim Jing Yi_402_Report
L2_Tue_PM Du Yantang_744_Archive	L2_Tue_PM Du Yantang_744_Report
L2_Thu_AM Edly Irsyad B Elham_555_Archive	L2_Thu_AM Edly Irsyad B Elham_555_Report
L2_Thu_AM Elumalai Oviya Dharshini_353_Archive	L2_Thu_AM Elumalai Oviya Dharshini_353_Report
L2_Thu_AM Eric Bryan_789_Archive	L2_Thu_AM Eric Bryan_789_Report
L2_Thu_AM Eugene Chong Zhi Liang_525_Archive	L2_Thu_AM Eugene Chong Zhi Liang_525_Report
L2_Thu_AM Fan Shixi_848_Archive	L2_Thu_AM Fan Shixi_848_Report
L2_Thu_AM FOONG XIN YU_018_Archive	L2_Thu_AM FOONG XIN YU_018_Report
L2_Tue_PM Fu Zhehui_218_Archive	L2_Tue_PM Fu Zhehui_218_Report
L2_Thu_AM Gavien Pat Wei Zhuo_185_Archive	L2_Thu_AM Gavien Pat Wei Zhuo_185_Report
L2_Tue_AM GOH KAI YAO BRYAN_690_Archive	L2_Tue_AM GOH KAI YAO BRYAN_690_Report
L2_Tue_PM Goh Shao Quan_422_Archive	L2_Tue_PM Goh Shao Quan_422_Report
L2_Tue_PM GOH SHAU HUI GEORGE_353_Archive	L2_Tue_PM GOH SHAU HUI GEORGE_353_Report
L2_Tue_PM Goh Wei Yang_254_Archive	L2_Tue_PM Goh Wei Yang_254_Report

L2_Tue_PM_Gu_Jianqiang_514_Archive	L2_Tue_PM_Gu_Jianqiang_514_Report
L2_Tue_PM_Guan_Dinghe_736_Archive	L2_Tue_PM_Guan_Dinghe_736_Report
L2_Wed_PM_Han_Si_Yuan_050_Archive	L2_Wed_PM_Han_Si_Yuan_050_Report
L2_Tue_PM_Hemanth_Bangalore_Sriniva_135_Archive	L2_Tue_PM_Hemanth_Bangalore_Sriniva_135_Report
L2_Tue_PM_Ho_Shu_Jun_198_Archive	L2_Tue_PM_Ho_Shu_Jun_198_Report
L2_Thu_AM_Ho_Zhen_Hong_014_Archive	L2_Thu_AM_Ho_Zhen_Hong_014_Report
L2_Thu_AM_Hoang_Trong_Tan_425_Archive	L2_Thu_AM_Hoang_Trong_Tan_425_Report
L2_Thu_AM_HOE_JUN_LEONG_182_Archive	L2_Thu_AM_HOE_JUN_LEONG_182_Report
L2_Tue_PM_Hong_Xingwen_861_Archive	L2_Tue_PM_Hong_Xingwen_861_Report
L2_Thu_AM_Hossan_Goh_Xuan_Rong_833_Archive	L2_Thu_AM_Hossan_Goh_Xuan_Rong_833_Report
L2_Tue_PM_How_Teck_Wei_391_Archive	L2_Tue_PM_How_Teck_Wei_391_Report
L2_Thu_AM_HU_JIALUN_521_Archive	L2_Thu_AM_HU_JIALUN_521_Report
L2_Thu_AM_Hu_Xuefei_885_Archive	L2_Thu_AM_Hu_Xuefei_885_Report
L2_Thu_AM_Huang_Che_Yen_597_Archive	L2_Thu_AM_Huang_Che_Yen_597_Report
L2_Mon_PM_HUANG_HAOFENG_936_Archive	L2_Mon_PM_HUANG_HAOFENG_936_Report
L2_Tue_PM_Huang_Shanshan_622_Archive	L2_Tue_PM_Huang_Shanshan_622_Report
L2_Tue_PM_HUANG_YUJING_485_Archive	L2_Tue_PM_HUANG_YUJING_485_Report
L2_Thu_AM_Ian_Wang_Ee_En_227_Archive	L2_Thu_AM_Ian_Wang_Ee_En_227_Report
L2_Tue_PM_Imperial_Edward_Justin_Ja_356_Archive	L2_Tue_PM_Imperial_Edward_Justin_Ja_356_Report
L2_Thu_AM_Ishaan_Maunil_Vyas_479_Archive	L2_Thu_AM_Ishaan_Maunil_Vyas_479_Report
L2_Thu_AM_Izdiyyad_Farhan_B_Zuri_407_Archive	L2_Thu_AM_Izdiyyad_Farhan_B_Zuri_407_Report
L2_Mon_PM_Jared_Cheang_192_Archive	L2_Mon_PM_Jared_Cheang_192_Report
L2_Tue_PM_Jareth_Tan_Eu_Quan_240_Archive	L2_Tue_PM_Jareth_Tan_Eu_Quan_240_Report
L2_Tue_PM_Jason_Ong_Meng_Lee_174_Archive	L2_Tue_PM_Jason_Ong_Meng_Lee_174_Report
L2_Tue_PM_Jasshan_Kumeresh_503_Archive	L2_Tue_PM_Jasshan_Kumeresh_503_Report
L2_Tue_PM_Jeremiah_Jiang_139_Archive	L2_Tue_PM_Jeremiah_Jiang_139_Report
L2_Tue_PM_Jeremiah_Ong_Ray_551_Archive	L2_Tue_PM_Jeremiah_Ong_Ray_551_Report
L2_Tue_PM_Jeremy_Goh_Liang_Yi_393_Archive	L2_Tue_PM_Jeremy_Goh_Liang_Yi_393_Report
L2_Mon_PM_JIANG_QIXIONG_698_Archive	L2_Mon_PM_JIANG_QIXIONG_698_Report
L2_Thu_AM_Jiang_Xing_Kai_564_Archive	L2_Thu_AM_Jiang_Xing_Kai_564_Report
L2_Tue_AM_Jin_Minyue_069_Archive	L2_Tue_AM_Jin_Minyue_069_Report
L2_Wed_PM_JIN_YIXUAN_976_Archive	L2_Wed_PM_JIN_YIXUAN_976_Report
L2_Thu_AM_Joanne_Wong_Wei_Yin_527_Archive	L2_Thu_AM_Joanne_Wong_Wei_Yin_527_Report
L2_Thu_AM_Joel_Matthew_Chiam_Zhi_Qi_250_Archive	L2_Thu_AM_Joel_Matthew_Chiam_Zhi_Qi_250_Report
L2_Thu_AM_Jon_Lim_Yong_Kiat_782_Archive	L2_Thu_AM_Jon_Lim_Yong_Kiat_782_Report
L2_Thu_AM_Jonathan_Mui_Koy_Kit_534_Archive	L2_Thu_AM_Jonathan_Mui_Koy_Kit_534_Report
L2_Thu_AM_Joshua_Harsha_Dass_714_Archive	L2_Thu_AM_Joshua_Harsha_Dass_714_Report
L2_Thu_AM_Justin_Fidelis_Wong_Jun_W_326_Archive	L2_Thu_AM_Justin_Fidelis_Wong_Jun_W_326_Report
L2_Thu_AM_Kairos_Koh_Jia_Jun_149_Archive	L2_Thu_AM_Kairos_Koh_Jia_Jun_149_Report
L2_Thu_AM_Keh_Wen_Yang_Rachel_249_Archive	L2_Thu_AM_Keh_Wen_Yang_Rachel_249_Report
L2_Thu_PM_Kevinaldi_Dwiastajulio_Hu_912_Archive	L2_Thu_PM_Kevinaldi_Dwiastajulio_Hu_912_Report
L2_Thu_AM_Khoo_Jia_Le_Isaac_733_Archive	L2_Thu_AM_Khoo_Jia_Le_Isaac_733_Report
L2_Thu_PM_Khor_Sheng_Hou_443_Archive	L2_Thu_PM_Khor_Sheng_Hou_443_Report
L2_Thu_AM_Kishor_Kumar_Haribaskar_481_Archive	L2_Thu_AM_Kishor_Kumar_Haribaskar_481_Report
L2_Tue_AM_Koh_Meng_Kiat_Kenneth_512_Archive	L2_Tue_AM_Koh_Meng_Kiat_Kenneth_512_Report
L2_Thu_AM_Koh_Qianqi_746_Archive	L2_Thu_AM_Koh_Qianqi_746_Report
L2_Thu_PM_Koh_Qin_Ruo_055_Archive	L2_Thu_PM_Koh_Qin_Ruo_055_Report
L2_Thu_PM_Koh_Ruizhe_Jerome_429_Archive	L2_Thu_PM_Koh_Ruizhe_Jerome_429_Report
L2_Thu_AM_Kom_Xing_Yuan_993_Archive	L2_Thu_AM_Kom_Xing_Yuan_993_Report
L2_Thu_AM_Kong_Dak_Nam_171_Archive	L2_Thu_AM_Kong_Dak_Nam_171_Report
L2_Tue_PM_Koo_Wei_De_133_Archive	L2_Tue_PM_Koo_Wei_De_133_Report
L2_Thu_PM_Krishna_R_R_900_Archive	L2_Thu_PM_Krishna_R_R_900_Report
L2_Thu_AM_Kum_Wing_Ho_725_Archive	L2_Thu_AM_Kum_Wing_Ho_725_Report
L2_Thu_AM_Kumaravel_Vignesh_585_Archive	L2_Thu_AM_Kumaravel_Vignesh_585_Report
L2_Thu_AM_Kwok_Xiu_Sheng_Theodore_118_Archive	L2_Thu_AM_Kwok_Xiu_Sheng_Theodore_118_Report
L2_Thu_AM_Kwong_Zhi_Qian_569_Archive	L2_Thu_AM_Kwong_Zhi_Qian_569_Report
L2_Thu_AM_Lam_Junyu_William_903_Archive	L2_Thu_AM_Lam_Junyu_William_903_Report
L2_Thu_AM_LAM_KAI_WEN_JONATHAN_213_Archive	L2_Thu_AM_LAM_KAI_WEN_JONATHAN_213_Report
L2_Thu_PM_Lau_Miang_Puang_Glennard_207_Archive	L2_Thu_PM_Lau_Miang_Puang_Glennard_207_Report
L2_Tue_AM_Lee_An_Sheng_263_Archive	L2_Tue_AM_Lee_An_Sheng_263_Report
L2_Tue_AM_Lee_Cheok_Feng_743_Archive	L2_Tue_AM_Lee_Cheok_Feng_743_Report
L2_Thu_PM_Lee_Hung_Tien_965_Archive	L2_Thu_PM_Lee_Hung_Tien_965_Report
L2_Thu_PM_Lee_Jia_Jun_423_Archive	L2_Thu_PM_Lee_Jia_Jun_423_Report
L2_Thu_PM_Lee_Jing_Rui_Evan_399_Archive	L2_Thu_PM_Lee_Jing_Rui_Evan_399_Report
L2_Wed_PM_Lee_Jun_Wen_466_Archive	L2_Wed_PM_Lee_Jun_Wen_466_Report
L2_Tue_AM_LEE_KENG_YONG_JOSHUA_644_Archive	L2_Tue_AM_LEE_KENG_YONG_JOSHUA_644_Report
L2_Tue_AM_Lee_Qi_An_644_Archive	L2_Tue_AM_Lee_Qi_An_644_Report
L2_Thu_PM_Lee_ShiAn_Matthew_324_Archive	L2_Thu_PM_Lee_ShiAn_Matthew_324_Report
L2_Tue_AM_Lee_Sungmin_490_Archive	L2_Tue_AM_Lee_Sungmin_490_Report
L2_Tue_PM_Lee_Sze_Ern_Jeremy_510_Archive	L2_Tue_PM_Lee_Sze_Ern_Jeremy_510_Report
L2_Tue_AM_Lee_Yi_Kai_550_Archive	L2_Tue_AM_Lee_Yi_Kai_550_Report
L2_Thu_PM_Lee_YuHsueh_639_Archive	L2_Thu_PM_Lee_YuHsueh_639_Report

L2_Tue_PM LEONARD CHUA ZHONG QI 873 Archive	L2_Tue_PM LEONARD CHUA ZHONG QI 873_Report
L2_Thu_PM Leong Kah Choong 455 Archive	L2_Thu_PM Leong Kah Choong 455_Report
L2_Tue_AM Leow Yuan Yang 574 Archive	L2_Tue_AM Leow Yuan Yang 574_Report
L2_Thu_PM Leroy Ong Nai Kiat 506 Archive	L2_Thu_PM Leroy Ong Nai Kiat 506_Report
L2_Thu_PM Li Huanda 101 Archive	L2_Thu_PM Li Huanda 101_Report
L2_Tue_AM Li Xi Yuan 926 Archive	L2_Tue_AM Li Xi Yuan 926_Report
L2_Tue_AM Liang Yuzhao 802 Archive	L2_Tue_AM Liang Yuzhao 802_Report
L2_Wed_PM LIM BING SEN 580 Archive	L2_Wed_PM LIM BING SEN 580_Report
L2_Thu_AM LIM CHANG QUAN THADDEUS 210 Archive	L2_Thu_AM LIM CHANG QUAN THADDEUS 210_Report
L2_Thu_PM Lim Jia Sheng Jackson 596 Archive	L2_Thu_PM Lim Jia Sheng Jackson 596_Report
L2_Tue_AM Lim Kay Yun 244 Archive	L2_Tue_AM Lim Kay Yun 244_Report
L2_Tue_AM Lim Shyun Yin 063 Archive	L2_Tue_AM Lim Shyun Yin 063_Report
L2_Thu_PM Lim Wen Jie 382 Archive	L2_Thu_PM Lim Wen Jie 382_Report
L2_Thu_PM Liu Danfeng 777 Archive	L2_Thu_PM Liu Danfeng 777_Report
L2_Thu_PM Liu Ruijun 371 Archive	L2_Thu_PM Liu Ruijun 371_Report
L2_Tue_AM LIU ZEHANG 491 Archive	L2_Tue_AM LIU ZEHANG 491_Report
L2_Wed_PM LIU ZHIYANG 653 Archive	L2_Wed_PM LIU ZHIYANG 653_Report
L2_Thu_PM Loo Keng Leong 408 Archive	L2_Thu_PM Loo Keng Leong 408_Report
L2_Tue_AM LOW ZHEN WEI JERRELL 516 Archive	L2_Tue_AM LOW ZHEN WEI JERRELL 516_Report
L2_Thu_PM Lu Jingguang 319 Archive	L2_Thu_PM Lu Jingguang 319_Report
L2_Tue_AM Lu Sicheng 634 Archive	L2_Tue_AM Lu Sicheng 634_Report
L2_Tue_PM LU ZONGHAN 452 Archive	L2_Tue_PM LU ZONGHAN 452_Report
L2_Tue_PM MA XUDONG 493 Archive	L2_Tue_PM MA XUDONG 493_Report
L2_Tue_AM Ma Zijian 828 Archive	L2_Tue_AM Ma Zijian 828_Report
L2_Tue_AM Madhan Selvapandian 482 Archive	L2_Tue_AM Madhan Selvapandian 482_Report
L2_Thu_PM Madheswaran Niveytha 465 Archive	L2_Thu_PM Madheswaran Niveytha 465_Report
L2_Tue_AM Mah Yuan Jie Alvin 500 Archive	L2_Tue_AM Mah Yuan Jie Alvin 500_Report
L2_Tue_AM Mahadevan Svetha 108 Archive	L2_Tue_AM Mahadevan Svetha 108_Report
L2_Tue_AM Mahadevan Swati 107 Archive	L2_Tue_AM Mahadevan Swati 107_Report
L2_Thu_PM Marcus Goh Xuan De 355 Archive	L2_Thu_PM Marcus Goh Xuan De 355_Report
L2_Thu_PM Marcus Lim Sheng Jie 408 Archive	L2_Thu_PM Marcus Lim Sheng Jie 408_Report
L2_Tue_AM Marcus Ong Yih 404 Archive	L2_Tue_AM Marcus Ong Yih 404_Report
L2_Tue_AM Mathur Aayush 581 Archive	L2_Tue_AM Mathur Aayush 581_Report
L2_Tue_AM Mayank Panjiyara 763 Archive	L2_Tue_AM Mayank Panjiyara 763_Report
L2_Thu_PM Mehedi Hasan Salim 436 Archive	L2_Thu_PM Mehedi Hasan Salim 436_Report
L2_Thu_PM Mohamed Faez Bin Shahlan 297 Archive	L2_Thu_PM Mohamed Faez Bin Shahlan 297_Report
L2_Tue_AM Mohammad Shoib Memon Loya 487 Archive	L2_Tue_AM Mohammad Shoib Memon Loya 487_Report
L2_Thu_PM Muhammad Aizat Bin Rahim 437 Archive	L2_Thu_PM Muhammad Aizat Bin Rahim 437_Report
L2_Tue_AM Muhammad Ashraf B Mohamad 432 Archive	L2_Tue_AM Muhammad Ashraf B Mohamad 432_Report
L2_Thu_PM MUHAMMAD HAZIM BIN ABDULL 633 Archive	L2_Thu_PM MUHAMMAD HAZIM BIN ABDULL 633_Report
L2_Wed_PM Muhammad Jaish Bin Jamalu 287 Archive	L2_Wed_PM Muhammad Jaish Bin Jamalu 287_Report
L2_Tue_AM Mun Le Zong 172 Archive	L2_Tue_AM Mun Le Zong 172_Report
L2_Thu_PM Nan Song 102 Archive	L2_Thu_PM Nan Song 102_Report
L2_Tue_AM Ng Andre 973 Archive	L2_Tue_AM Ng Andre 973_Report
L2_Tue_AM Ng Cheng Yang Titus 478 Archive	L2_Tue_AM Ng Cheng Yang Titus 478_Report
L2_Thu_PM Ng Jin Loong Jeremy 395 Archive	L2_Thu_PM Ng Jin Loong Jeremy 395_Report
L2_Thu_PM Ng Qi Hao 420 Archive	L2_Thu_PM Ng Qi Hao 420_Report
L2_Thu_PM Ng Xinyi 545 Archive	L2_Thu_PM Ng Xinyi 545_Report
L2_Tue_AM Ngoi Hui Wen Vanessa 471 Archive	L2_Tue_AM Ngoi Hui Wen Vanessa 471_Report
L2_Tue_AM Nguyen Minh Tuan 389 Archive	L2_Tue_AM Nguyen Minh Tuan 389_Report
L2_Mon_PM Nguyen Van Binh 453 Archive	L2_Mon_PM Nguyen Van Binh 453_Report
L2_Thu_PM Nigel Loh Weien 416 Archive	L2_Thu_PM Nigel Loh Weien 416_Report
L2_Mon_PM Nigel Ng 444 Archive	L2_Mon_PM Nigel Ng 444_Report
L2_Mon_PM Nishant Rai 182 Archive	L2_Mon_PM Nishant Rai 182_Report
L2_Thu_PM Oh Qi Ren 441 Archive	L2_Thu_PM Oh Qi Ren 441_Report
L2_Tue_PM Ong Chor Yew 460 Archive	L2_Tue_PM Ong Chor Yew 460_Report
L2_Thu_PM Ong Jun Giat 205 Archive	L2_Thu_PM Ong Jun Giat 205_Report
L2_Thu_AM Ong Siying Falicia 566 Archive	L2_Thu_AM Ong Siying Falicia 566_Report
L2_Thu_PM Ong Yew Yong Adrian 401 Archive	L2_Thu_PM Ong Yew Yong Adrian 401_Report
L2_Thu_PM Owng Kai Leng Sally 331 Archive	L2_Thu_PM Owng Kai Leng Sally 331_Report
L2_Thu_PM Pang Kai Lin 036 Archive	L2_Thu_PM Pang Kai Lin 036_Report
L2_Thu_PM Pang Kai Yi 236 Archive	L2_Thu_PM Pang Kai Yi 236_Report
L2_Wed_PM Pang Qi Wei Jenna 685 Archive	L2_Wed_PM Pang Qi Wei Jenna 685_Report
L2_Mon_PM Paramita Tejasvi 194 Archive	L2_Mon_PM Paramita Tejasvi 194_Report
L2_Thu_PM Peh Li Yan 267 Archive	L2_Thu_PM Peh Li Yan 267_Report
L2_Mon_PM PENG FEI 518 Archive	L2_Mon_PM PENG FEI 518_Report
L2_Tue_AM Peng Yanjia 877 Archive	L2_Tue_AM Peng Yanjia 877_Report
L2_Thu_PM Phoon Pei Zhen 744 Archive	L2_Thu_PM Phoon Pei Zhen 744_Report
L2_Thu_PM Phua Keng Wee 706 Archive	L2_Thu_PM Phua Keng Wee 706_Report
L2_Thu_PM Phuah Yong Chen Keith 360 Archive	L2_Thu_PM Phuah Yong Chen Keith 360_Report
L2_Tue_AM Pichanon Rattanadilok Na 545 Archive	L2_Tue_AM Pichanon Rattanadilok Na 545_Report
L2_Wed_PM Pojcharapol Leenukiat 642 Archive	L2_Wed_PM Pojcharapol Leenukiat 642_Report

L2_Wed_PM_Poon_Jeun_Lek_202_Archive	L2_Wed_PM_Poon_Jeun_Lek_202_Report
L2_Tue_AM_Pow_Zhi_Xiang_942_Archive	L2_Tue_AM_Pow_Zhi_Xiang_942_Report
L2_Wed_PM_Pradhan_Rachit_Manish_230_Archive	L2_Wed_PM_Pradhan_Rachit_Manish_230_Report
L2_Tue_AM_Pranav_Venkatram_200_Archive	L2_Tue_AM_Pranav_Venkatram_200_Report
L2_Wed_PM_Qi_Tian_Cong_442_Archive	L2_Wed_PM_Qi_Tian_Cong_442_Report
L2_Tue_AM_Ramalingam_Saravanamani_586_Archive	L2_Tue_AM_Ramalingam_Saravanamani_586_Report
L2_Tue_AM_Ravindiran_Rakesh_010_Archive	L2_Tue_AM_Ravindiran_Rakesh_010_Report
L2_Thu_AM_Rebecca_Chua_171_Archive	L2_Thu_AM_Rebecca_Chua_171_Report
L2_Mon_PM_REN_TIANLE_446_Archive	L2_Mon_PM_REN_TIANLE_446_Report
L2_Thu_AM_Renzo_Rivera_Canare_502_Archive	L2_Thu_AM_Renzo_Rivera_Canare_502_Report
L2_Wed_PM_Reuel_Teo_Lu_Wei_435_Archive	L2_Wed_PM_Reuel_Teo_Lu_Wei_435_Report
L2_Thu_AM_Richard_Willie_368_Archive	L2_Thu_AM_Richard_Willie_368_Report
L2_Thu_AM_Roycius_Lim_Yuanwei_060_Archive	L2_Thu_AM_Roycius_Lim_Yuanwei_060_Report
L2_Tue_PM_Samuel_Ong_Wei_Chuan_462_Archive	L2_Tue_PM_Samuel_Ong_Wei_Chuan_462_Report
L2_Wed_PM_Se_Seal_140_Archive	L2_Wed_PM_Se_Seal_140_Report
L2_Thu_AM_See_Jian_Hui_737_Archive	L2_Thu_AM_See_Jian_Hui_737_Report
L2_Mon_PM_Seet_Ting_Yang_Irvin_608_Archive	L2_Mon_PM_Seet_Ting_Yang_Irvin_608_Report
L2_Mon_PM_Seetoh_Yit_Ching_154_Archive	L2_Mon_PM_Seetoh_Yit_Ching_154_Report
L2_Mon_PM_Seo_Gimin_442_Archive	L2_Mon_PM_Seo_Gimin_442_Report
L2_Wed_PM_Seth_Teng_Shann_419_Archive	L2_Wed_PM_Seth_Teng_Shann_419_Report
L2_Mon_PM_Shao_Yurui_111_Archive	L2_Mon_PM_Shao_Yurui_111_Report
L2_Wed_PM_Shawn_Chang_151_Archive	L2_Wed_PM_Shawn_Chang_151_Report
L2_Wed_PM_Shreshth_Sarda_424_Archive	L2_Wed_PM_Shreshth_Sarda_424_Report
L2_Mon_PM_Shyam_Ganesh_Jayagopi_484_Archive	L2_Mon_PM_Shyam_Ganesh_Jayagopi_484_Report
L2_Wed_PM_Sidharth_Premnath_502_Archive	L2_Wed_PM_Sidharth_Premnath_502_Report
L2_Thu_AM_Siew_Yang_Zhi_331_Archive	L2_Thu_AM_Siew_Yang_Zhi_331_Report
L2_Wed_PM_Sim_Le_Yee_Beatrice_769_Archive	L2_Wed_PM_Sim_Le_Yee_Beatrice_769_Report
L2_Thu_PM_Sin_Ren_Xiang_865_Archive	L2_Thu_PM_Sin_Ren_Xiang_865_Report
L2_Wed_PM_Sivakumar_Yogarajan_505_Archive	L2_Wed_PM_Sivakumar_Yogarajan_505_Report
L2_Wed_PM_Song_Chenan_797_Archive	L2_Wed_PM_Song_Chenan_797_Report
L2_Wed_PM_Song_Min_Kyu_226_Archive	L2_Wed_PM_Song_Min_Kyu_226_Report
L2_Mon_PM_Sridharan_Arvind_Srinivas_477_Archive	L2_Mon_PM_Sridharan_Arvind_Srinivas_477_Report
L2_Mon_PM_Sthitipragyan_Samal_664_Archive	L2_Mon_PM_Sthitipragyan_Samal_664_Report
L2_Mon_PM_Sun_Jiale_853_Archive	L2_Mon_PM_Sun_Jiale_853_Report
L2_Thu_PM_SUN_JIAWEI_496_Archive	L2_Thu_PM_SUN_JIAWEI_496_Report
L2_Mon_PM_SWAMINATHAN_VARUN_281_Archive	L2_Mon_PM_SWAMINATHAN_VARUN_281_Report
L2_Mon_PM_Swann_Tet_Aung_552_Archive	L2_Mon_PM_Swann_Tet_Aung_552_Report
L2_Wed_PM_Tan_Haoxuan_934_Archive	L2_Wed_PM_Tan_Haoxuan_934_Report
L2_Mon_PM_Tan_Hui_En_373_Archive	L2_Mon_PM_Tan_Hui_En_373_Report
L2_Mon_PM_Tan_Jun_Heng_Daren_Justin_331_Archive	L2_Mon_PM_Tan_Jun_Heng_Daren_Justin_331_Report
L2_Mon_PM_Tan_Kah_Heng_677_Archive	L2_Mon_PM_Tan_Kah_Heng_677_Report
L2_Mon_PM_Tan_Le_Yi_071_Archive	L2_Mon_PM_Tan_Le_Yi_071_Report
L2_Wed_PM_Tan_Lindsey_197_Archive	L2_Wed_PM_Tan_Lindsey_197_Report
L2_Wed_PM_Tan_Qi_Xian_Keith_397_Archive	L2_Wed_PM_Tan_Qi_Xian_Keith_397_Report
L2_Mon_PM_Tan_Rui_Yang_472_Archive	L2_Mon_PM_Tan_Rui_Yang_472_Report
L2_Wed_PM_Tan_Tze_Yeong_970_Archive	L2_Wed_PM_Tan_Tze_Yeong_970_Report
L2_Wed_PM_Tan_Wei_Li_336_Archive	L2_Wed_PM_Tan_Wei_Li_336_Report
L2_Mon_PM_Tan_Xing_Jie_747_Archive	L2_Mon_PM_Tan_Xing_Jie_747_Report
L2_Wed_PM_Tan_Yong_Zheng_261_Archive	L2_Wed_PM_Tan_Yong_Zheng_261_Report
L2_Mon_PM_Tang_Zehou_210_Archive	L2_Mon_PM_Tang_Zehou_210_Report
L2_Mon_PM_Tay>Weida_027_Archive	L2_Mon_PM_Tay>Weida_027_Report
L2_Mon_PM_Tay_Yi_Heng_Atticus_994_Archive	L2_Mon_PM_Tay_Yi_Heng_Atticus_994_Report
L2_Mon_PM_Teh_Jiewen_520_Archive	L2_Mon_PM_Teh_Jiewen_520_Report
L2_Wed_PM_Teh_ZiChun_328_Archive	L2_Wed_PM_Teh_ZiChun_328_Report
L2_Mon_PM_Teng_Yi_Shiong_647_Archive	L2_Mon_PM_Teng_Yi_Shiong_647_Report
L2_Mon_PM_Teo_Ziyi_Ivy_117_Archive	L2_Mon_PM_Teo_Ziyi_Ivy_117_Report
L2_Wed_PM_Tham_Yang_Tze_Xavier_256_Archive	L2_Wed_PM_Tham_Yang_Tze_Xavier_256_Report
L2_Thu_PM_TIAN_ZHENYU_467_Archive	L2_Thu_PM_TIAN_ZHENYU_467_Report
L2_Wed_PM_Tiang_Zhang_Quan_Xavier_446_Archive	L2_Wed_PM_Tiang_Zhang_Quan_Xavier_446_Report
L2_Wed_PM_Tie_Zhou_Peng_264_Archive	L2_Wed_PM_Tie_Zhou_Peng_264_Report
L2_Wed_PM>Toh_Yi_Cheng_421_Archive	L2_Wed_PM>Toh_Yi_Cheng_421_Report
L2_Mon_PM>Toh_Yi_Zhi_086_Archive	L2_Mon_PM>Toh_Yi_Zhi_086_Report
L2_Mon_PM_Tran_Nhan_Duc_Anh_358_Archive	L2_Mon_PM_Tran_Nhan_Duc_Anh_358_Report
L2_Wed_PM_Tran_Thi_Phuong_Thao_438_Archive	L2_Wed_PM_Tran_Thi_Phuong_Thao_438_Report
L2_Wed_PM_Varun_Agarwal_605_Archive	L2_Wed_PM_Varun_Agarwal_605_Report
L2_Mon_PM_VIKAS_HARLANI_376_Archive	L2_Mon_PM_VIKAS_HARLANI_376_Report
L2_Mon_PM_Vishal_Jeyaram_224_Archive	L2_Mon_PM_Vishal_Jeyaram_224_Report
L2_Wed_PM_Wan_Haocheng_780_Archive	L2_Wed_PM_Wan_Haocheng_780_Report
L2_Wed_PM_Wang_Wenxuan_649_Archive	L2_Wed_PM_Wang_Wenxuan_649_Report
L2_Thu_PM_WANG_YUDA_443_Archive	L2_Thu_PM_WANG_YUDA_443_Report
L2_Mon_PM_Wang_Zhao_Yu_Edward_953_Archive	L2_Mon_PM_Wang_Zhao_Yu_Edward_953_Report
L2_Mon_PM_Wang_Zhihuang_682_Archive	L2_Mon_PM_Wang_Zhihuang_682_Report

L2_Wed_PM_Wang_Zichen_951_Archive	L2_Wed_PM_Wang_Zichen_951_Report
L2_Wed_PM_Wang_Zihan_361_Archive	L2_Wed_PM_Wang_Zihan_361_Report
L2_Wed_PM_Wang_Zixi_445_Archive	L2_Wed_PM_Wang_Zixi_445_Report
L2_Mon_PM_William_Wahyudi_230_Archive	L2_Mon_PM_William_Wahyudi_230_Report
L2_Tue_AM_Wong_Jun_Lin_077_Archive	L2_Tue_AM_Wong_Jun_Lin_077_Report
L2_Mon_PM_Wong_Tze_Shan_Samantha_672_Archive	L2_Mon_PM_Wong_Tze_Shan_Samantha_672_Report
L2_Mon_PM_Wong_Zi_Xin_Avellin_073_Archive	L2_Mon_PM_Wong_Zi_Xin_Avellin_073_Report
L2_Mon_PM_Woo_Bo_Tuan_153_Archive	L2_Mon_PM_Woo_Bo_Tuan_153_Report
L2_Thu_PM_WU_HAO_HSUAN_635_Archive	L2_Thu_PM_WU_HAO_HSUAN_635_Report
L2_Mon_PM_Wu_Luoyu_894_Archive	L2_Mon_PM_Wu_Luoyu_894_Report
L2_Wed_PM_WU_YUWEI_472_Archive	L2_Wed_PM_WU_YUWEI_472_Report
L2_Wed_PM_XIAO_JUNTIAN_497_Archive	L2_Wed_PM_XIAO_JUNTIAN_497_Report
L2_Wed_PM_Xu_Yuxing_183_Archive	L2_Wed_PM_Xu_Yuxing_183_Report
L2_Wed_PM_Xue_Yuxuan_250_Archive	L2_Wed_PM_Xue_Yuxuan_250_Report
L2_Mon_PM_Yam_Jin_Ee_Dmitri_974_Archive	L2_Mon_PM_Yam_Jin_Ee_Dmitri_974_Report
L2_Tue_AM_Yang_Zikun_313_Archive	L2_Tue_AM_Yang_Zikun_313_Report
L2_Mon_PM_Yap_Joon_Siong_925_Archive	L2_Mon_PM_Yap_Joon_Siong_925_Report
L2_Mon_PM_YAP_WEI_XUAN_997_Archive	L2_Mon_PM_YAP_WEI_XUAN_997_Report
L2_Thu_PM_Yap_Zhan_Wei_455_Archive	L2_Thu_PM_Yap_Zhan_Wei_455_Report
L2_Mon_PM_Yeat_Nai_Jie_613_Archive	L2_Mon_PM_Yeat_Nai_Jie_613_Report
L2_Wed_PM_Yeo_Shi_Heng_390_Archive	L2_Wed_PM_Yeo_Shi_Heng_390_Report
L2_Mon_PM_Yeo_Wei_Hng_075_Archive	L2_Mon_PM_Yeo_Wei_Hng_075_Report
L2_Mon_PM_Yeo_Zi_Hao_Edwin_710_Archive	L2_Mon_PM_Yeo_Zi_Hao_Edwin_710_Report
L2_Mon_PM_YIP_WAYNE_998_Archive	L2_Mon_PM_YIP_WAYNE_998_Report
L2_Wed_PM_YU_HAIHONG_470_Archive	L2_Wed_PM_YU_HAIHONG_470_Report
L2_Thu_AM_Yue_Junfeng_802_Archive	L2_Thu_AM_Yue_Junfeng_802_Report
L2_Wed_PM_Yuk_Yeon_Soo_243_Archive	L2_Wed_PM_Yuk_Yeon_Soo_243_Report
L2_Mon_PM_Zeng_Jiexiong_052_Archive	L2_Mon_PM_Zeng_Jiexiong_052_Report
L2_Thu_AM_ZHANG_HAOYU_783_Archive	L2_Thu_AM_ZHANG_HAOYU_783_Report
L2_Mon_PM_ZHAO_LUOYUANG_466_Archive	L2_Mon_PM_ZHAO_LUOYUANG_466_Report
L2_Wed_PM_Zhao_Yibo_863_Archive	L2_Wed_PM_Zhao_Yibo_863_Report
L2_Wed_PM_Zhao_Ziqi_275_Archive	L2_Wed_PM_Zhao_Ziqi_275_Report
L2_Mon_PM_ZHONG_XINGHAN_468_Archive	L2_Mon_PM_ZHONG_XINGHAN_468_Report
L2_Mon_PM_ZHOU_CHENGXU_492_Archive	L2_Mon_PM_ZHOU_CHENGXU_492_Report
L2_Wed_PM_ZHOU_YUHAN_530_Archive	L2_Wed_PM_ZHOU_YUHAN_530_Report
L2_Wed_PM_Zhu_Shaohan_Steven_193_Archive	L2_Wed_PM_Zhu_Shaohan_Steven_193_Report
L2_Mon_PM_Zhuang_Jianning_277_Archive	L2_Mon_PM_Zhuang_Jianning_277_Report
L2_Tue_PM_Zubin_Jain_990_Archive	L2_Tue_PM_Zubin_Jain_990_Report