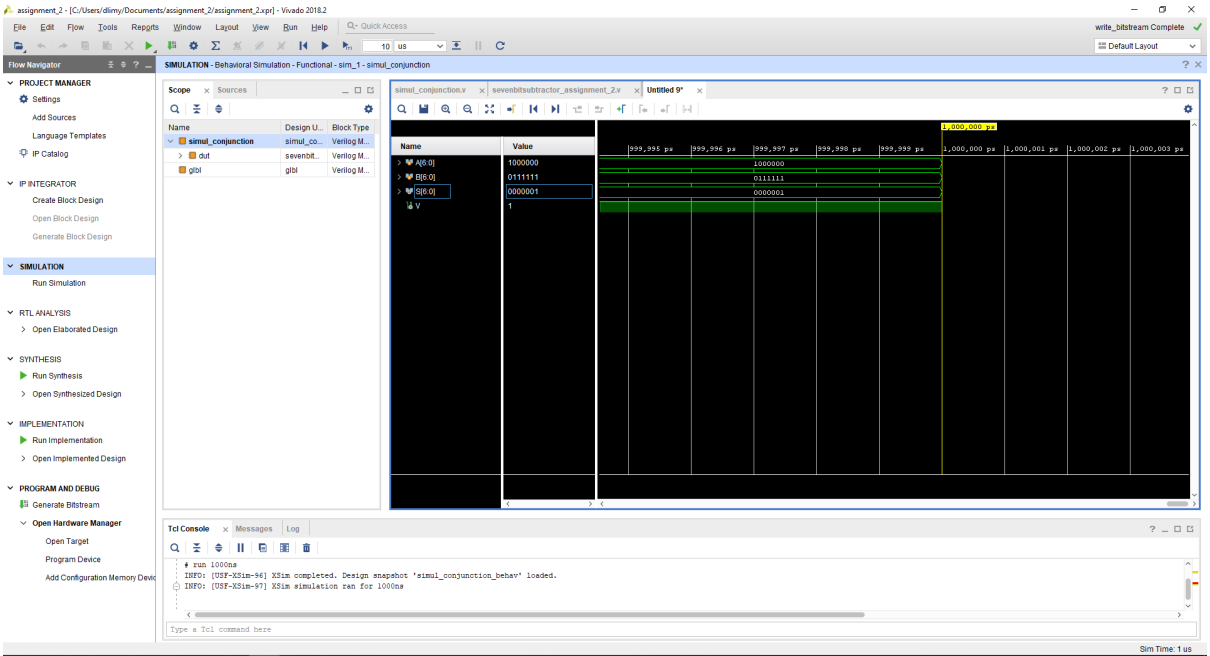
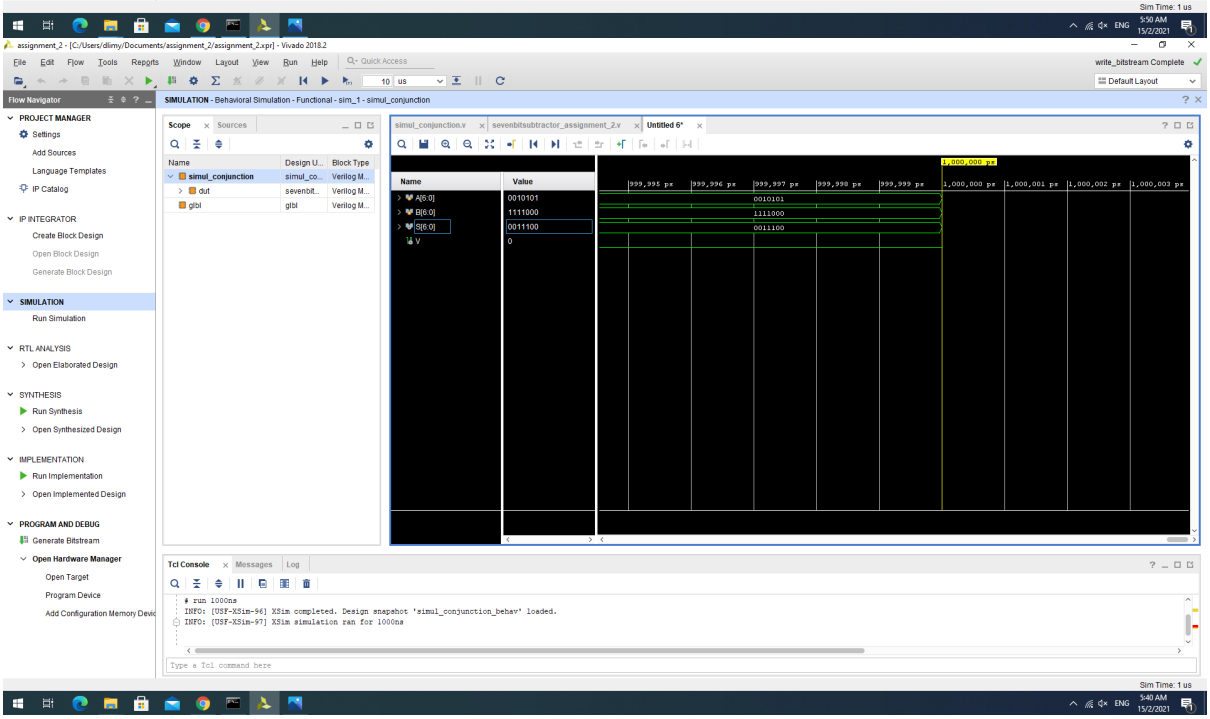
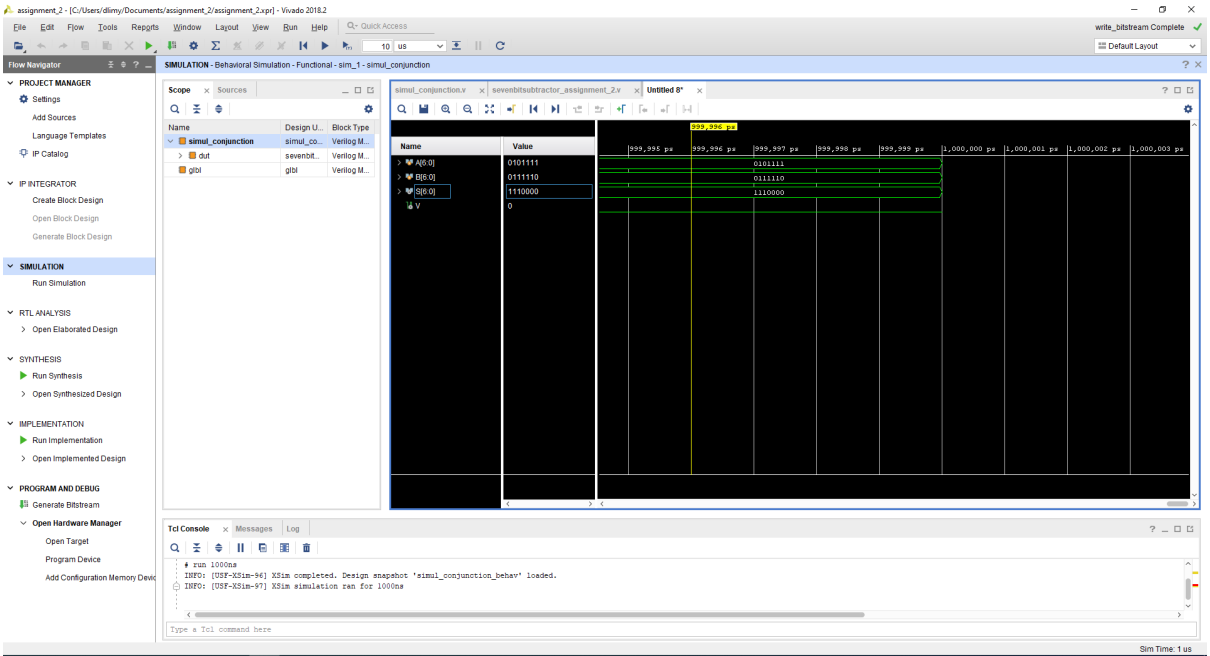
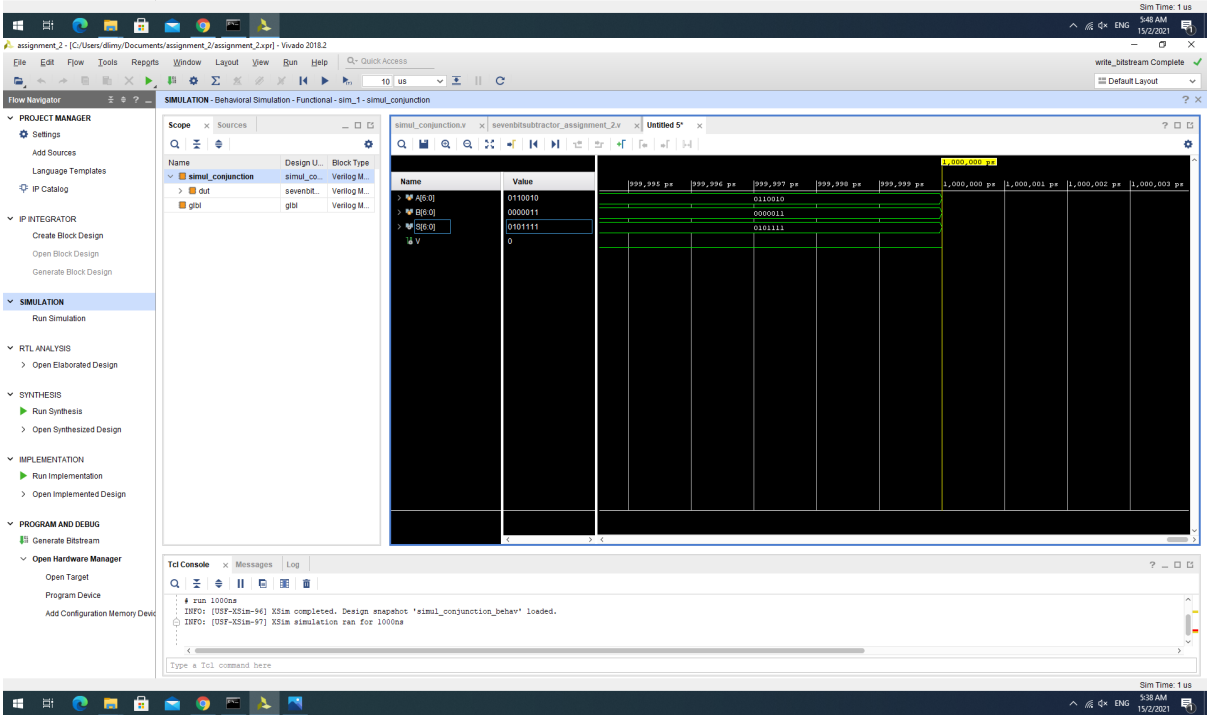
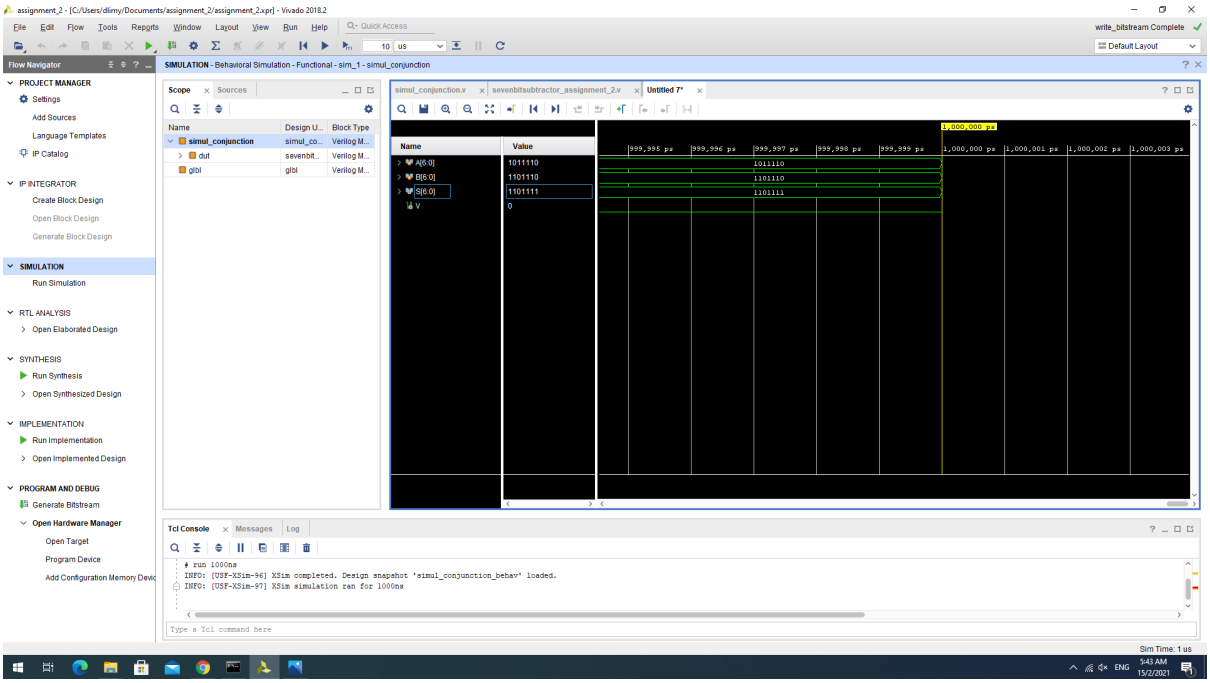
Damien Lim Yu Hao
A0223892Y

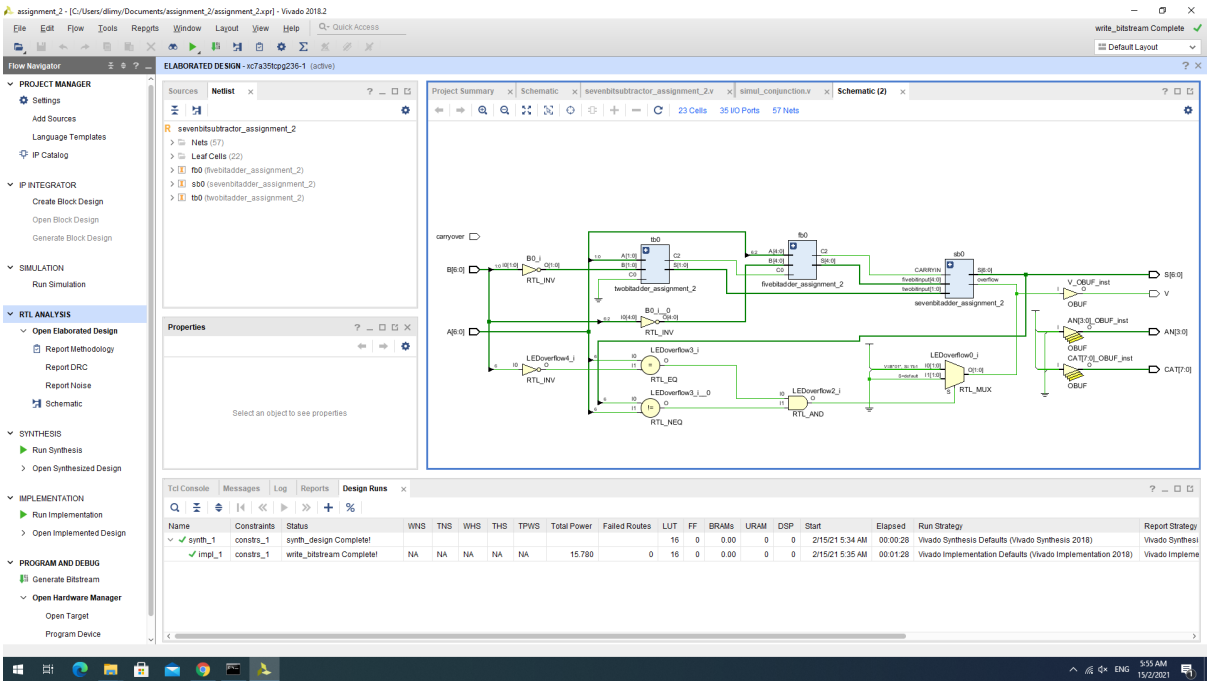





assignment_2 - [C:/Users/dilmy/Documents/assignment_2/assignment_2.xpr] - Vivado 2018.2
SIMULATION - Behavioral Simulation - Functional - sim_1 - simul_conjunction
simul_conjunction
dut
glbl
A[6:0]
B[6:0]
S[6:0]
V
0101111
0111110
1110000
0
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'simul_conjunction_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
Sim Time: 1 us


assignment_2 - [C:/Users/dilmy/Documents/assignment_2/assignment_2.xpr] - Vivado 2018.2
SIMULATION - Behavioral Simulation - Functional - sim_1 - simul_conjunction
simul_conjunction
dut
glbl
A[6:0]
B[6:0]
S[6:0]
V
0110010
0000011
0101111
0
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'simul_conjunction_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
Sim Time: 1 us


assignment_2 - [C:/Users/dlimy/Documents/assignment_2/assignment_2.xpr] - Vivado 2018.2
File Edit Flow Tools Reports Window Layout View Run Help
Quick Access
write_bitstream Complete
Default Layout
Flow Navigator
SIMULATION - Behavioral Simulation - Functional - sim_1 - simul_conjunction
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
Add Configuration Memory Devic
Scope
Sources
Name
Design U...
Block Type
simul_conjunction
simul_co...
Verilog M...
dut
sevenbit...
Verilog M...
glbl
glbl
Verilog M...
simul_conjunction.v
sevenbitsubtractor_assignment_2.v
Untitled 7*
Name
Value
A[6:0]
1011110
B[6:0]
1101110
S[6:0]
1101111
V
0
1,000,000 ps
999,995 ps
999,996 ps
999,997 ps
999,998 ps
999,999 ps
1,000,000 ps
1,000,001 ps
1,000,002 ps
1,000,003 ps
1011110
1101110
1101111
Tcl Console
Messages
Log
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'simul_conjunction_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
Type a Tcl command here
Sim Time: 1 us
ENG
5:43 AM
15/2/2021


assignment_2 - [C:/Users/dlimy/Documents/assignment_2/assignment_2.xpr] - Vivado 2018.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
write_bitstream Complete
Default Layout
Flow Navigator
ELABORATED DESIGN - xc7a35tcpg236-1 (active)
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
Sources
Netlist
sevenbitsubtractor_assignment_2
Nets (57)
Leaf Cells (22)
fb0 (fivebitadder_assignment_2)
sb0 (sevenbitadder_assignment_2)
tb0 (twobitadder_assignment_2)
Properties
Select an object to see properties
Project Summary
Schematic
sevenbitsubtractor_assignment_2.v
simul_conjunction.v
Schematic (2)
23 Cells
35 I/O Ports
57 Nets
carryover
B[6:0]
A[6:0]
RTL_INV
twobitadder_assignment_2
fivebitadder_assignment_2
sevenbitadder_assignment_2
V_OBUF_inst
OBUF
AN[3:0]_OBUF_inst
CA[7:0]_OBUF_inst
S[6:0]
V
AN[3:0]
CA[7:0]
LEDoverflow4_i
LEDoverflow3_i
LEDoverflow3_i_0
LEDoverflow2_i
LEDoverflow0_i
RTL_EQ
RTL_NEQ
RTL_AND
RTL_MUX
Tcl Console
Messages
Log
Reports
Design Runs
Name
Constraints
Status
WNS
TNS
WHS
THS
TPWS
Total Power
Failed Routes
LUT
FF
BRAMs
URAM
DSP
Start
Elapsed
Run Strategy
Report Strategy
synth_1
constrs_1
synth_design Complete!
16
0
0.00
0
0
2/15/21 5:34 AM
00:00:28
Vivado Synthesis Defaults (Vivado Synthesis 2018)
Vivado Synthesi
impl_1
constrs_1
write_bitstream Complete!
NA
NA
NA
NA
NA
15.780
0
16
0
0.00
0
0
2/15/21 5:35 AM
00:01:28
Vivado Implementation Defaults (Vivado Implementation 2018)
Vivado Impleme
ENG
5:55 AM
15/2/2021