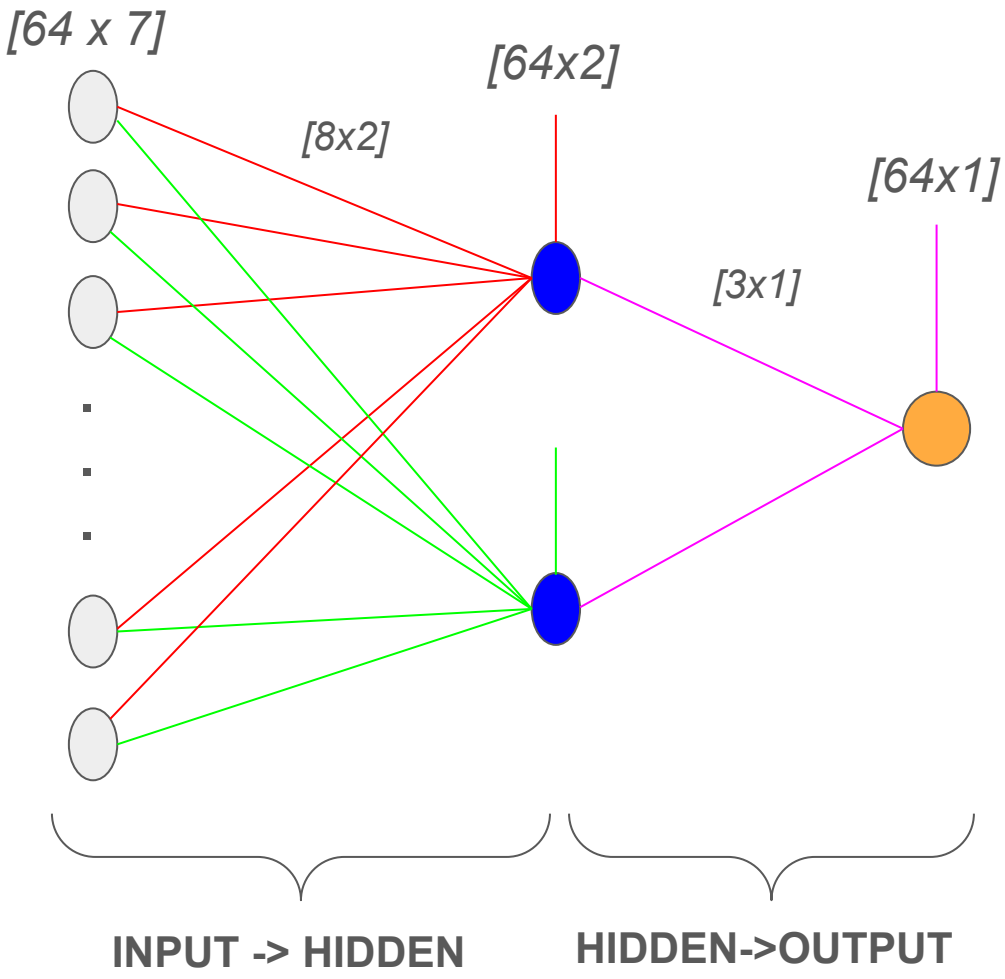
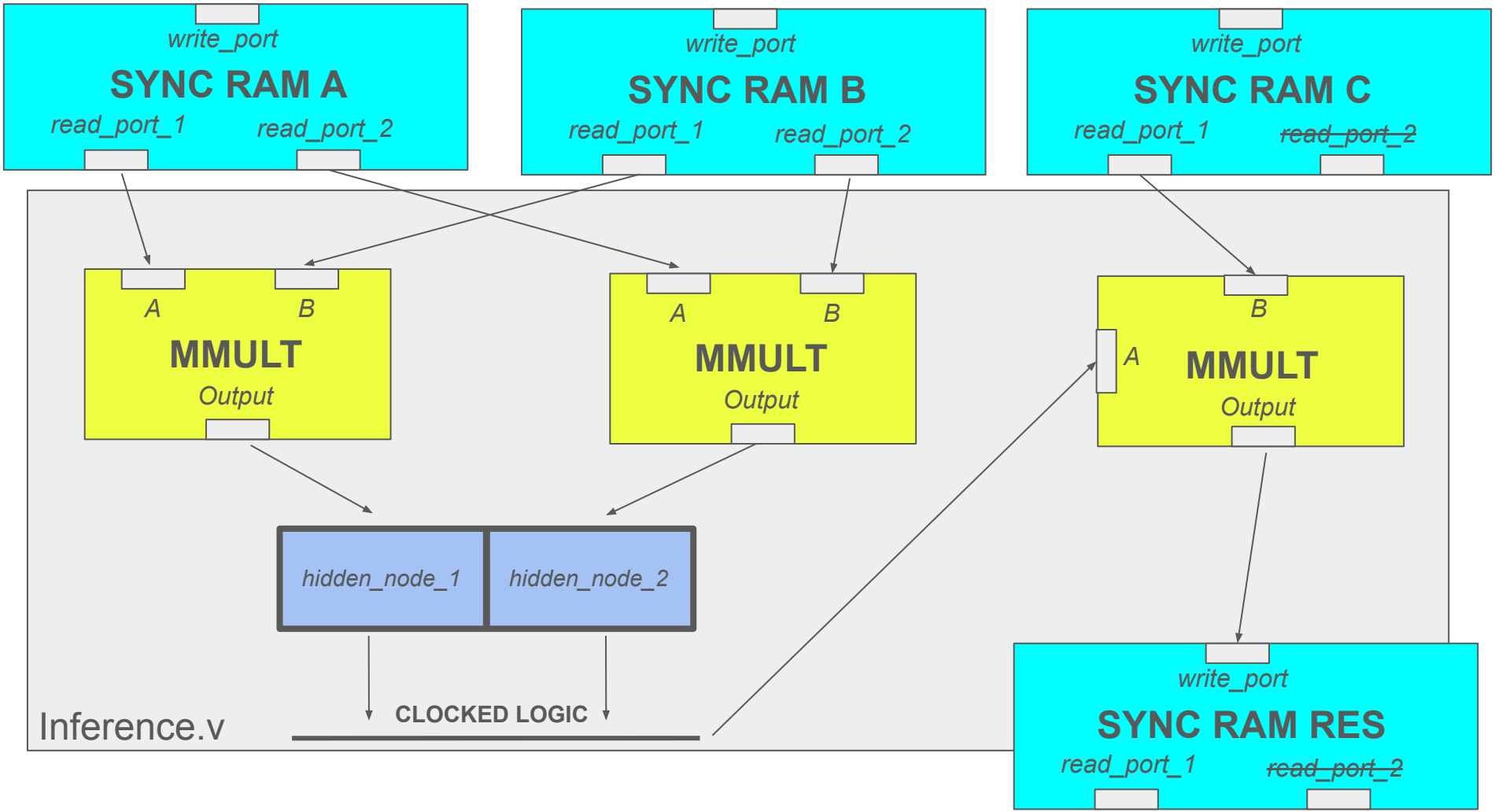
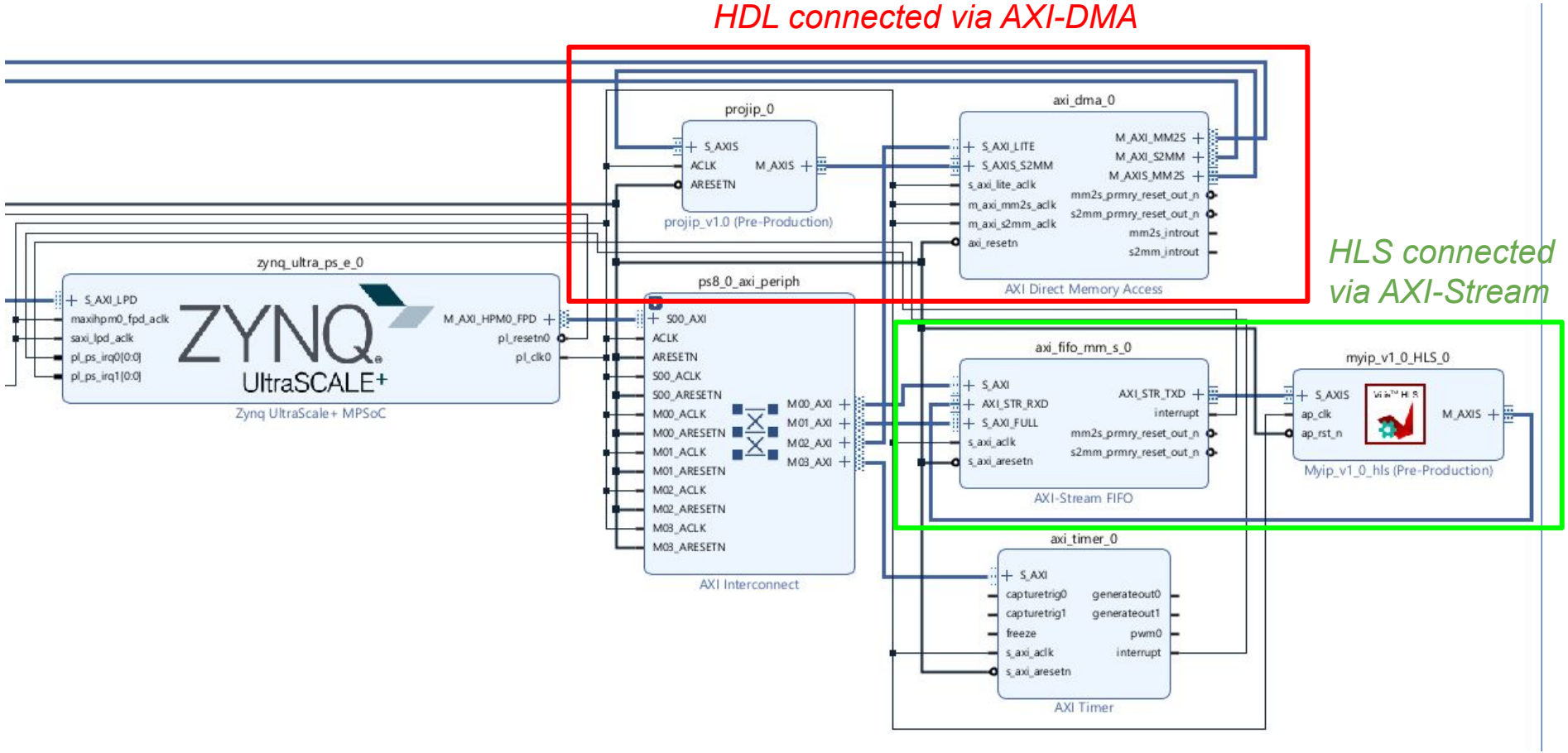


We do not need to wait for entire *INPUT->HIDDEN* layer to complete, before we can start on *HIDDEN->OUTPUT*

Once we have computed the *[1x2]* matrix corresponding to the hidden nodes for an $\mathbf{i}^{th}$ datapoint, we can concurrently do …

- Computation of *[1x1]* matrix corresponding to output node for the $\mathbf{i}^{th}$ datapoint
- Computation of [1x2] matrix corresponding to hidden nodes for $\mathbf{i}^{th+1}$ datapoint


write_port
SYNC RAM A
read_port_1
read_port_2
write_port
SYNC RAM B
read_port_1
read_port_2
write_port
SYNC RAM C
read_port_1
read_port_2
A
B
MMULT
Output
A
B
MMULT
Output
B
A
MMULT
Output
hidden_node_1
hidden_node_2
CLOCKED LOGIC
Inference.v
write_port
SYNC RAM RES
read_port_1
read_port_2


HDL connected via AXI-DMA
HLS connected via AXI-Stream
projip_0
S_AXIS
ACLK
ARESETN
M_AXIS
projip_v1.0 (Pre-Production)
axi_dma_0
S_AXI_LITE
S_AXIS_S2MM
s_axi_lite_aclk
m_axi_mm2s_aclk
m_axi_s2mm_aclk
axi_resetn
M_AXI_MM2S
M_AXI_S2MM
M_AXIS_MM2S
mm2s_prmry_reset_out_n
s2mm_prmry_reset_out_n
mm2s_introut
s2mm_introut
AXI Direct Memory Access
zynq_ultra_ps_e_0
S_AXI_LPD
maxihpm0_fpd_aclk
saxi_lpd_aclk
pl_ps_irq0[0:0]
pl_ps_irq1[0:0]
ZYNQ
UltraSCALE+
M_AXI_HPM0_FPD
pl_resetn0
pl_clk0
Zynq UltraScale+ MPSoC
ps8_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
M02_ACLK
M02_ARESETN
M03_ACLK
M03_ARESETN
M00_AXI
M01_AXI
M02_AXI
M03_AXI
AXI Interconnect
axi_fifo_mm_s_0
S_AXI
AXI_STR_RXD
S_AXI_FULL
s_axi_aclk
s_axi_aresetn
AXI_STR_TXD
interrupt
mm2s_prmry_reset_out_n
s2mm_prmry_reset_out_n
AXI-Stream FIFO
myip_v1_0_HLS_0
S_AXIS
ap_clk
ap_rst_n
M_AXIS
Myip_v1_0_hls (Pre-Production)
axi_timer_0
S_AXI
capturetrig0
capturetrig1
freeze
s_axi_aclk
s_axi_aresetn
generateout0
generateout1
pwm0
interrupt
AXI Timer

```
Zynq MP First Stage Boot Loader
Release 2023.2   Mar 20 2024  -  19:33:41
PMU-FW is not running, certain applications may not be supported.
HARD_HDL chosen. AXI-DMA(Polling).
Ready to accept files from Realterm
Files received from Realterm
Kickoff SOFT and HARD calculations
SW mult is 3011
HW mult is 1370 Comparing data ...
15 78 78 62 49 55 77 84 72 56 47 45 88 78 78 55 90 50 75 46 55 58 78 36 72 68 82
 71 46 35 45 49 49 39 68 73 47 82 40 84 39 104 43 41 57 84 96 67 79 47 34 70 69
44 78 39 33 87 45 50 81 45 62 52 Verification success
```

Resource	Estimation	Available	Utilization...
LUT	570	117120	0.49
LUTRAM	34	57600	0.06
FF	336	234240	0.14
BRAM	1	144	0.69
IO	47	189	24.87
BUFG	1	352	0.28

```
Zynq MP First Stage Boot Loader
Release 2023.2   Mar 20 2024  -  19:33:41
PMU-FW is not running, certain applications may not be supported.
HARD_HLS chosen. AXI-Stream(Interrupt).
Ready to accept files from Realterm
Files received from Realterm
Kickoff SOFT and HARD calculations
SW mult is 3032
HW mult is 22929 Comparing data ...
15 78 78 62 49 55 77 84 72 56 47 45 88 78 78 55 90 50 75 46 55 58 78 36 72 68 82
 71 46 35 45 49 49 39 68 73 47 82 40 84 39 104 43 41 57 84 96 67 79 47 34 70 69
44 78 39 33 87 45 50 81 45 62 52 Verification success
```

BRAM	DSP	FF	LUT	URAM
1	192	14680	25053	0