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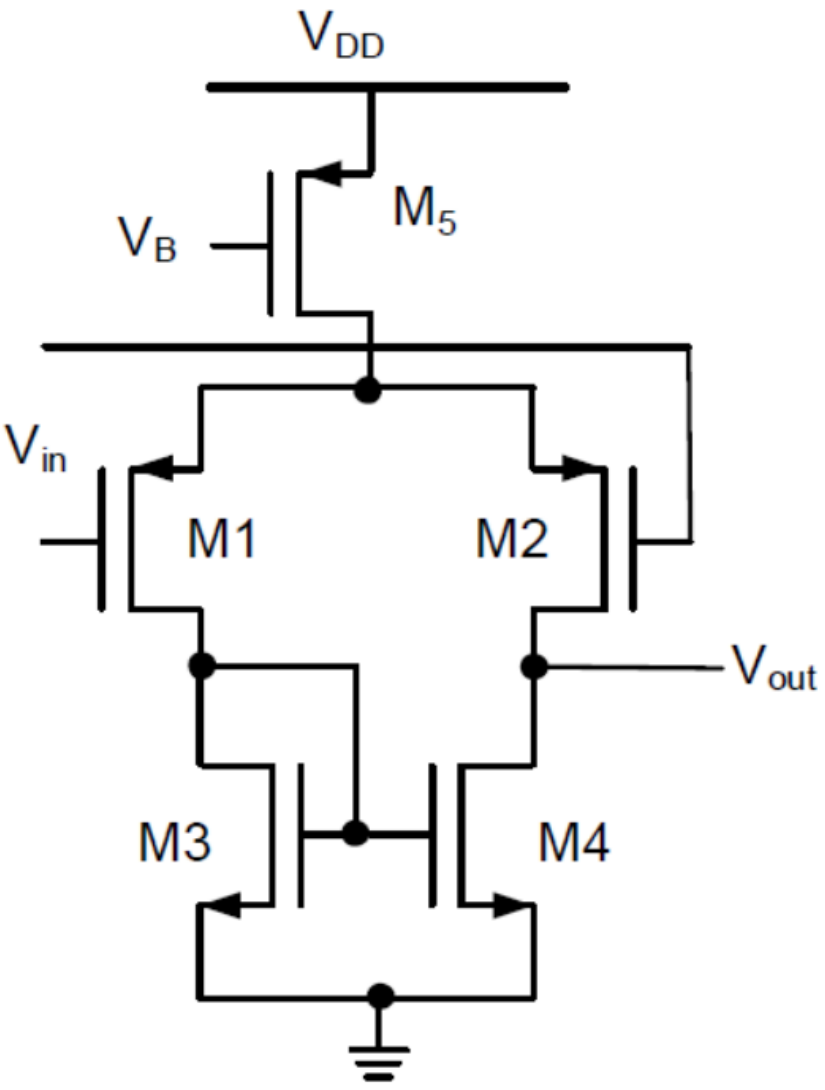
/class1/ug22/a223892y/ee3408C/project/SubProj3/TwoStageOpAmp

INTRODUCTION

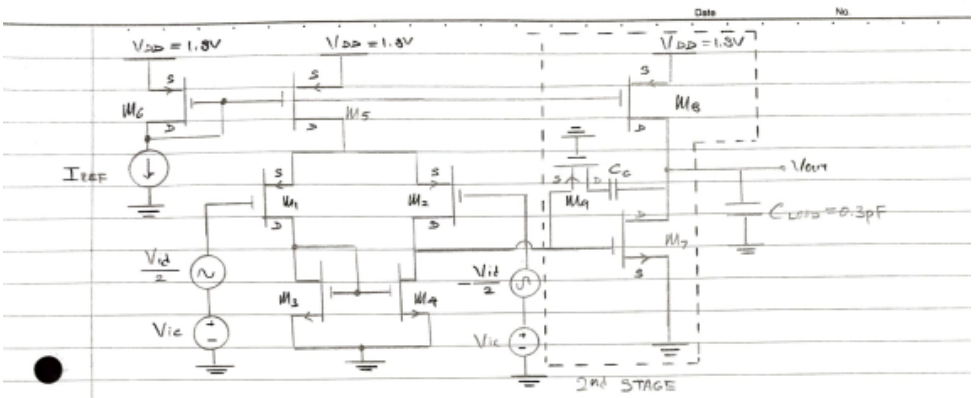
Designing a (PMOS) two stage Op-Amp, according to specifications.

1. Supply Voltage: 1.8V (Single supply)
2. Open-loop DC Gain: > 72dB
3. Gain Peaking < 1.5dB (ratio of maximum gain to DC gain)
4. Unity Gain Bandwidth > 18Mhz
5. Phase Margin > 60 degrees
6. CMRR: > 70dB
7. Output voltage swing >1V (peak to peak)
8. Offset voltage: < 1mV
9. Supply Current: < 600uA
10. Output Load Capacitance = 0.3pF
11. Maximum channel width: 1000um



Sample Schematic of the <u>FIRST</u> stage

HAND CALCULATION



DC Requirements

- $V_{DD} = 1.8V$
- $I_{SUPPLY} < 600\,\mu A$
- $V_{OD7} = V_{GS7} - V_{THN}$
  → choose $V_{OD7} = 100mV$, $V_{GS7} = 420mV$
- $V_{OD8} = V_{SG8} - |V_{THP}|$
  → choose $V_{OD8} = 100mV$, $V_{SG7} = 550mV$

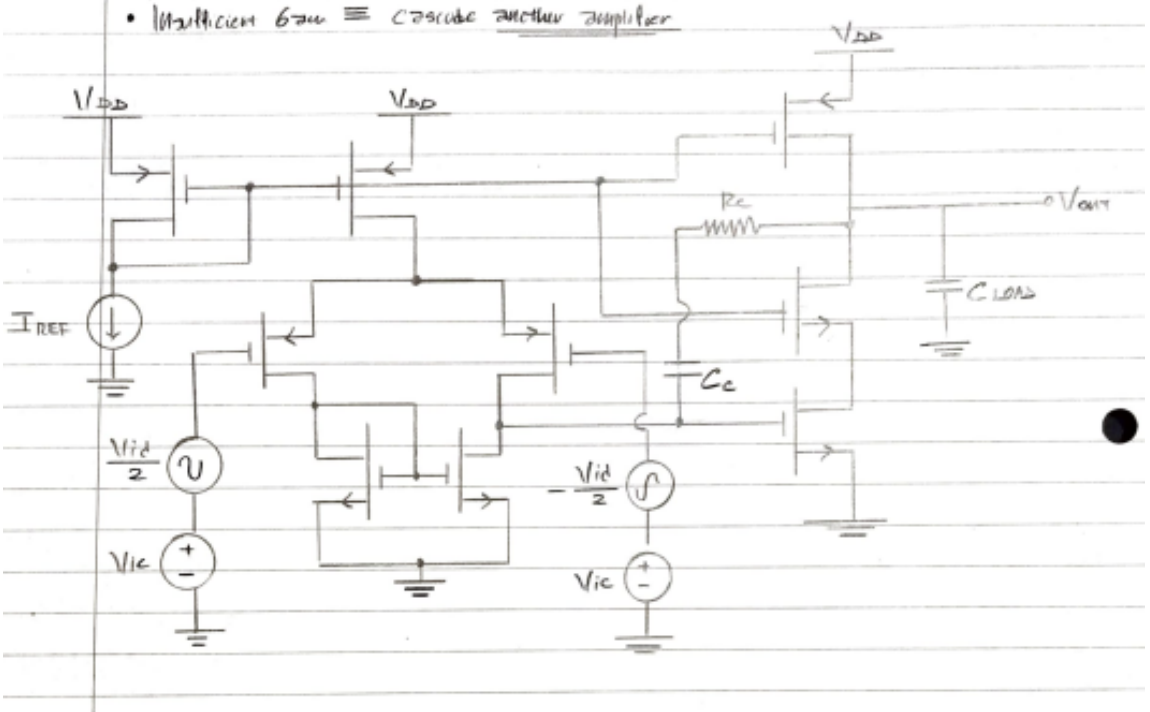
Transient

- Voltage swing > 1V peak to peak ⟹ V_{DD} / V_{OD8} / V_{out} / V_{OD7}, set $V_{out} = 0.9V$
- $V_{OFFSET} < 1mV$
- Differential $G_{DM} > 72\,dB = 10000\,V/V$ ⟹ $\frac{V_{OUT,\,PEAK\,TO\,PEAK}}{V_{IN1} - V_{IN2}} = 10000$, set $V_{OUT,\,PEAK\,TO\,PEAK} = 1.2V$, $V_{IN1} - V_{IN2} = 1.2\times10^{-4}V = 0.12mV$
- CMRR > 70 dB ⟹ $20\log_{10}\left(\frac{A_{DC}}{A_{CM}}\right) = 90\,dB$, $A_{CM} = 1$
- $\frac{\text{MAX } G_{DM}}{DC\ G_{DM}} < 1.5\,dB$

AC

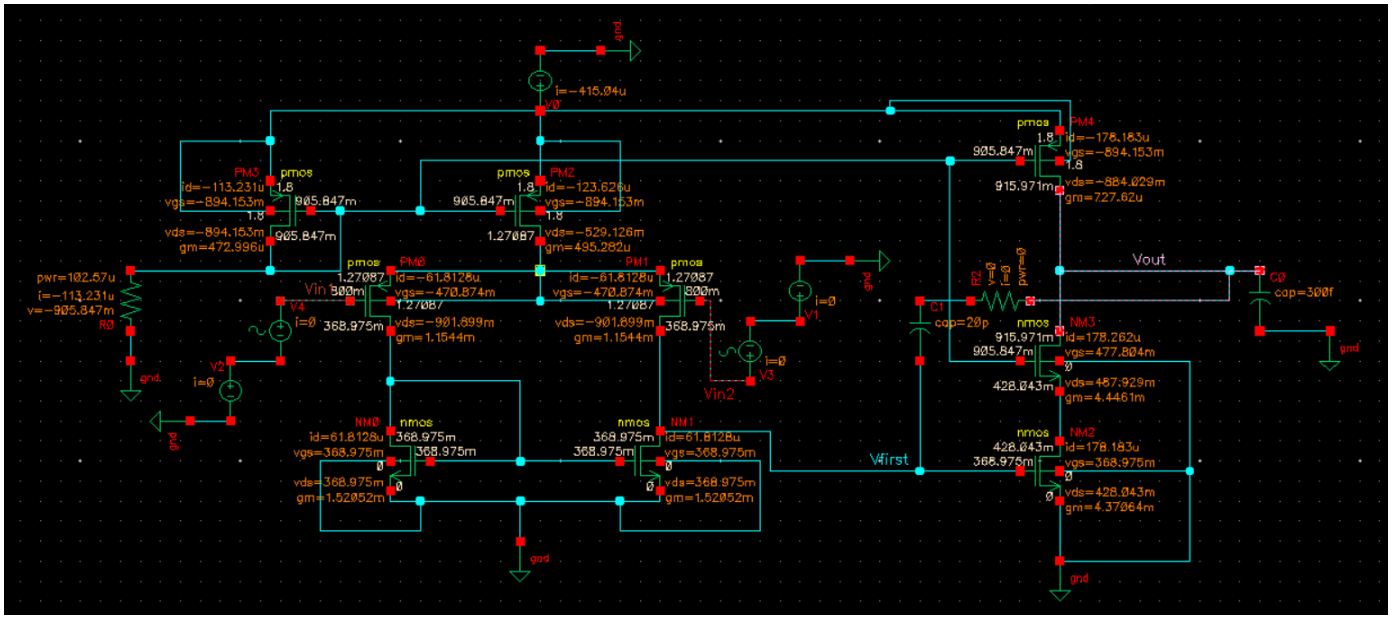
- Unity G_{DM} Bandwidth $f_u > 1MHz$
  → $\omega_u = 2\pi \cdot f_u \approx 38M$ rads^{-1} ⟹ $\omega_u \approx \frac{g_{m2}}{C_c}$, $C_c = \frac{g_{m2}}{\omega_u} \approx \frac{300\times10^{-6}}{38M\,Hz} \approx 7\times10^{-12}F$
  → $f_{3dB} = \frac{f_u}{A_{DC}} = 1900\,Hz$
  → choosing $\omega_z \approx 1.2\cdot\omega_u = 45.6M$ rads^{-1}
  → $R_c \approx \frac{1}{g_{m3}}\left(\frac{C_c + C_2}{C_c}\right) \approx 1300\Omega$
- Phase Margin > 60°

- Multiplicem G_{DM} ≡ Cascade another Amplifier



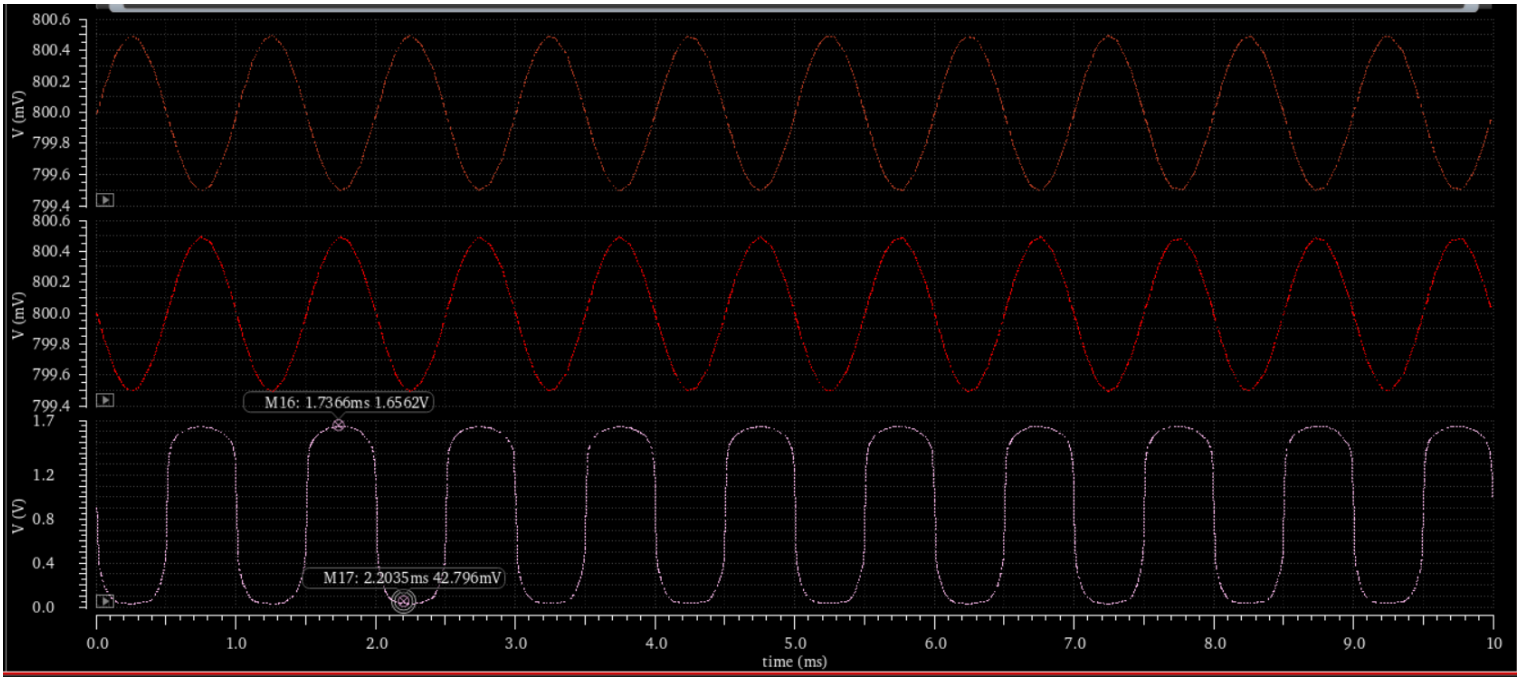
CADENCE SIMULATION

1. Ensure transistors in saturation (DC Analysis)



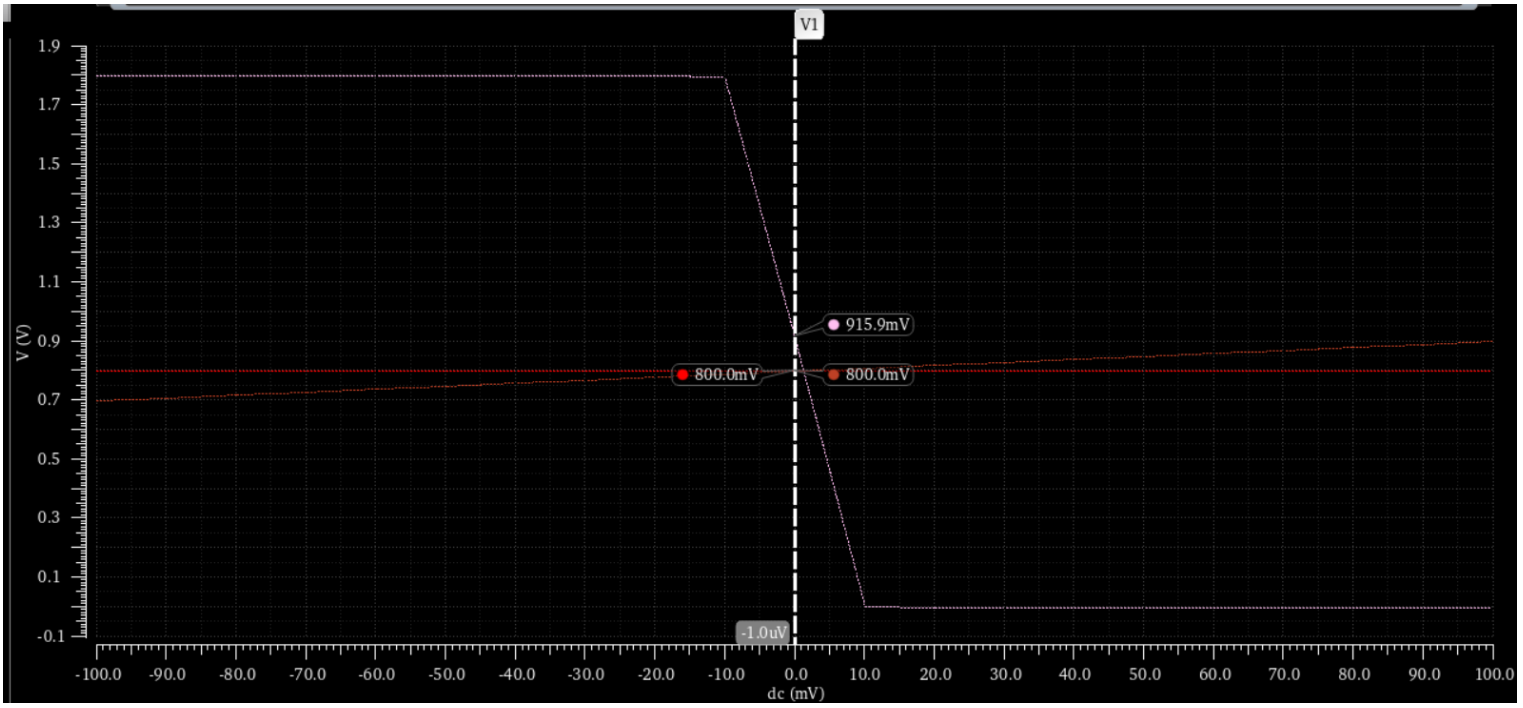
- **Supply Current = 415.04uA < 600uA *(meets specifications)***

2. Determining Output Voltage Swing (Transient Analysis)



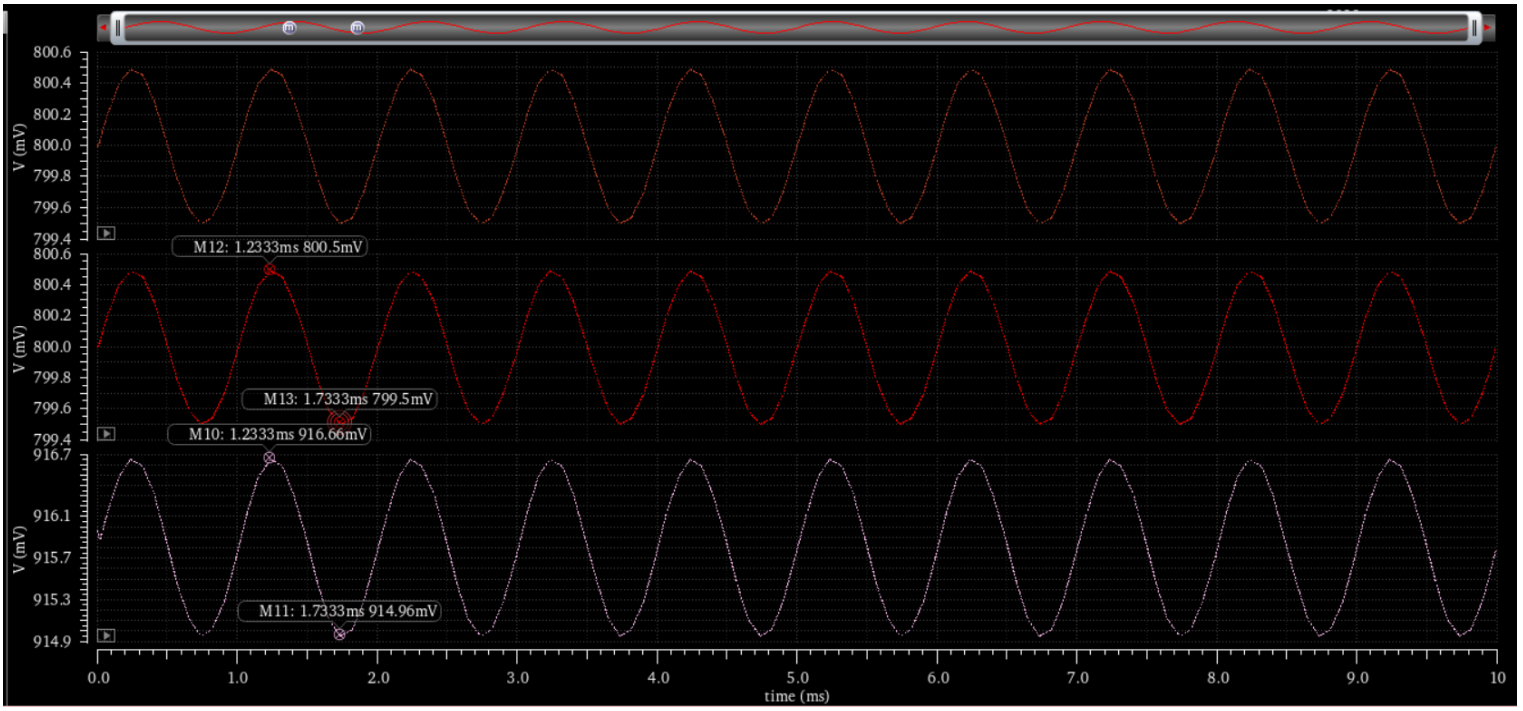
- Introduce sinusoidal inputs of same magnitude (1mV) and opposite phase at Vin1 and Vin2 ports
  - **Output Voltage Swing (peak to peak) ≈ 1.656V - 0.042V = 1.614V > 1V *(meets specifications)***

3. Determining Offset Voltage (DC Sweep Analysis)



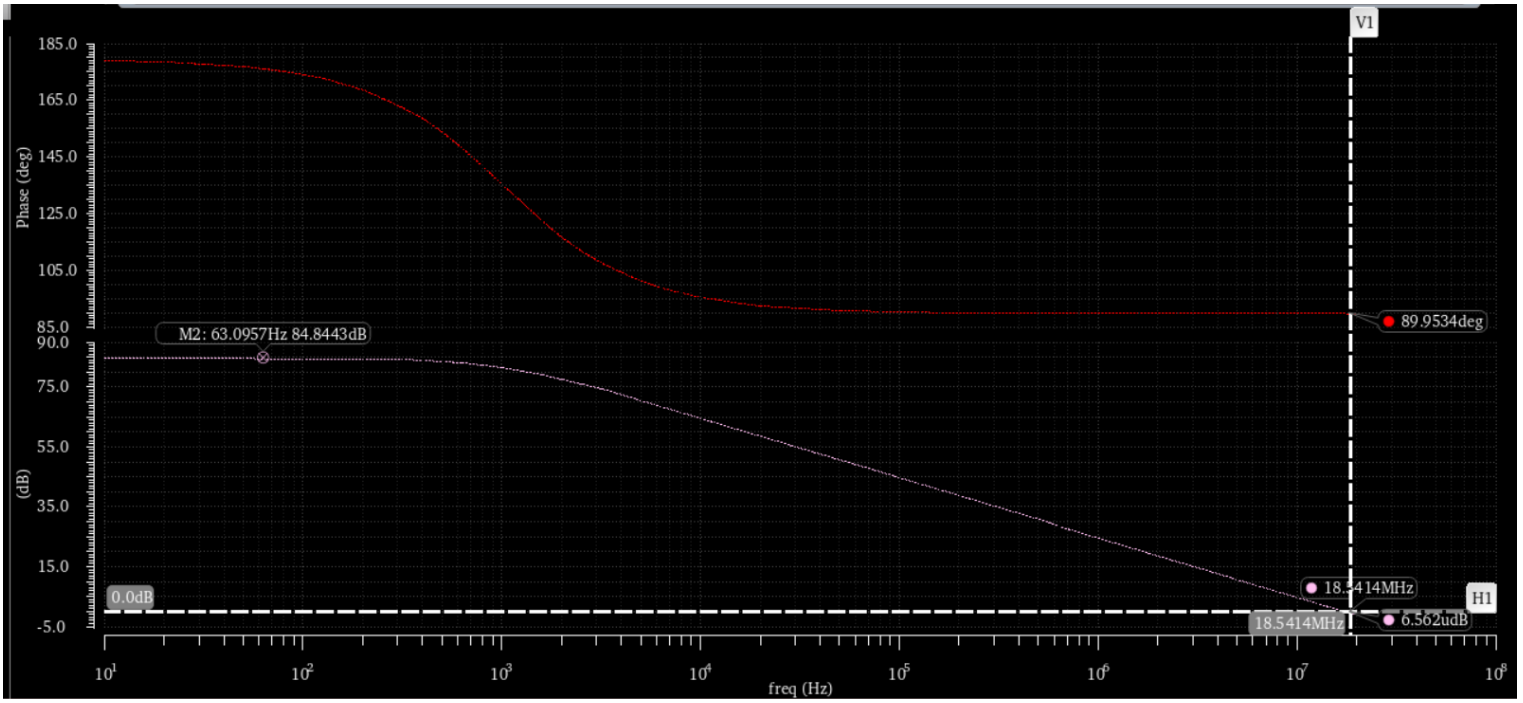
- Provide Vcommon-mode at input port Vin1, and proceed to DC sweep at input port Vin2
    - When Vin1 - Vin2 = -1nV, equals to DC output voltage (915.971mV, as seen in part 1)
    - Hence, **Offset Voltage = -1nV < 1mV (meets specifications)**

4. Determining Common Mode Gain (Transient Analysis)



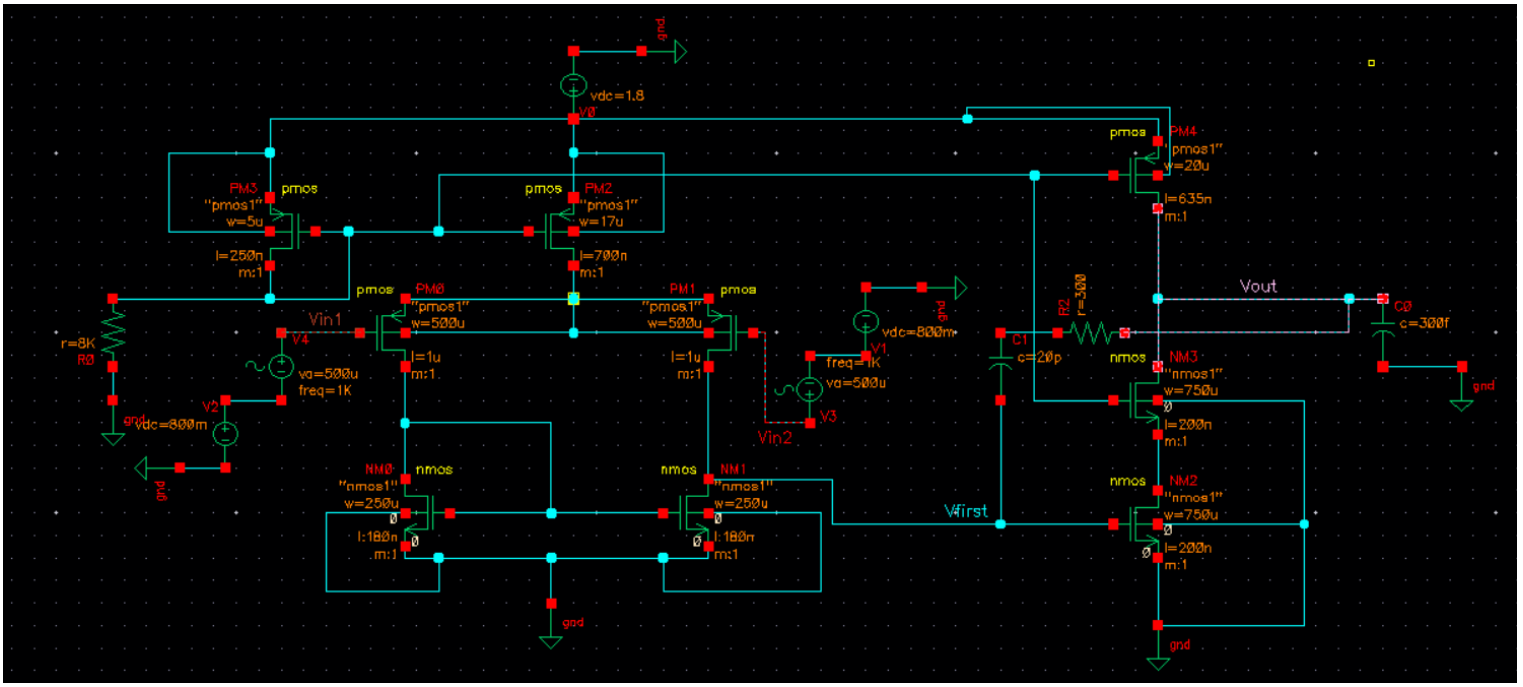
- Introduce sinusoidal inputs of same magnitude (1mV) and same phase (0 degrees) at Vin1 and Vin2 ports
    - Determining Common Mode Gain
        - Vout (peak to peak) ≈ 916.66mV - 914.96mV = 1.7mV
        - Vin (peak to peak) = 1mV
        - Common Mode Gain = Vout / Vin = 1.7V/V

5. Frequency Characteristics (AC Analysis)



- Differential Gain = **Open Loop DC Gain = 84.8443dB *(read from plot)* > 72dB (meets specifications)**
- **Gain Peaking = maximum gain / DC Gain ≈ 84.8443dB / 84.8443dB = 1dB < 1.5dB (meets specifications)**
- **Unity Gain Bandwidth = 18.5414MHz *(read from plot)* > 18Mhz (meets specifications)**
- **Phase Margin ≈ 90 *(read from plot)* > 60 degrees (meets specifications)**
- **CMRR = 20 * log(Open Loop Gain / Common Mode Gain)**
  = Open Loop Gain in dB - 20*log(Common Mode Gain)
  = 84.8443dB - 20*log(1.7)
  = 80.2dB > 70dB (meets specifications)

APPENDIX (SCHEMATIC)



- **Transistors do not exceed maximum width of 1000um *(specification met)***
- ***Output Load Capacitance = 0.3pF (specification met)***
- ***Supply Voltage = 1.8V (specification met)***