EE4415 - Homework 1

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1 DC Characterization

1.1 V_{out} within 1% of $V_{in} = 0.6V$

Using the formula $\frac{(\frac{W}{L})_p}{(\frac{W}{L})_n} = \frac{k'_n V_{DSATn}(V_m - Vthn - \frac{V_{DSATn}}{2})}{k'_p V_{DSATp}(V_{DD} - Vm - |V_{thp}| - \frac{|V_{DSATp}|}{2})} \approx \frac{(V_m - Vthn - \frac{V_{DSATn}}{2})}{(V_{DD} - Vm - |Vthp| - \frac{|V_{DSATp}|}{2})}$.

Then, assuming we are working with long channel devices, we get $V_{DSAT} = V_{gs} - Vth$.

Looking at the *NMOS_VTG.inc* and *PMOS_VTG.inc* files, we get $V_{thn} = 0.4356$ and $V_{thp} = 0.3842$.

Therefore, we get $\frac{(\frac{W}{L})_p}{(\frac{W}{L})_n} \approx 0.6$. We size the transistors as $\frac{(\frac{W}{L})_p}{(\frac{W}{L})_n} = \frac{(\frac{30n}{250n})_p}{(\frac{50}{250})_n}$

Sizing the transistors as such, we attain the following VTC curve with V_m too far left.

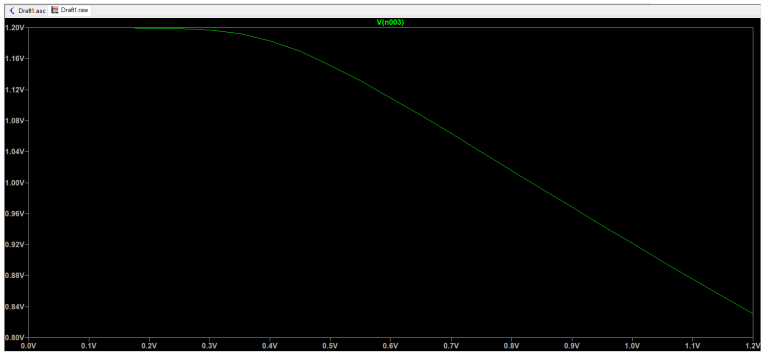


Figure 1: VTC of inverter (Initial attempt)

To rectify this, we must make the PMOS stronger. Assuming L is fixed, we do this by increasing width of PMOS. We resize the transistors as $\frac{(\frac{W}{L})_p}{(\frac{W}{L})_n} = \frac{(\frac{73n}{250n})_p}{(\frac{50}{250})_n}$.

Sizing the transistors as such, we attain the following VTC curve with V_m as desired.

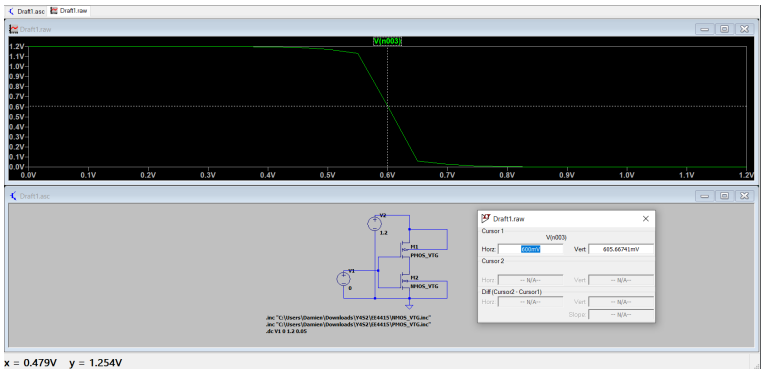


Figure 2: VTC of inverter, fufilling requirements

1.2 I_{supply} vs V_{in}

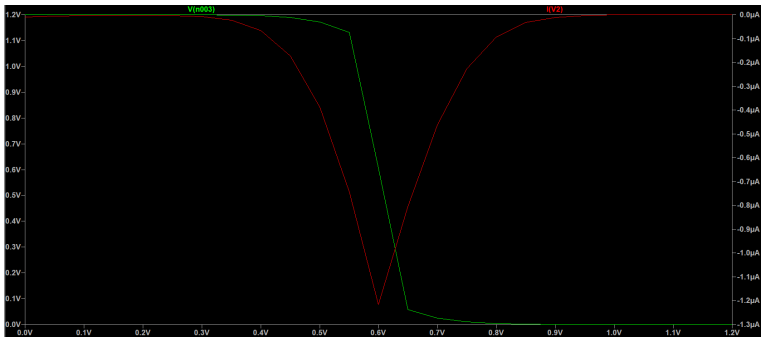


Figure 3: IV graph of Inverter

1.3 Determining VTC characteristics

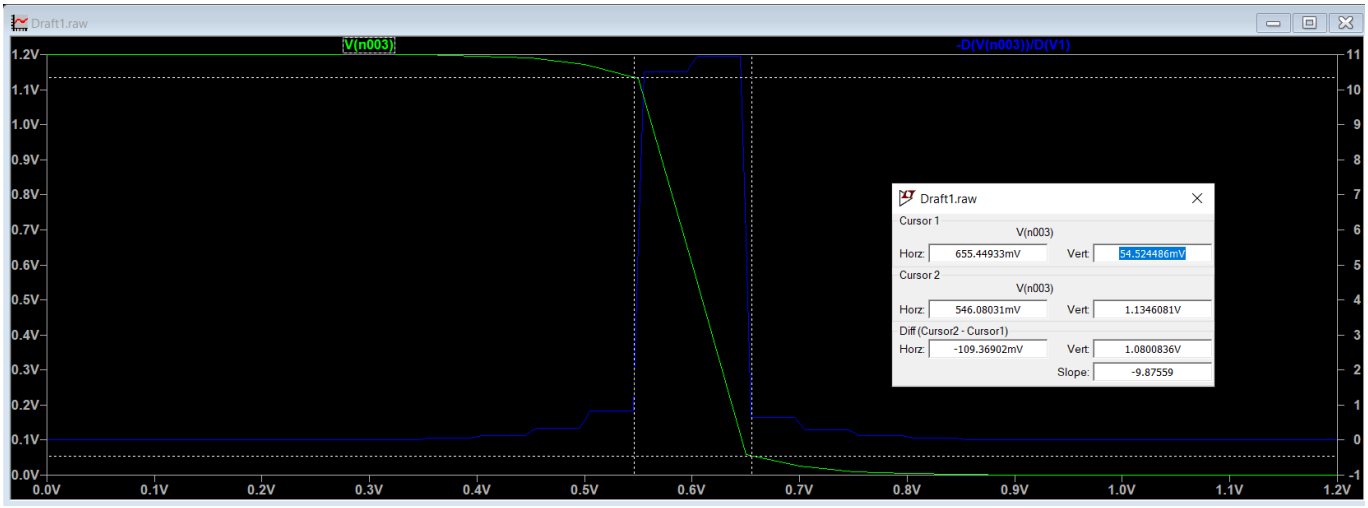


Figure 4: IV graph of Inverter

- V_{IL} and V_{IH} are obtained when the gradient of VTC curve is -1. Accordingly, we have plotted the gradient in blue. Reading off the graph's cursors, we have that $V_{IL} = 546.1mV$ and $V_{IH} = 655.4mV$.
- V_{OL} and V_{OH} are the corresponding y-values of V_{IL} and V_{IH}. Reading off the graph's cursors, we have that $V_{OL} = 54.52mV$ and $V_{OH} = 1.135V$.

2 Transient Characterization

2.1 Construct 2-stage inverter chain

We construct the 2-stage inverter chain as below, adding in some capacitances to model C_{Gin} of the MOSFETS.

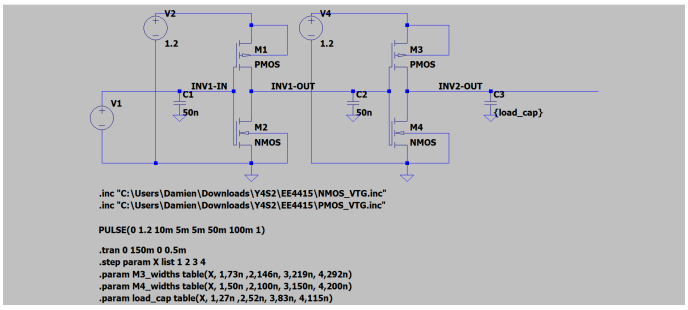


Figure 5: LTSPICE Schematic

2.2 Finding capacitance to balance t_p between stages

We have the formula for time propagation of the j^{th} stage: $t_{p,j} = t_{p0}(1 + \frac{C_{G,IN,j+1}}{C_{G,IN,j} * \gamma})$.

For the following derivations below, we assume $\gamma \approx 1$.

Therefore, it is desired that we have $\frac{t_{p2}}{t_{p1}} = \frac{1+\frac{C_{LOAD}}{C_{G,IN2}}}{1+\frac{C_{G,IN2}}{C_{G,IN1}}} = 1.001$.

We can rewrite the equation as $1.001(1 + \frac{C_{G,IN2}}{C_{G,IN1}}) = 1 + \frac{C_{LOAD}}{C_{G,IN2}}$.

Furthur simplifying, we attain the equation $C_{LOAD} = [1.001(1 + n) - 1] * C_{G,IN2}$, where $n = \frac{C_{G,IN2}}{C_{G,IN1}}$.

After plugging in and tweaking C_{LOAD} values, we execute a *.step* simulation to observe the propagation delays.

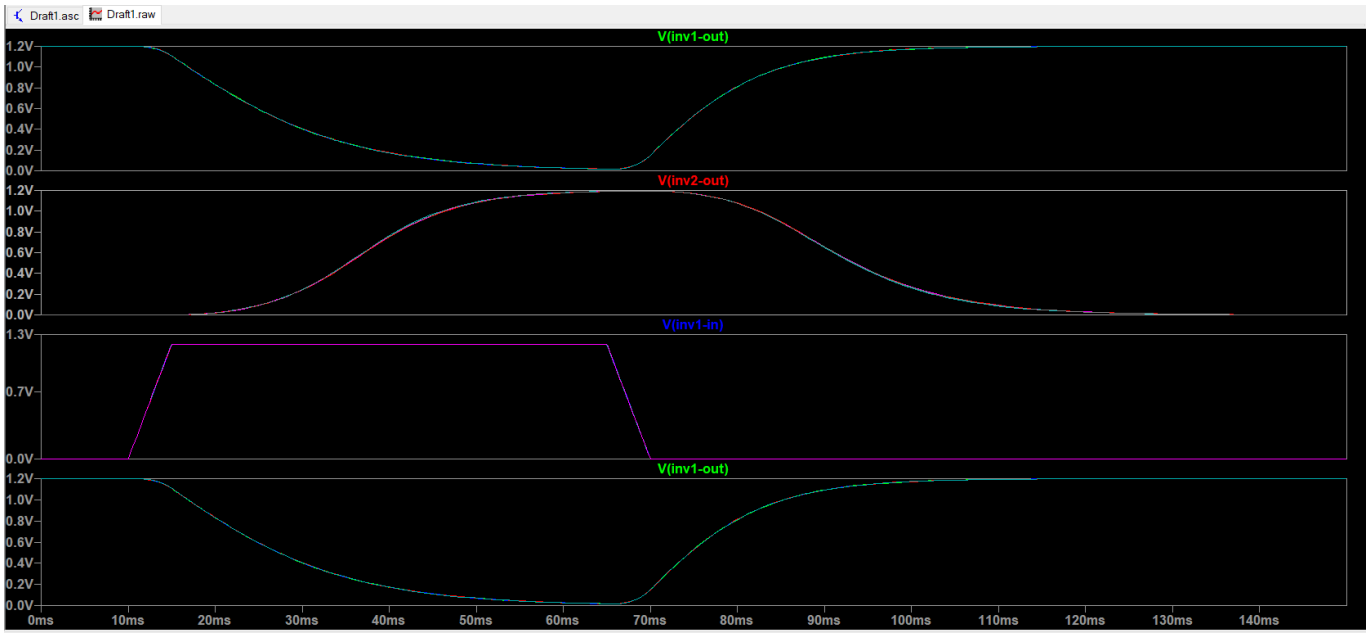


Figure 6: Step Simulation

We can calculate the t_{ph} for the 1^{st} and 2^{nd} invertors as seen below.

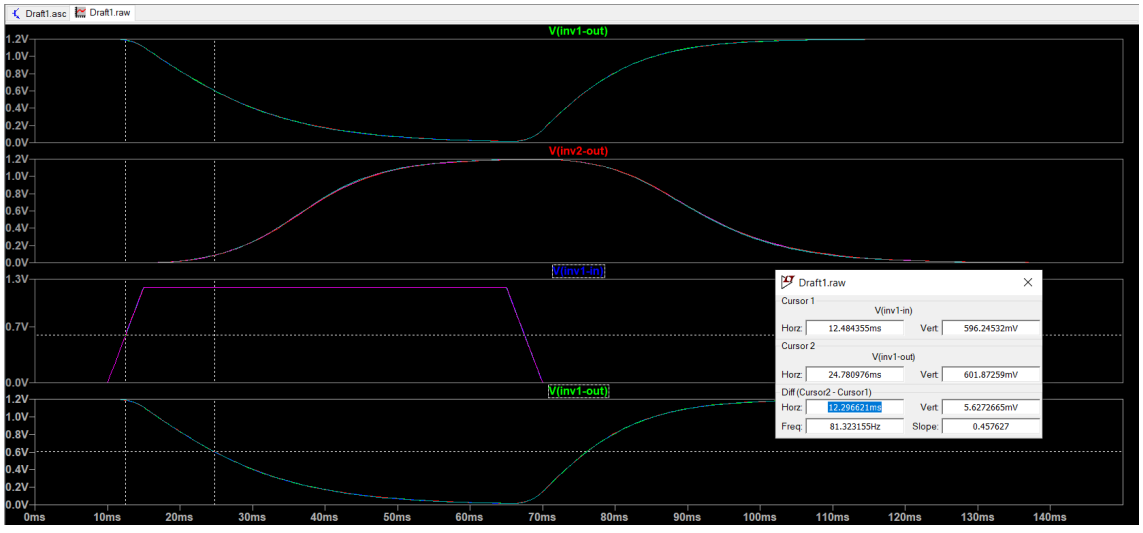


Figure 7: First Inverter, t_{phl}

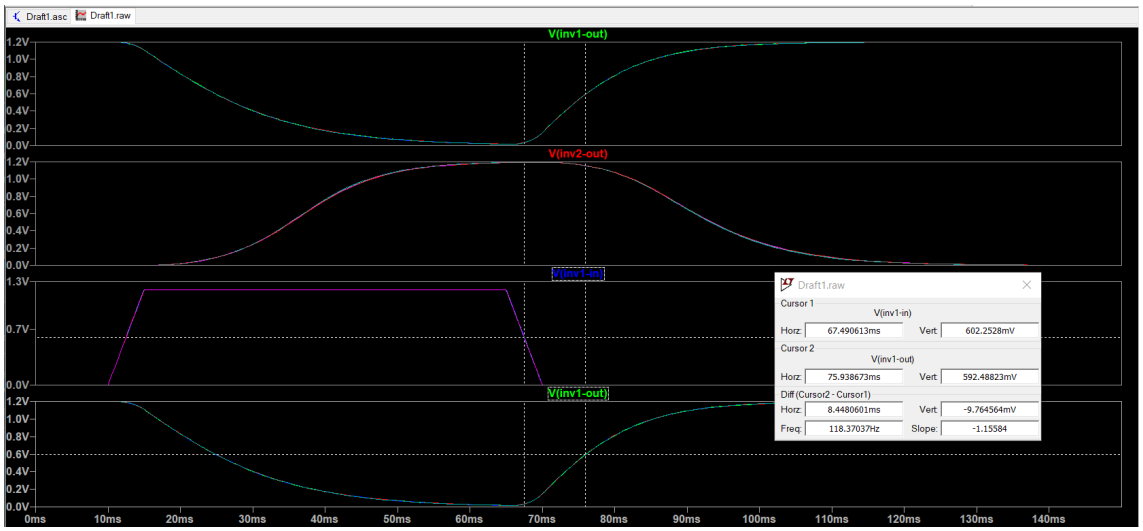


Figure 8: First Inverter, t_{plh}

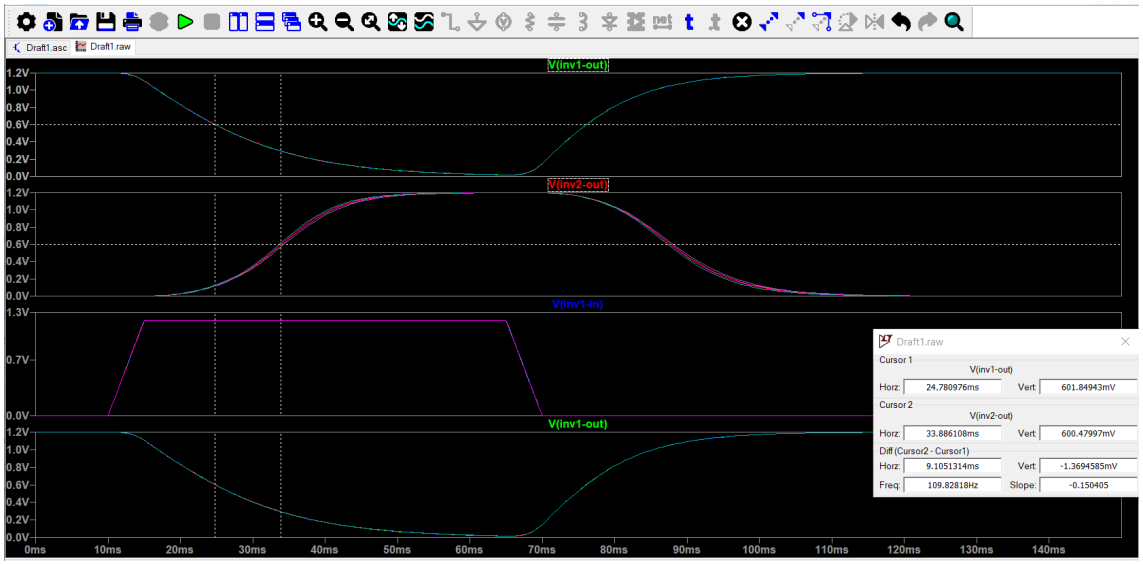


Figure 9: Second Inverter, t_{plh}

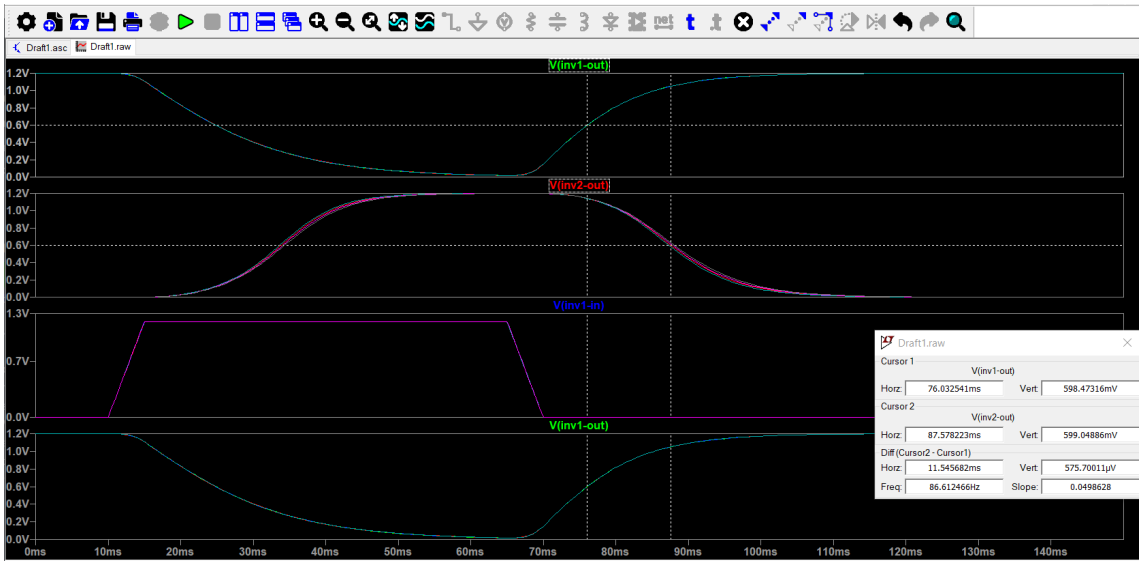
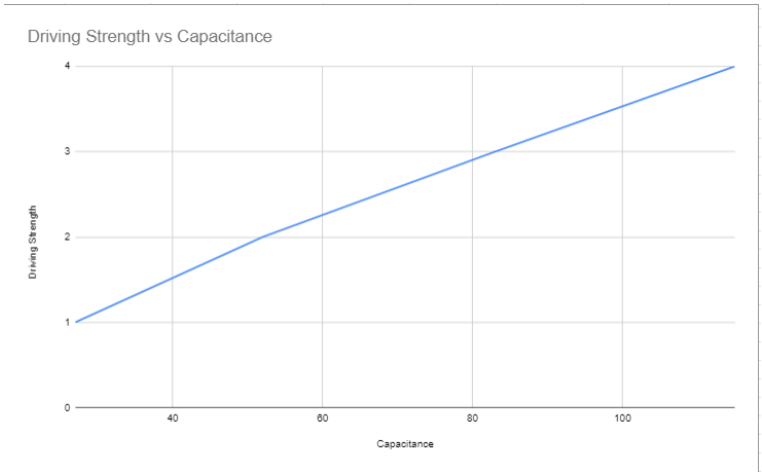


Figure 10: Second Inverter, t_{phl}

Observe that the propagation delay for each stage is within 1% of each other. Therefore, we can plot the driving strength vs capacitance graph.



3 SPICE netlist

```
* C:\Users\Damien\Documents\LTspice\Draft1.asc
V1 INV1-IN 0 PULSE(0 1.2 10m 5m 5m 50m 100m 1)
V2 N001 0 1.2
M1 N001 INV1-IN INV1-OUT N001 PMOS l=250n w=73n
M2 INV1-OUT INV1-IN 0 0 NMOS l=250n w=50n
V4 N002 0 1.2
M3 N002 INV1-OUT INV2-OUT N002 PMOS l=250n w={M3_widths}
M4 INV2-OUT INV1-OUT 0 0 NMOS l=250n w={M4_widths}
C1 INV1-IN 0 50n
C2 INV1-OUT 0 50n
C3 INV2-OUT 0 {load_cap}
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\Damien\AppData\Local\LTspice\lib\cmp\standard.mos
.inc "C:\Users\Damien\Downloads\Y4S2\EE4415\NMOS_VTG.inc"
.inc "C:\Users\Damien\Downloads\Y4S2\EE4415\PMOS_VTG.inc"
.tran 0 150m 0 0.5m
.step param X list 1 2 3 4
.param M3_widths table(X, 1,73n ,2,146n, 3,219n, 4,292n)
.param M4_widths table(X, 1,50n ,2,100n, 3,150n, 4,200n)
.param load_cap table(X, 1,41n ,2,80n, 3,122n, 4,162n)
.backanno
.end
```