1 DRAM operation

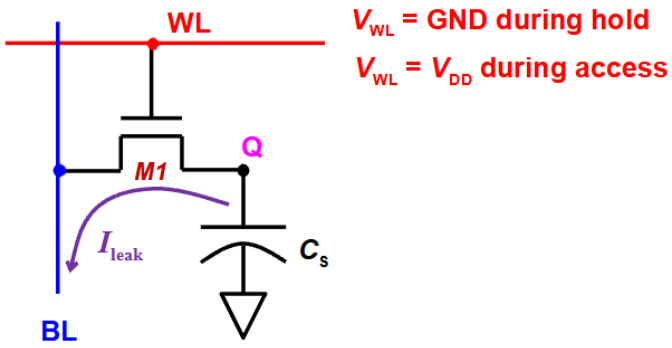

Figure 1: DRAM Bitcell

Operation of DRAM is as follows . . .

- Bitcell is *accessed* to read or write data into the bitcell
  - Electrically connect BL to *storage node* Q
- Otherwise, bitcell is in *hold* mode and retains stored data
  - Affected by leakage current I_{leak}
  - Larger C_s allows for more charge to be stored (and higher data retention time before refresh is required)

1.1 DRAM Write

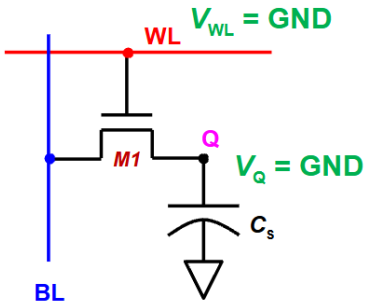

Figure 2: Initial state
WL is off, capacitor charge is zero

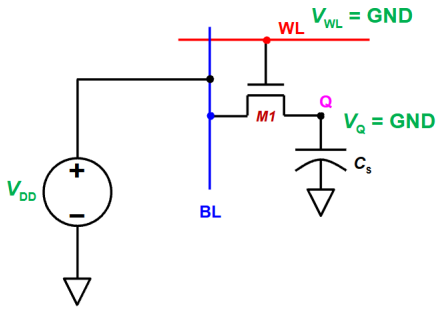

Figure 3: Suppose we want to write **1**
Precharge BL to V_{DD}

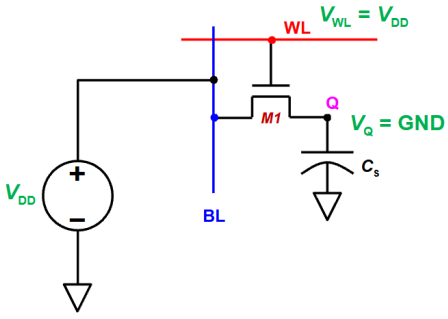

Figure 4: Turn on WL

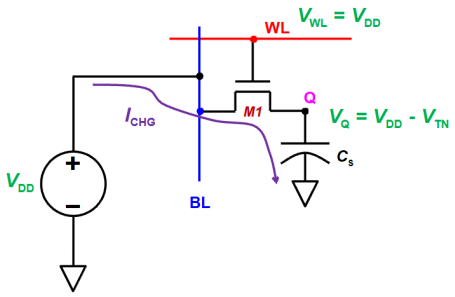

Figure 5: Current flows into C_s
NMOS passes weak 1, therefore V_Q goes up to $V_{DD} - V_{TH}$

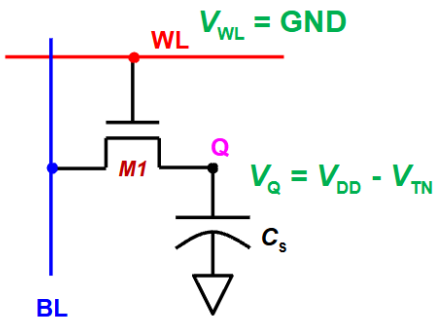

Figure 6: Data successfully written into bitcell
WL can be turned off, voltage at BL can be removed

1.2 DRAM Read

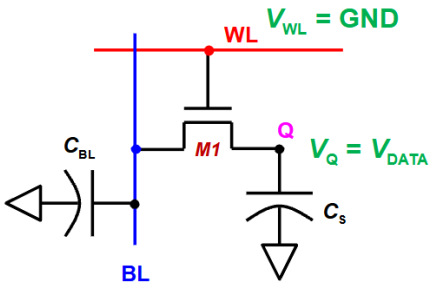

Figure 7: We want to read V_{DATA} stored on V_Q
Notice that there is parasitic C_{BL} on BL

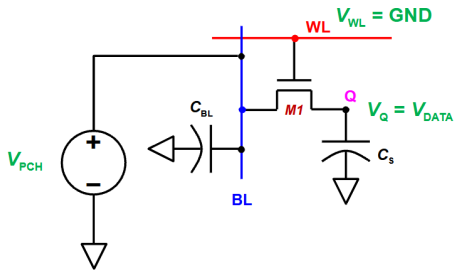

Figure 8: Precharge BL to V_{PCH}
Note that V_{PCH} may be lower than V_{DD}

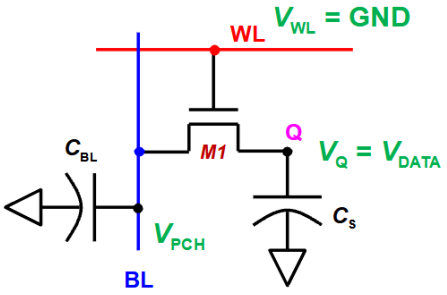

Figure 9: C_{BL} now holds onto V_{PCH}
ie. high impedance node

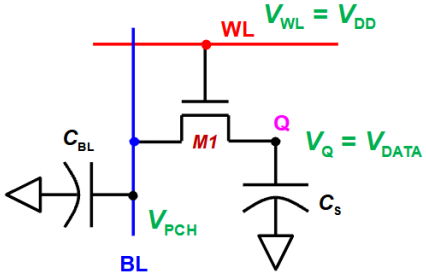

Figure 10: Turn on the WL, short-circuiting C_S with C_{BL}
Charge-sharing occurs

1.2.1 Charge Sharing

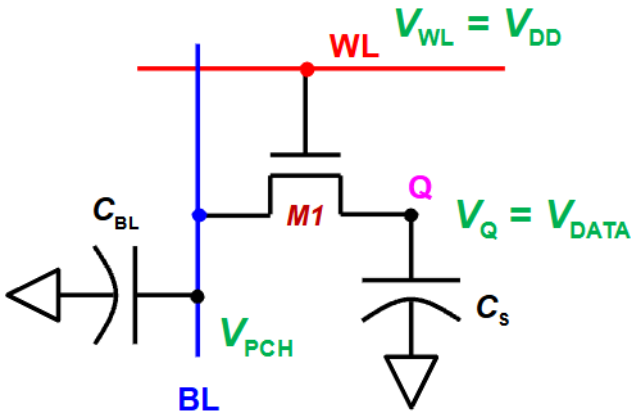

Figure 11: Charge Sharing

- $Q_S = C_S V_{DATA}$
- $Q_{BL} = C_{BL} V_{PCH}$
- $Q_{TOTAL} = Q_{BL} + Q_S$

When M1 turns on ...

- $\Delta V_{BL} = \frac{Q_{TOTAL}}{C_{BL}+C_S} - V_{PCH}$
- $\Delta V_Q = \frac{Q_{TOTAL}}{C_{BL}+C_S} - V_{DATA}$

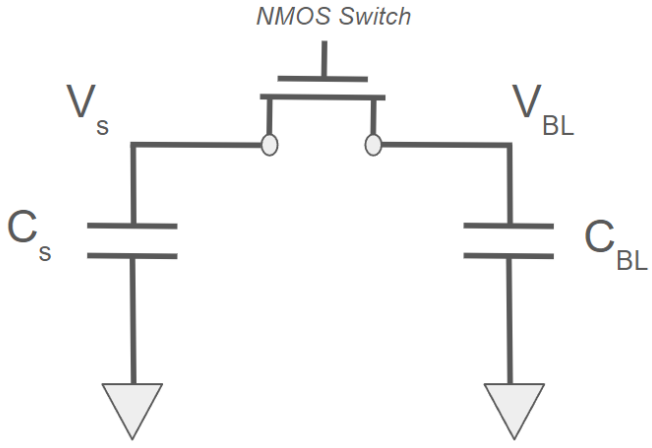

Figure 12: Charge Sharing (Alternative view)

$$\underbrace{C_S V_S + C_{BL}\frac{V_{DD}}{2}}_{\text{Initial charge; NMOS open}} = \underbrace{(C_S + C_{BL})V_{common}}_{\text{After charge sharing; NMOS closed}}$$

- If store **1**, then $V_S = V_{DD}$
- Assume that V_{BL} is precharged to $\frac{V_{DD}}{2}$

We can rearrange the above equation to get ...
$\Delta V_{BL} = V_{common} - V_{BL} = \frac{C_S}{C_S+C_{BL}} \cdot \frac{V_{DD}}{2}$

From this, we can see that we want $C_S >>> C_{BL}$

1.2.2 Sense Amplifier and Writeback

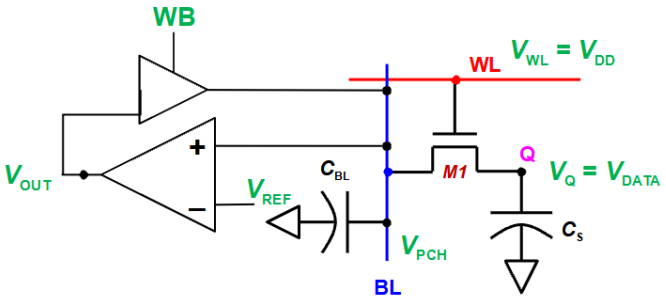

Figure 13: Op-amp with writeback

- V_{REF} must be tuned correctly
- WB ensures that we rectify our destructive read