Dynamic Latches

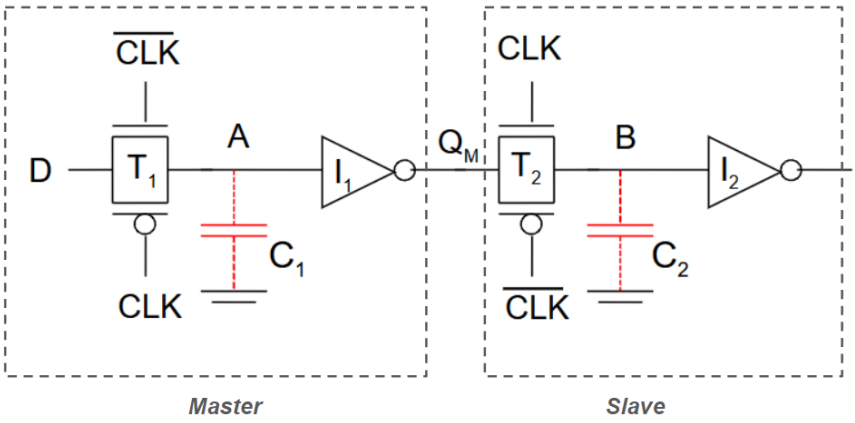
1 Introduction

Dynamic latches are based upon **temporary** storage of charge on parasitic capacitances, as opposed to static latches which utilize feedback.

Hence, periodic refresh of logic value is necessary to overcome any leakage, and reading of stored value should be **non-destructive**.

More advanced dynamic latches such as C^2MOS or $TSPC$ dynamic latches are not covered.

2 Dynamic edge-triggered (ET) register



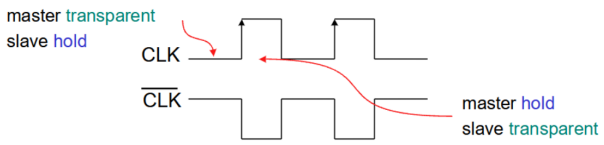


Figure 2: Master-Slave timing

Figure 1: Dynamic ET register
(Positive edge-triggered)

- $t_{setup} = t_{PD,t_1} + t_{INV,I_1}$
- $t_{hold} = 0$
- $t_{clk-q} = t_{PD,t_2} + t_{INV,I_2}$

2.1 Race problems

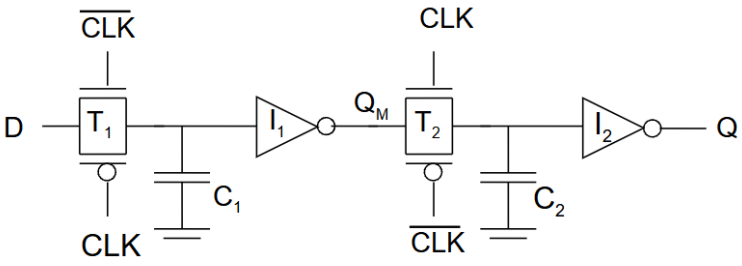


Figure 3: Dynamic ET register

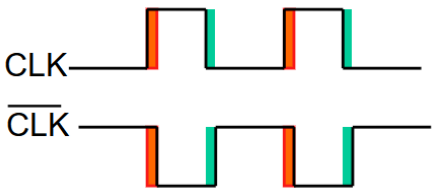


Figure 4: Overlapping clocks
Green=*0-0*, Red=*1-1*

- *0-0* overlap race
  - Suppose $\overline{CLK} = CLK = 0$
  - T_1 turns on (more accurately, PMOS side controlled via CLK will be ON)
    - Master latch goes transparent and samples D
  - However, T_2 **wrongfully** turns on (more accurately, PMOS side controlled via $\overline{CLK}$ will be ON).
    - Slave latch goes transparent and samples Q_M (which is actually D)
  - D therefore wrongly overwrites sampled data on C_2

– **Cannot** be solved by using non-overlapping clocks

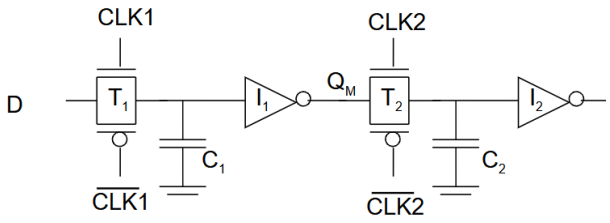


Figure 5: Non-overlapping clocks

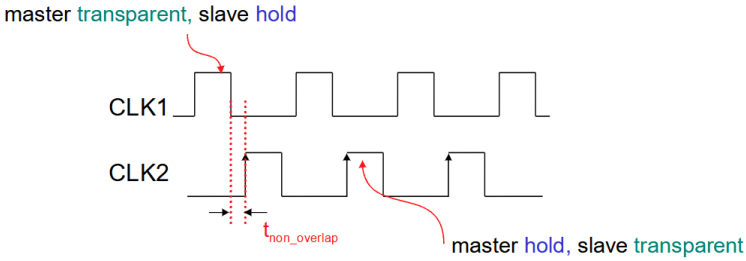


Figure 6: *0-0* overlap still exists

– Can be solved by increasing t_{setup}

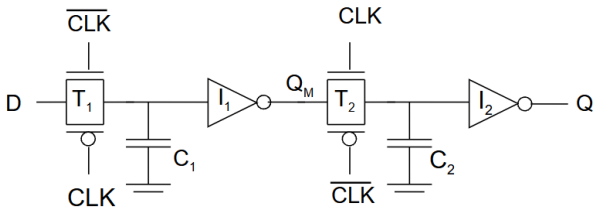


Figure 7: Dynamic ET register

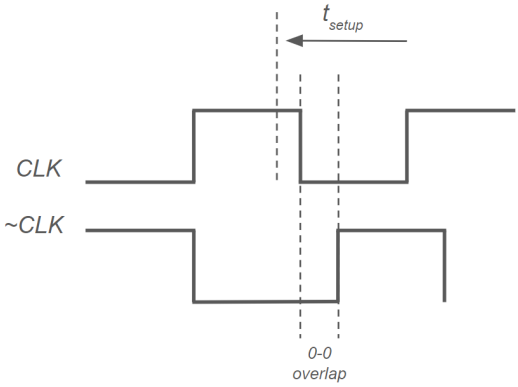


Figure 8: Setup time

∗ T_1 is a **negative** latch, but ET register is **positive** edge-triggered

∗ t_{setup} can be increased by increasing t_{PD,t_1}

∗ Intuitively, we do not allow D to change within the *0-0* overlap period, which solves the issue

∗ Alternatively, we can understand that via increasing t_{PD,t_1}, $D_{sampled}$ from transparent T_1 takes a longer time to travel to T_2. If it takes sufficiently long enough, by the time $D_{sampled}$ reaches T_2, we will already be outside of the *0-0* overlap zone, and T_2 is in hold mode.

- *1-1* overlap race
  - Suppose $\overline{CLK} = CLK = 1$
  - T_1 **wrongfully** turns on (more accurately, NMOS side controlled via $\overline{CLK}$ will be ON)
    ∗ Master latch goes transparent and samples D
    ∗ But, T_2 is currently transparent and sampling from Q_m
    ∗ $D_{sampled}$ may overwrite data on C_1, and corrupt what T_2 is sampling
  - Can be solved by increasing t_{hold}

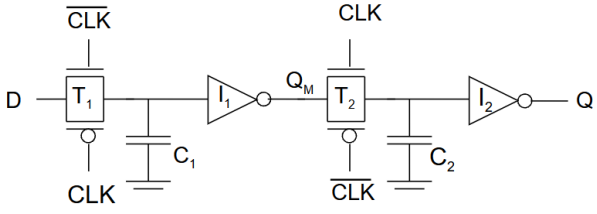


Figure 9: Dynamic ET register

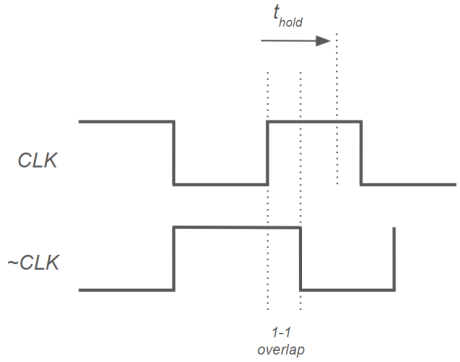


Figure 10: Hold time

∗ D is only allowed to change **after** $\overline{CLK}$ becomes 0