Pipeline Description

Format : .xml

The top-level element :

<!-- pipeline ::= -->

<processor class="otawa::hard::Processor">

<arch>ARCH</arch>(arm ,ppc, sparc, tricore,etc)

<model>MODEL</model>

<builder>BUILDER</builder>

<stages> <!-- stage -->+ </stages>

<queues> <!-- queue -->+ </qeues>

</processor>

ARCH gives the programming model (instruction set, registers, etc) supported by the pipeline.(主要用于检查处理器描述是否支持加载的二进制程序的编程模型)

MODEL represents the accurate model of the hardware: for example, if ARCH is arm, usual models includes armv5t, cortexa8. BUILDER item gives the name of the microprocessor builder like atmel, nxp, etc for an arm architecture.

Stages elements gives the list of stages composing the pipeline（组成pipeline的Stage列表） Notice： list is ordered according to the order of stages in the actual pipeline----The first stage must be of type fetch while the last stage must be of type commit.

The queues represents any pipeline feature storing a set of instructions, that is, FIFO buffer, reorder buffer, etc.