Binary Classification using Logistic Regression

Objective: To classify between Sequential and Combinational circuits using Logistic Regression.

Methodology: We have generated a dataset using circuit simulator to generate netlist which is then converted to cells which are in 2D matrix form. These matrices (cells) are given as input to the model. For example, a simple VLSI cell at circuit level is shown

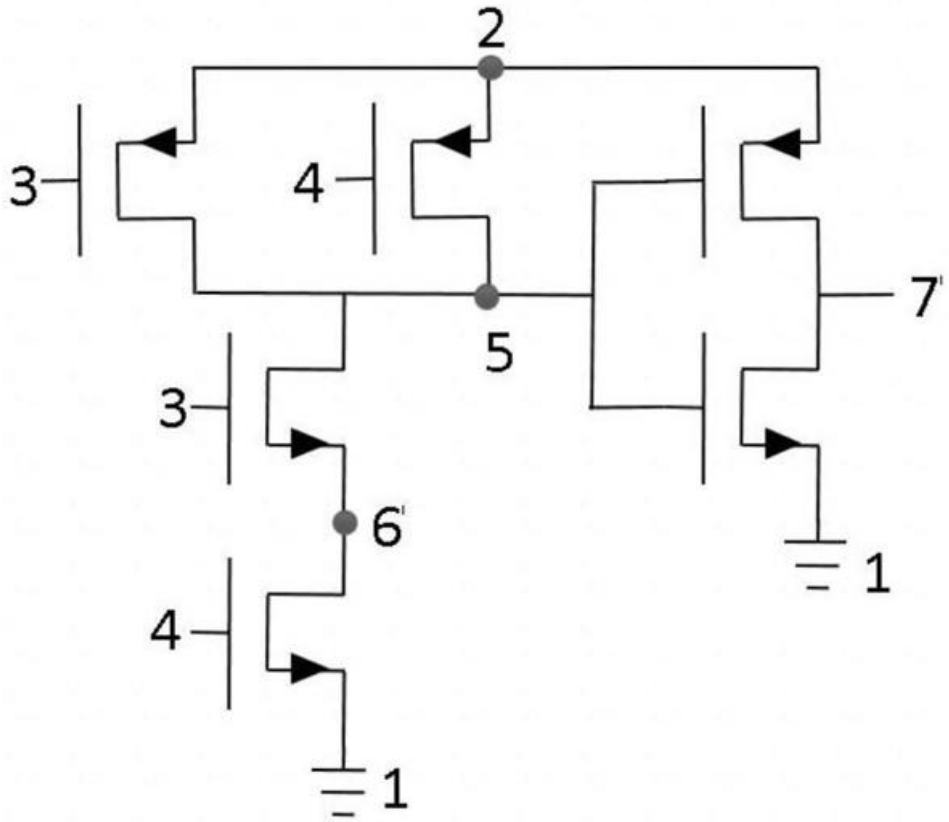

Figure 1 AND gate

These transistor level cells are shown in the form of matrix consisting of 14 different parameters like NMOS and PMOS are represented as 10 and 20 respectively and number 1 and 2 are reserved for special nodes ground and power respectively. Similarly, other parameters show connectivity of the transistor. 80 percent of this set was used in training and 20 percent was reserved as a test set.

*MOS	DRAIN	GATE	SOURCE
20	2	3	5
20	2	4	5
10	5	3	6
10	1	4	6
20	2	5	7
10	1	5	7

Figure 2 Matrix representation of AND gate

The dataset is input in the form of comb dataset and seq dataset. Both these datasets are randomly shuffled and combined into a common dataset. Reshaping and Normalization is done to make the values between -1 and 1. Dataset is divided into training and test data.

In logistic regression, Sequential model is used in which two dense layers are used with SoftMax activation function. The first Dense layer has 28096 (16*1755+16) output parameters and second layer has 3 (2*16+2) output parameters.

Adam optimizer is used along with mean square error to calculate loss.

Output:

Accuracy=1.0

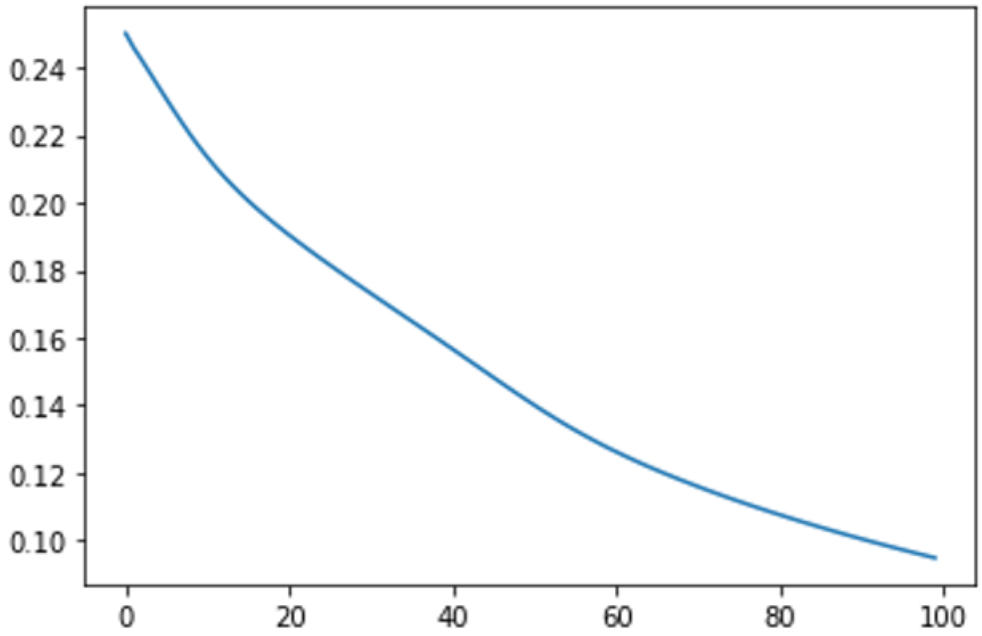

Figure 3 Loss vs Epochs