

Varium C1100 Compute Adaptor User Guide

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Revision History

The following table shows the revision history for this document.

Section	Revision Summary
09/17/2021 Version 1.0	
Initial release.	N/A

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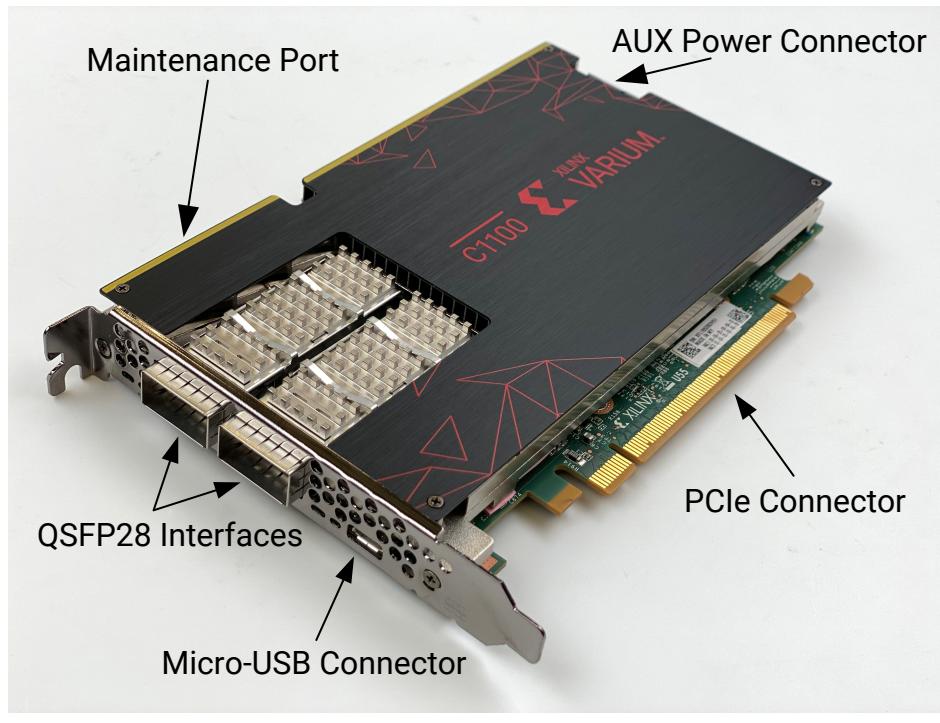
Introduction

The Xilinx® Varium™ C1100 compute adaptor is PCI Express® Gen3 x16 compliant featuring the Xilinx 16 nm UltraScale+™ technology. The Varium C1100 card offers two QSFP28 interfaces and 8 GB of HBM to provide high-performance, adaptable acceleration for memory-bound, compute-intensive applications targeting blockchain applications.

The Varium C1100 is a full-height, half-length card available in a passive cooling configuration only. It is designed for installation into a data center server where controlled air flow provides direct cooling to the card. The following figure shows the Varium C1100 compute adaptor, including the following interfaces:

1. A PCIe® card connector.
2. Two QSFP interfaces.
3. Micro-USB maintenance connector.
4. Maintenance port.
5. AUX power connector.

Figure 1: Varium C1100 Compute Adaptor



X25657-081321



CAUTION! Varium compute adaptors are designed to be installed into a data center server, where controlled air flow provides direct cooling. If the cooling enclosure is removed from the card and the card is powered-up, external fan cooling airflow MUST be applied to prevent over-temperature shut-down and possible damage to the card electronics. Removing the cooling enclosure voids the board warranty.

For additional information about airflow requirements, see the *Varium C1100 Compute Adaptor Data Sheet (DS1003)* for additional information about airflow requirements.

See [Appendix A: Additional Resources and Legal Notices](#) for references to documents, files, and resources relevant to the Varium C1100 compute adaptor.

Card Features

The Varium C1100 card features are as follows.

Table 1: Varium C1100 Features

Card Component	Varium C1100
FPGA	UltraScale+™ XCU55N FPGA
HBM	8 GB - two 4 gigabyte (GB) HBM memory stacks Split into 32 256 MB channels

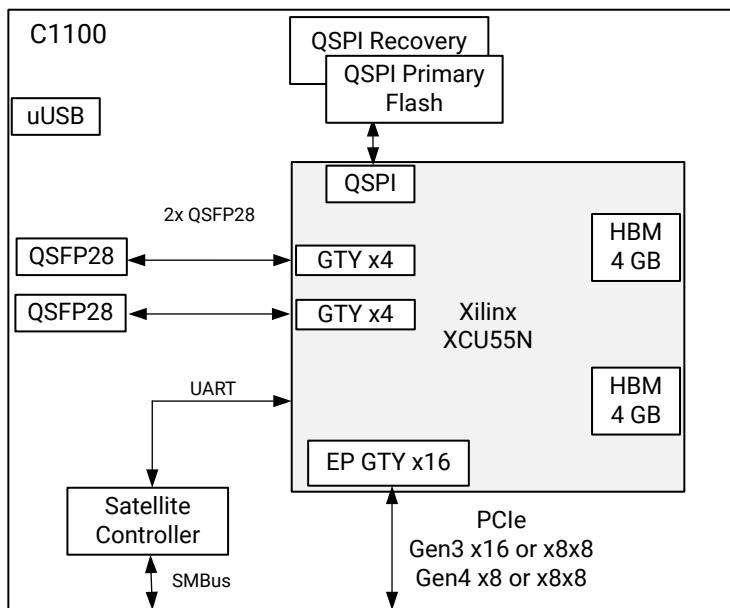
Table 1: Varium C1100 Features (cont'd)

Card Component	Varium C1100
Network Interface	2x QSFP28
	Supporting 100 GbE, 40 GbE, or 4x10/25 GbE
	Status LEDs
PCIe	16-lane PCIe Express
	PCIe Integrated Endpoint block connectivity
	Gen1, 2, or 3 up to x16, Gen4 x8
	Dual Gen4 x8
I2C Bus	✓
Power Management	Power management with system management bus (SMBus) voltage, current, and temperature monitoring
External Power Sources	150W with PCIe auxiliary power connector.
Configuration Options	1 gigabit (Gb) Quad Serial Peripheral Interface (SPI) flash memory
	UltraScale+ device configurable over USB/JTAG and Quad SPI configuration flash memory
UART	UART access through the micro USB connector

Block Diagram

A block diagram of the Varium C1100 card is shown in the following figure.

Figure 2: Varium C1100 Card Block Diagram



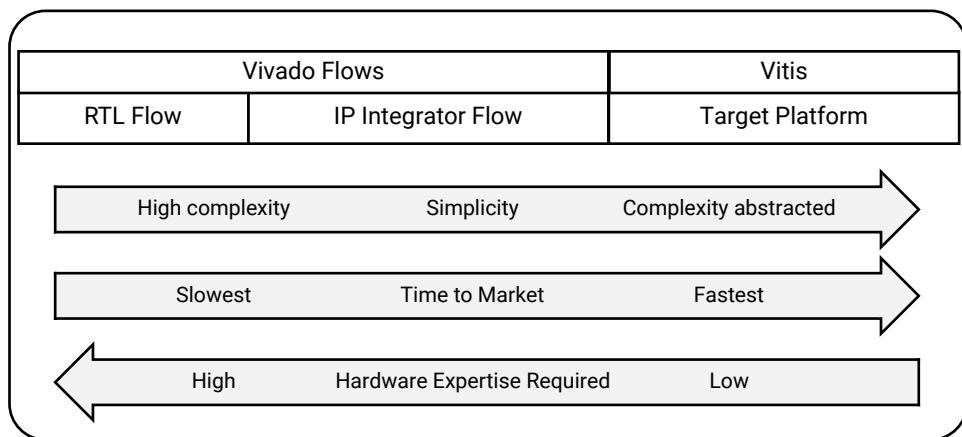
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Note: QSFP0 is port 1, the upper port on the PCIe bracket and QSFP1 is port 2, the lower port on the PCIe bracket, closest to the PCIe card edge fingers.

Design Flows

The following figure shows a summary of the Varium design flows.

Figure 3: Varium Compute Adaptor Design Flows



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Documents related to the different design flows are listed in the following table. Additional details on the Vivado design flow are given in [Chapter 2: Vivado Design Flow](#).

Table 2: Documentation to Get Started with Varium Compute Adaptor Design Flows

	RTL Flow	IP Integrator Flow	Vitis
Vivado tools support	Board support XDC	N/A	N/A
Programming the FPGA	Vivado Hardware Manager	N/A	N/A
Card Installation	UG1525 ¹	N/A	N/A

Notes:

1. *Varium C1100 Compute Adaptor Installation Guide* (UG1525).

Vivado Design Flow

This section provides a starting point for expert HDL developers using the RTL flow using the Vivado® tools.

XDC Files Installation

Prior to creating a Vivado RTL project based on a Varium card, download the XDC files associated with your Varium card from the [Varium Vivado Lounge](#).

Creating a Vivado RTL Project

There are two flows available for the RTL developer; board aware and XDC based flow. In either flow, you can add RTL files or block designs to your project. The steps necessary for creating a project for each flow are described in the following sections.

XDC Based Flow

Use the following steps to create an XDC based Vivado RTL project using the XDC downloaded from the lounge. The XDC is a reference for the static pinout of the Varium card.

Within the XDC based Vivado flow, the Varium parts are not visible in the Vivado part selection window. A project using a Vivado part can only be created using a Tcl command. Use the following steps:

1. Launch Vivado tools.
2. In the Tcl console, run the following command:

```
create_project <project> <path> -part <part number>
```

where,

- <project> is the name of the project you want to create
- <path> is the path where you want to create the project
- <part number> is the Vivado part number as defined in the following table.

Table 3: Vivado Part Number

Varium Card	Varium Part	Vivado Part Number
A-U55N	XCU55N-L2SVH2892E	XCU55N-FSVH2892-2L-E

- Add the card XDC file to the project by clicking on **File → Add Sources → Add or Create Constraints**. Click **Next**. Select **Add Files**. Navigate to the location of the XDC file and click **OK**.
-

UltraScale+ Device Configuration

The Varium C1100 compute adaptor supports two UltraScale+™ FPGA configuration modes:

- Quad SPI flash memory
- JTAG (through USB maintenance port)

The FPGA bank 0 mode pins are hardwired to M[2:0] = 001 master SPI mode with pull-up/down resistors.

At power up, the FPGA is configured by the QSPI NOR flash device (Micron MT25QU01GBBB8E12-0AAT) with the FPGA_CCLK operating at a clock rate of up to 63.8 MHz using the master serial configuration mode.

If the JTAG cable is plugged in, QSPI configuration might not occur. JTAG mode is always available independent of the mode pin settings.

For complete details on configuring the FPGA, see the *UltraScale Architecture Configuration User Guide* ([UG570](#)).

Table 4: Configuration Modes

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	FPGA output
JTAG	Not applicable – JTAG overrides	x1	Not applicable

MCS File Generation and Varium Card Programming

This section outlines the steps to generate and program the MCS file.

MCS File Generation

The MCS file is the PROM image which is loaded onto the Varium compute adaptor at power ON. It is generated using the write_cfmem tool. This section outlines the steps to generate and program the MCS file.

Prior to generating the MCS file, ensure your project XDC file sets the following properties. You can use the XDC file in the [Varium Vivado Lounge](#) for reference.

- CONFIG_VOLTAGE
- BITSTREAM.CONFIG.CONFIGFALLBACK
- BITSTREAM.GENERAL.COMPRESS
- CONFIG_MODE
- BITSTREAM.CONFIG.SPI_BUSWIDTH
- BITSTREAM.CONFIG.CONFIGRATE
- BITSTREAM.CONFIG.EXTMASTERCLK_EN
- BITSTREAM.CONFIG.SPI_FALL_EDGE
- BITSTREAM.CONFIG.UNUSEDPIN
- BITSTREAM.CONFIG.SPI_32BIT_ADDR

Use the following command line with the parameters outlined in [Table 5](#) to generate the MCS file.

```
write_cfmem -force -format mcs -interface <interface_type> -size <size> -
loadbit "up <user_config_region_offset> <input_file.bit>" -file
"<output_file.mcs>"
```

Table 5: write_cfmem Parameter Settings

write_cfmem Parameter	Setting
interface_type	spix4
user_config_region_offset ¹	0x01002000
size	128
input_file.bit	Filename of the input .bit file
output_file.mcs	MCS output filename

Notes:

- Address 0x00000000 through 0x01001FFF is a write protected region which holds the card's golden recovery image and cannot be written to. The user_config_region_offset setting cannot be within this range.

For additional details on write_cfmem, see the *UltraScale Architecture Configuration User Guide (UG570)*.

Program the Varium Card

After the MCS file has been generated, use the following steps to flash the Varium compute adaptor using the Vivado hardware manager. Detailed steps for programming the FPGA are outlined in the chapter Programming the FPGA Device in the *Vivado Design Suite User Guide: Programming and Debugging* ([UG908](#)).



RECOMMENDED: *Programming through JTAG maintenance port must be from a separate machine to avoid PCIe downlink causing the server to reboot during programming. Alternatively, the PCIe link can be manually disabled through software and rescanned after programming is complete.*

1. Connect to the Varium C1100 compute adaptor using the Vivado hardware manager via the maintenance connector or micro-USB port. Details on connecting to the Varium card through the maintenance connector are provided in the *Alveo Programming Cable User Guide* ([UG1377](#)).
2. Select **Add Configuration Device** and select the mt25qu01g-spi-x1_x2_x4 part.
3. Right-click the target to select **Program the Configuration Memory Device**.
 - a. Select the MCS file target.
 - b. Select **Configuration File Only**.
 - c. Click **OK**.
4. After programming has completed, disconnect the card in the hardware manager, and disconnect the JTAG programming cable from the Varium compute adaptor.
5. Perform a cold reboot on the host machine to complete the card update.



IMPORTANT! *If you are switching between an Varium compute adaptor target platform and a custom design, revert the card to the golden image before loading an alternate image into the PROM. See the `factory_reset` command available with `xbmgmt flash`. For more information, see [xbutil \(Next Generation\)](#).*

Card Installation

Standard ESD Measures



CAUTION! ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.

To prevent ESD damage:

- Attach a wrist strap to an unpainted metal surface of your hardware to prevent electrostatic discharge from damaging your hardware.
- When you are using a wrist strap, follow all electrical safety procedures. A wrist strap is for static control. It does not increase or decrease your risk of receiving electric shock when you are using or working on electrical equipment.
- If you do not have a wrist strap, before you remove the product from ESD packaging and installing or replacing hardware, touch an unpainted metal surface of the system for a minimum of five seconds.
- Do not remove the device from the antistatic bag until you are ready to install the device in the system.
- With the device still in its antistatic bag, touch it to the metal frame of the system.
- Grasp cards and boards by the edges. Avoid touching the components and gold connectors on the adapter.
- If you need to lay the device down while it is out of the antistatic bag, lay it on the antistatic bag. Before you pick it up again, touch the antistatic bag and the metal frame of the system at the same time.
- Handle the devices carefully to prevent permanent damage.

Installing Varium Compute Adaptors in Server Chassis

For the hardware installation procedures, see the *Varium C1100 Compute Adaptor Installation Guide* (UG1525).

Because each server or PC vendor's hardware is different, for physical board installation guidance, see the manufacturer's PCI Express® board installation instructions.

Card Component Description

This chapter provides a functional description of the components of the Varium C1100 compute adaptor.

UltraScale+ Device

The Varium C1100 compute adaptor is populated with the 16 nm UltraScale+™ XCU55N FPGA.

This UltraScale+ HBM device incorporates two 4 GB high-bandwidth memory (HBM) stacks adjacent to the device die. Using SSI technology, the device communicates to the HBM stacks through memory controllers that connect through the silicon interposer at the bottom of the device. Each XCU55N FPGA offers 8 GB of HBM in two 4 GB stacks. The device includes 32 HBM AXI interfaces used to communicate with the HBM allowing any of the 32 HBM AXI interfaces to access any memory address on either of the HBM stacks. This flexible connection between the device and the HBM stacks is helpful for floorplanning and timing closure.

Quad SPI Flash Memory

The Quad SPI device provides 1 Gb of nonvolatile storage.

- Supply voltage: 1.8V
- Datapath width: 4 bits
- Data rate: 63.8 MHz

For more flash memory details, see the Micron MT25QU01GBBB8E12-0AAT data sheet at the Micron website.

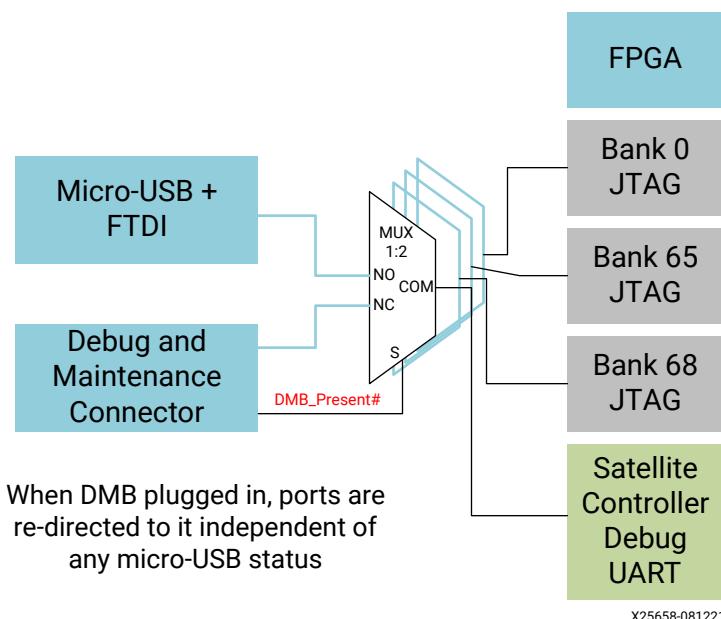
For configuration details, see the *UltraScale Architecture Configuration User Guide (UG570)*. The detailed FPGA and Flash pin connections for the feature described in this section are documented in the Varium C1100 compute adaptor XDC file found in the [Varium Vivado Lounge](#).

Maintenance Connector Interface

The Varium C1100 compute adaptor provides access to the FPGA through the JTAG interface using the Alveo programmable cable connected to the 30-pin maintenance connector or micro-USB port on ES Cards. Multiplexing control is automatic: when no Varium programmable cable is plugged to the maintenance connector, all interfaces are connected to micro-USB port. When Varium programmable cable is plugged in, all interfaces are re-directed to it.

The maintenance connector pinout supports three UART debug interfaces: PMBus, FPGA JTAG, and satellite controller JTAG. The following figure shows the maintenance connector interface. For more information, see *Alveo Programming Cable User Guide (UG1377)*.

Figure 4: Maintenance Connector



PCI Express Endpoint

The Varium C1100 compute adaptor implements a 16-lane PCI Express edge connector that performs data transfers at the rate of 2.5 giga-transfers per second (GT/s) for Gen1, 5.0 GT/s for Gen2, 8.0 GT/s for Gen3 applications, and 16.0 GT/s for Gen4 applications.

The detailed FPGA connections for this feature are documented in the Varium C1100 compute adaptor XDC file found in the [Varium Vivado Lounge](#). The endpoint is compliant to the v3.0 specification, and compatible with the specification. For additional information about Gen4 compatible features, see *UltraScale+ Devices Integrated Block for PCI Express LogiCORE IP Product Guide* ([PG213](#)).

QSFP Module Connectors

The Varium C1100 compute adaptors host two small form-factor pluggable (QSFP) connectors that accept an array of optical modules. Each connector is housed within a single cage assembly and are accessible through the I2C interface.

Access from the FPGA to QSFP modules and support for miscellaneous QSFP signals is provided through the satellite controller. For more information about the QSFP module, see [QSFP Specification](#).

- MGTREFCLK0 is from SI5394 with programmable output frequencies
- Maximum QSFP power is 3.5W per port
- The target for QSFP channel length is 4 inches maximum

Detailed FPGA connections for this feature are documented in the Varium C1100 compute adaptor XDC file.

I2C Bus

The Varium C1100 compute adaptors implement an I2C bus network to communicate with numerous sensors and voltage regulators on the card. These I2C interfaces are not accessible from the UltraScale+ device and are only accessible via the satellite controller.

Status LEDs

The C1100 has two set of LEDs:

1. Card status LEDs
2. Ethernet status LEDs

Card status LEDs are visible through a cutout in the PCIe end bracket and are defined in the following table.

Table 6: Card Status LEDs

Reference Designator	Description
DS1	When FPGA is configured, LED is blue, otherwise it remains Off
DS2	Not populated
DS3	Not populated
DS4	Not populated

There are two Ethernet status LEDs; one for link and the other for activity. The LED definitions for both the 100G and 4x25G configurations are given below.

- **100G QSFP LED Definition:**

- The Link LED is green when a physical link is present and operating at the highest supported link rate, yellow when operating at lower rates, and OFF in the absence of physical link.
- The Activity LED is ON or blinking to show link activity and OFF when there is no activity.

- **Multiple 4x25G QSFP LED Definition:**

- The Link LED is green when all physical links are present and operating at the highest supported link rate, yellow when any link is operating at a lower rate or is not linked, and OFF in the absence of physical link on all links.
- The Activity LED is ON or blinking to show activity link on any port and OFF when there is no activity on any port.

Card Power System

The Varium C1100 card has separate power rails for FPGA fabric and HBM memory. Developers must ensure their designs do not draw too much power for each rail. For more information, see the [Varium Vivado Lounge](#).

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see [Xilinx Support](#).

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help**→**Documentation and Tutorials**.
- On Windows, select **Start**→**All Programs**→**Xilinx Design Tools**→**DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the [Design Hubs](#) page.

Note: For more information on DocNav, see the [Documentation Navigator](#) page on the Xilinx website.

References

These documents provide supplemental material useful with this guide:

1. Varium C1100 Compute Adaptor Installation Guide (UG1525)
 2. Varium C1100 Compute Adaptor Data Sheet (DS1003)
 3. UltraScale Architecture Configuration User Guide ([UG570](#))
 4. Alveo Programming Cable User Guide ([UG1377](#))
 5. Vivado Design Suite User Guide: Programming and Debugging ([UG908](#))
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