1. Question 1: After building the project in Quartus, there should be a Compilation Report that shows a “Flow Summary” window with information about the resulting circuit. How many “Total logic elements” did the SOP design use?
    a. The “Total logic elements” category shows “8 / 49,760 (<1%)”, so I can only imagine that 8 logic elements were used.

2. How many “Total logic elements” did the POS design use?
    a. The “Total logic elements” category gave the exact same result as in the SOP test.

3. Based on the answers to Questions 1 and 2, what can you conclude about the need to minimize equations before calling the VHDL tool chain?
    a. I can conclude that although the equations were longer in the POS test, it did not require more logic elements, meaning that it is not entirely important to minimize the equations. (Aside from the fact that shorter logic is more readable)

4. Write all 7 outputs from Table 1 in min-term notation (a.k.a. sigma notation).
    a. $\Sigma_{S3,S2,S1,S0}(0, 2, 3, 5, 6, 7, 8, 9, 10, 12, 14, 15)$
    b. $\Sigma_{S3,S2,S1,S0}(0, 1, 2, 3, 4, 7, 8, 9, 10, 13)$
    c. $\Sigma_{S3,S2,S1,S0}(0, 1, 3, 4, 5, 6, 7, 8, 9, 10, 11, 13)$
    d. $\Sigma_{S3,S2,S1,S0}(0, 2, 3, 5, 6, 8, 9, 11, 12, 13, 14)$
    e. $\Sigma_{S3,S2,S1,S0}(0, 2, 6, 8, 10, 11, 12, 13, 14, 15)$
    f. $\Sigma_{S3,S2,S1,S0}(0, 4, 5, 6, 8, 9, 10, 11, 12, 14, 15)$
    g. $\Sigma_{S3,S2,S1,S0}(2, 3, 4, 5, 6, 8, 9, 10, 11, 13, 14, 15)$

5. Write all 7 outputs from Table 1 in max-term notation (a.k.a. pi notation).
    a. $\Pi_{S3,S2,S1,S0}(1, 4, 11, 13)$
    b. $\Pi_{S3,S2,S1,S0}(5, 6, 11, 12, 14, 15)$
    c. $\Pi_{S3,S2,S1,S0}(2, 12, 14, 15)$
    d. $\Pi_{S3,S2,S1,S0}(1, 4, 7, 10, 15)$
    e. $\Pi_{S3,S2,S1,S0}(1, 3, 4, 5, 7, 9)$
    f. $\Pi_{S3,S2,S1,S0}(1, 2, 3, 7, 13)$
    g. $\Pi_{S3,S2,S1,S0}(0, 1, 7, 12)$