Introduction to AMBA AXI

2014 – 2017 - 2018

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Agenda

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- Read data signals
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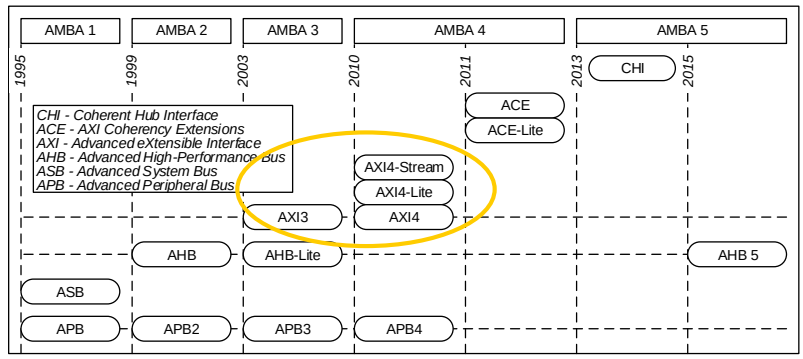
Evolution of AMBA Standards



- CHI - Coherent Hub Interface - The highest performance, used in networks and servers
- ACE - AXI Coherency Extensions - Used in big.LITTLE™ systems for smartphones, tablets, etc.
- AXI - Advanced eXtensible Interface - The most widespread AMBA interface. Connectivity up to 100's of Masters and Slaves in complex SoC's
- AHB - Advanced High-Performance Bus - The main system bus in microcontroller usage
- APB - Advanced Peripheral Bus - Minimal gate count for peripherals
- ATB - Advanced Trace Bus - For moving trace data around the chip

refer to “Ashley Stevens, Introduction to AMBA® 4 ACE™ and big.LITTLE™ Processing Technology, July 2013.”

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AMBA buses

AMBA 4 AXI	AMBA 3 AXI	AMBA 2 AHB
an extension of AMBA 3 AXI Burst length up to 256 beats Quality-of-service Removal of lock transaction Removal of write interleaving	channel architecture registers slices one address for burst up to 16 beats multiple outstanding bursts out of order completion data interleaving low-power interface	burst transfers pipelined operation split transactions single-cycle bus master handover single-clock edge operation multiple bus masters (up to 16) two uni-directional 32-bit data bus for read and write
AMBA 4 APB	**AMBA 3 APB**	**AMBA 2 APB**
an extension of AMBA 3 APB transaction protection (normal-privileged, secure-nonsecure, data-instruction) Sparse data transfer (partial access)	an extension of AMBA 2 APB wait state supported error response supported	low power latched address and control simple interface suitable for many peripherals

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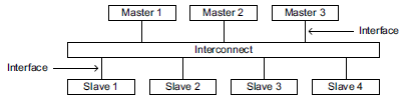
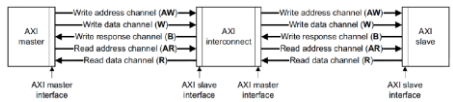
AXI terminologies

- Channel
  - Independent collection of AXI signals associated to a VALID signal
- Interface
  - Collection of one or more channels that expose an IP core's function, connecting a master to a slave (Each IP core may have multiple interfaces.)
- Bus
  - Multiple-bit signal (not an interface or channel)





- Transfer
  - A single exchange of information. That is, with one xVALID/xREADY handshake
- Transaction
  - An entire burst of transfers, comprising an address, one or more data transfers and a response transfer (writes only).
    - A write "transaction" including an AW "transfer", one or more W "transfers" and finally a B "transfer".
    - A read "transaction" starts with an AR "transfer" and is followed by one or more "R" transfers".
- Burst
  - Transaction that consists of more than one data transfers.

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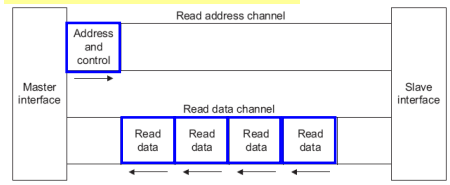
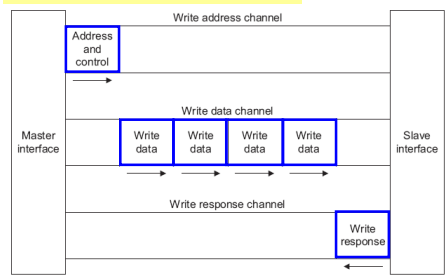
AXI architecture

- AXI protocol
  - Channel-based protocol
    - 5 independent channels
    - 32-bit addr/data: 184~204 wires
  - Single-clock edge operation: ACLK
  - Two-way flow-control mechanism for each channel
    - Valid/ready handshake mechanism
  - Separate address/control and data phases
  - Burst-based protocol
  - One address for burst
  - Variable-length burst
    - 1 to 16 data transfers per burst
  - Multiple outstanding bursts
  - Out-of-order transaction completion
  - Data interleaving

Channel architecture for read



Channel architecture for write



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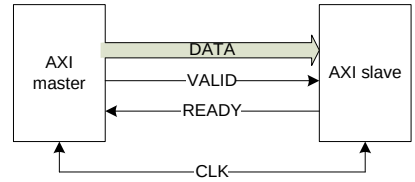
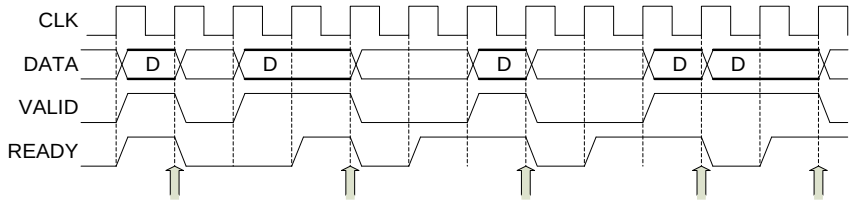
VALID/READY handshake mechanism (1/2)

- Basic AXI handshaking
  - Master asserts and holds 'VALID' when data is available
  - Slave asserts 'READY' if able to accept data
  - 'DATA' and other signals transferrred when 'VALID' and 'READY' are 1.





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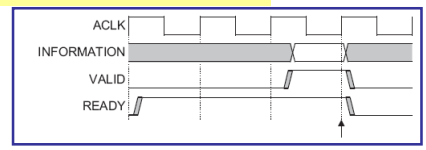
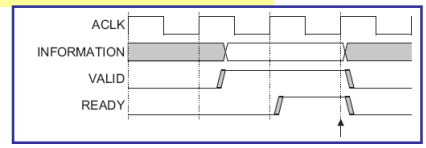
VALID/READY handshake mechanism (2/2)

- Protocol (basic AXI handshaking)
  - The transmitter asserts VALID on any clock cycle when it has data and de-asserts when it does not.
  - The receiver asserts READY on any cycle when it is ready for data and de-asserts when it is not.
  - In any clock cycle in which VALID and READY are both asserted, data "moves", meaning it is taken by the receiver.
  - 'Ready before Valid' handshake is better than others in terms of data transfer latency.
    - 'Valid before Ready' handshake requires at lease two cycles.
  - Deadlock avoidance scheme is required.
- Two-way flow-control
  - Both mater and slave can control the rate of information movement.
- Dual-ready handshake: two-way VALID/READY handshake
  - A LAST signal to indicate when the transfer of the final data item within a transaction takes place

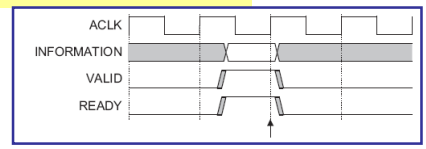
READY before VALID handshake



VALID before READY handshake



VALID with READY handshake



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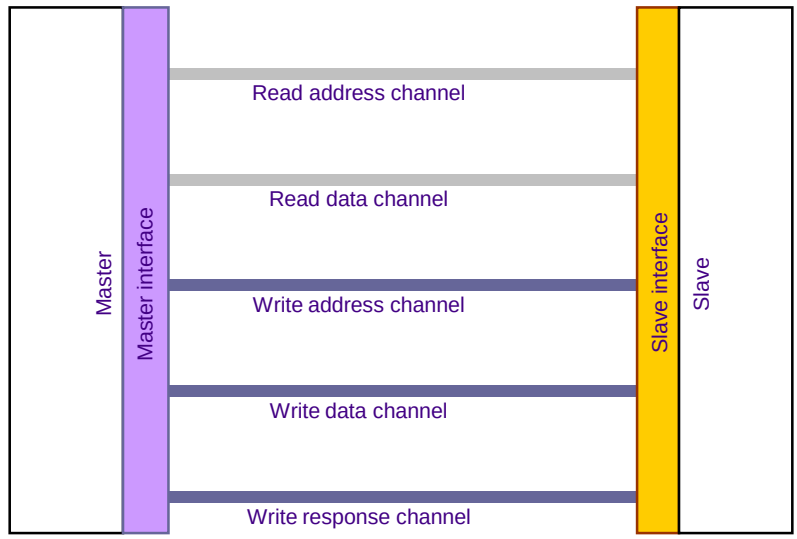
Channel-based burst protocol of AXI



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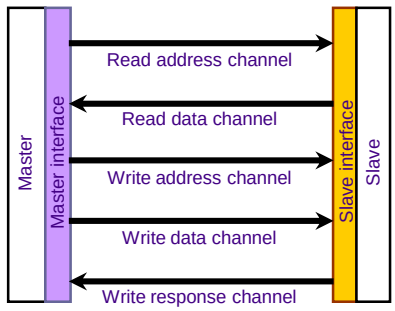
Five independent channels

- Each channel uses two-way valid/ready handshake mechanism.
- Each channel transfers information in only one direction.



- 1. Read address channel
  - Carrying address and control information from master to slave
  - 'AR' prefix
- 2. Read data channel
  - Conveying read data and read response information from slave to master
  - 'R' prefix
- 3. Write address channel
  - Carrying address and control information from master to slave
  - 'AW' prefix
- 4. Write data channel
  - Conveying write data from master to slave
  - Treated as buffered
  - 'W' prefix
- 5. Write response channel
  - Providing write response from slave to master
  - 'B' prefix

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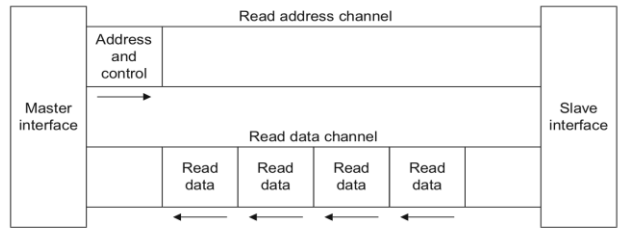
AMBA AXI Read Channels



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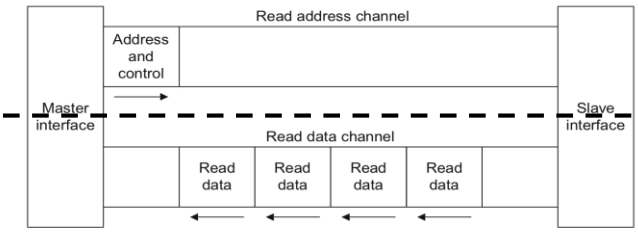
AMBA AXI Read Channels

Independent



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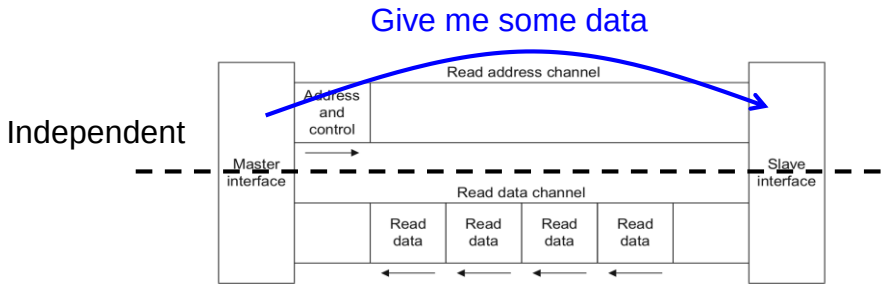
AMBA AXI Read Channels



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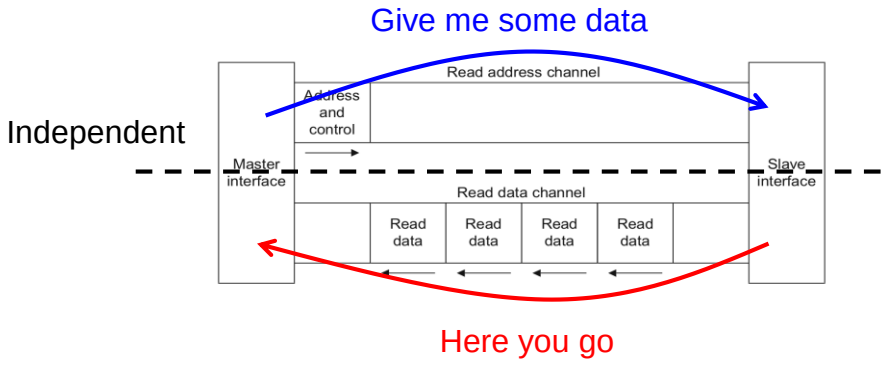
AMBA AXI Read Channels



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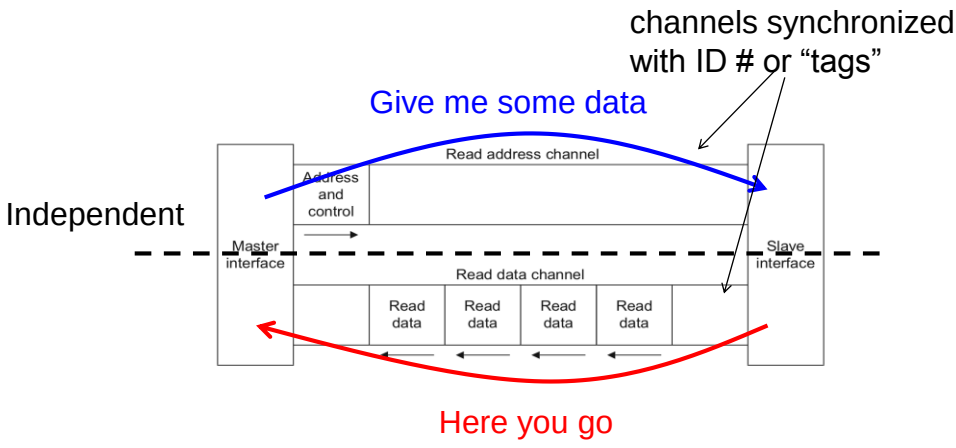
AMBA AXI Read Channels



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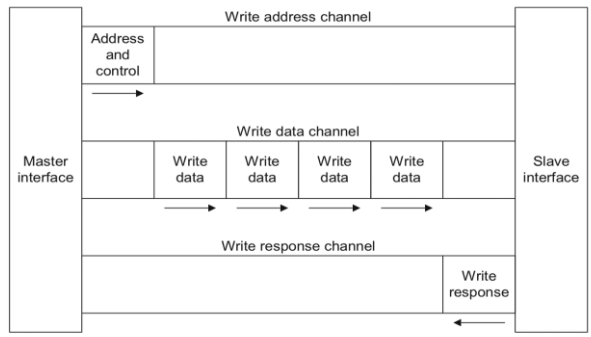
AMBA AXI Write Channels



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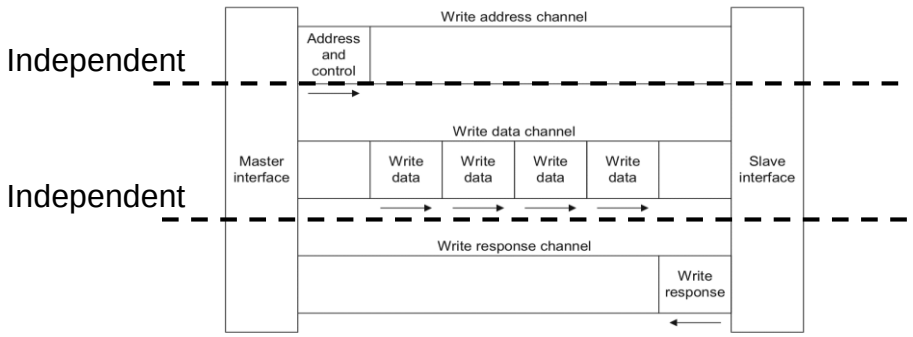
AMBA AXI Write Channels



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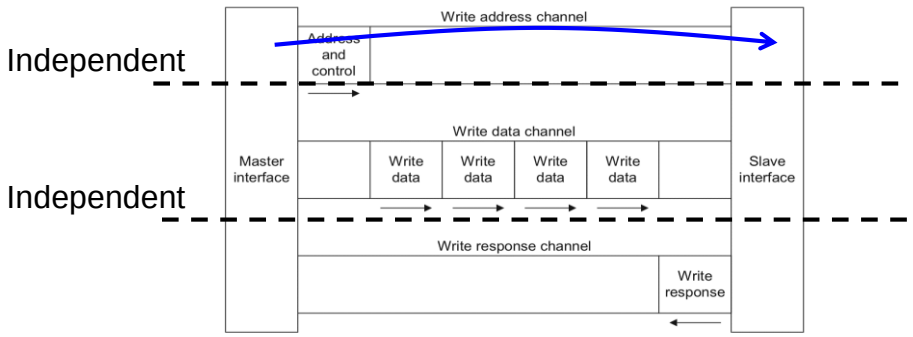
AMBA AXI Write Channels

I'm sending data. Please store it.



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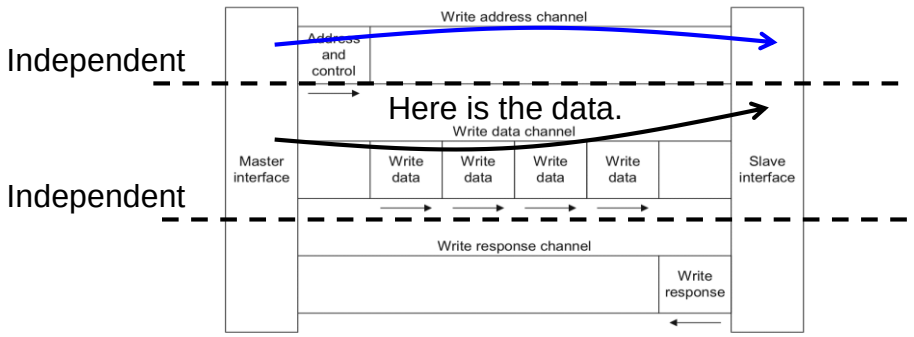
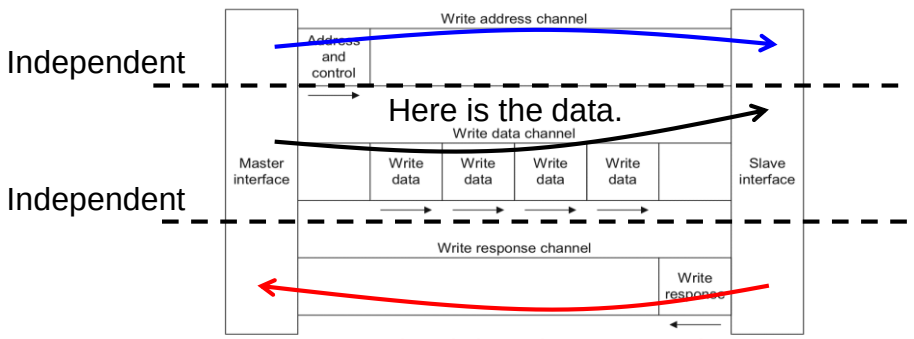
AMBA AXI Write Channels

I'm sending data. Please store it.



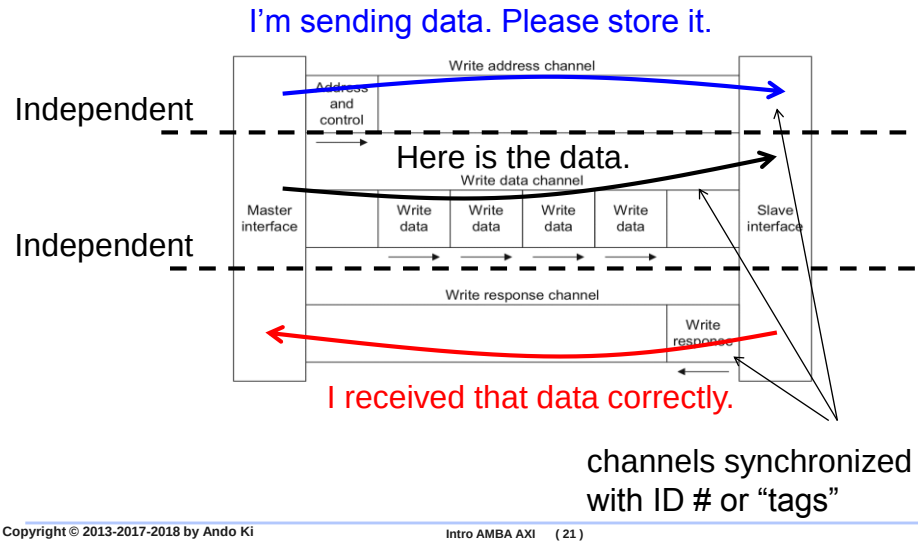
AMBA AXI Write Channels

I'm sending data. Please store it.



I received that data correctly.

AMBA AXI Write Channels



channels synchronized with ID # or "tags"

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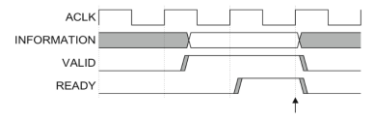
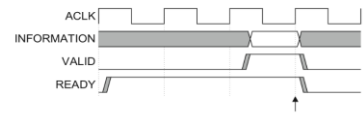
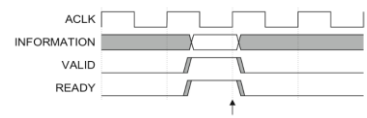
AMBA AXI Flow-Control

- Information moves only when:
  - Source is **Valid**, and
  - Destination is **Ready**
- On each channel the master or slav can limit the flow
- Very flexible







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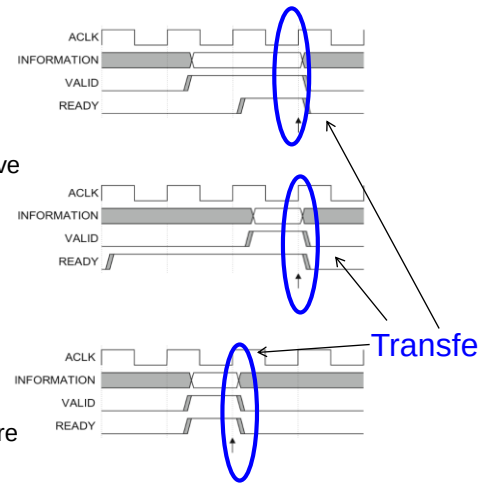
AMBA AXI Flow-Control

- Information moves only when:
  - Source is **Valid**, and
  - Destination is **Ready**
- On each channel the master or slave can limit the flow
- Very flexible
- There is a potential problem: **DEADLOCK**
- On a write transaction the master **must not wait** for AWREADY before asserting WVALID



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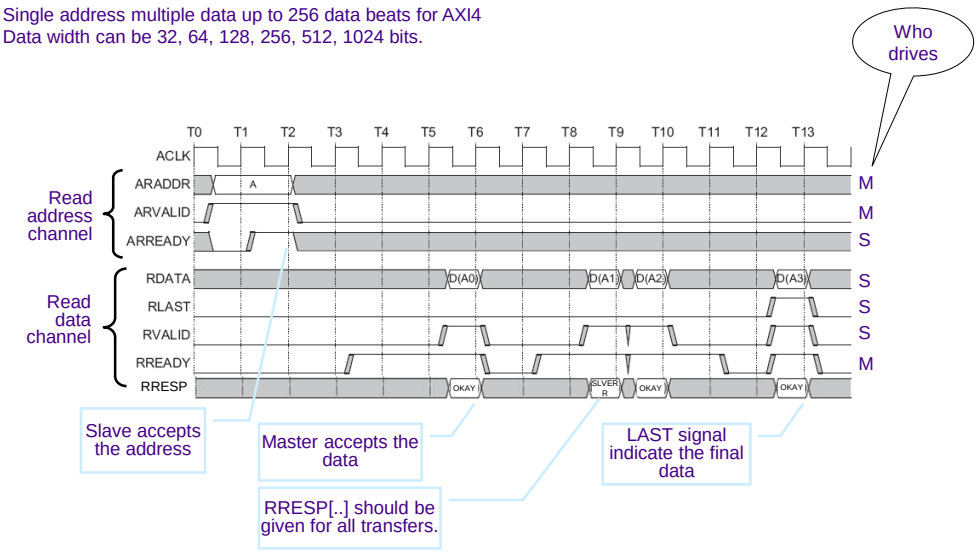
Read burst example

Single address multiple data up to 256 data beats for AXI4
Data width can be 32, 64, 128, 256, 512, 1024 bits.



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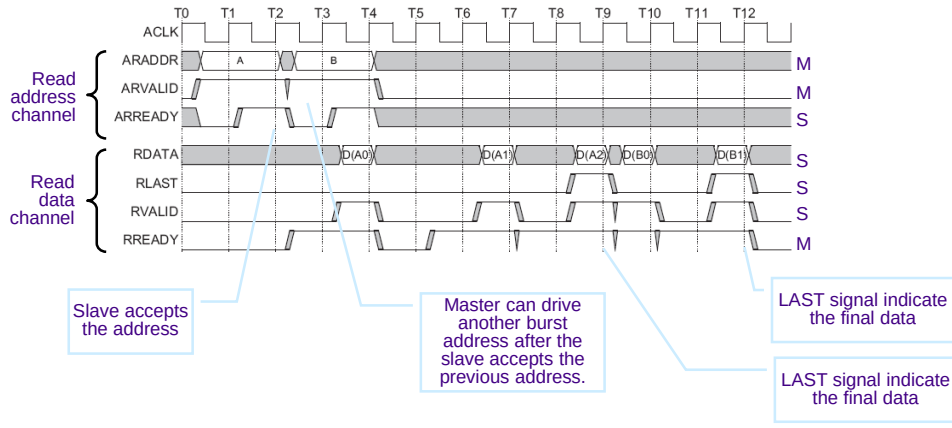
Read burst overlapping example



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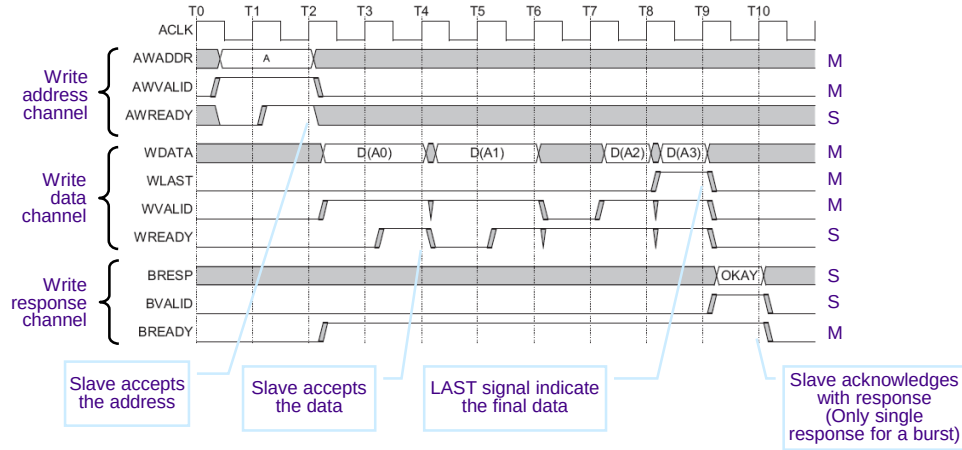
Write burst example



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Signals

Group	Prefix	Remarks
Global	**A**	ACLK, ARESETn
Write address channel	**AW**	AWID[], AWADDR[], AWLEN[], AWSIZE[], AWBURST[], AWLOCK[], AWCACHE[], AWPROT[], AWVALID, AWREADY
Write data channel	**W**	WID[], WDATA[], WSTRB[], WLAST, WVALID, WREADY
Write response channel	**B**	BID[], BRESP[], BVALID, BREADY
Read address channel	**AR**	ARID[], ARADDR[], AWLEN[], ARSIZE[], ARBURST[], ARLOCK[], ARCACHE[], ARPROT[], ARVALID, ARREADY
Read data channel	**R**	RID[], RDATA[], RSTRB[], RLAST, RVALID, RREADY
Low-power interface	**C**	CSYSREQ, CSYSACK, CACTIVE

Bus width and transaction ID width are implementation-specific. Normally, 32-bit data bus, 4-bit write data strobe, and 4-bit ID are used.

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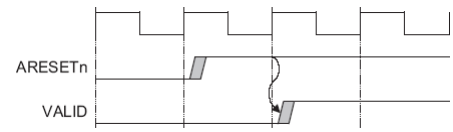
Global signals

Signal	Source	Description
ACLK	Clock source	Global clock signal. All signals are sampled on the rising edge of the global clock.
ARESETn	Reset source	Global reset signal. This signal is active LOW.



- Each AXI component uses a single clock signal: ACLK.
- All input signals are sampled on the rising edge of ACLK.
- All output signal changes must occur after the rising edge of ACLK.
- No combinational path between input and output is allowed.
- The reset signal, ARESETn, can be asserted asynchronously.
- The reset signal, ARESETn, must be de-asserted after the rising edge of ACLK.
- During ARESETn is low
  - All valid signals must be low: ARVALID, AWVALID, WVALID, RVALID, BVALID.
- All valid can be driven high only a rising ACLK edge after ARESETn is high.

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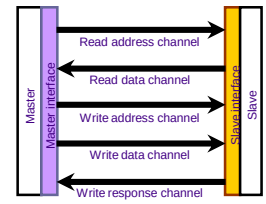
Write address signals

Signal	Source	Description
AWID[3:0]	Master	Write address ID. This signal is the identification tag for the write address group of signals.
AWADDR[31:0]	Master	Write address. The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst.
AWLEN[3:0]	Master	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address. See Table 4-1 on page 4-3.
AWSIZE[2:0]	Master	Burst size. This signal indicates the size of each transfer in the burst. Byte lane strobes indicate exactly which byte lanes to update. See Table 4-2 on page 4-4.
AWBURST[1:0]	Master	Burst type. The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated. See Table 4-3 on page 4-5.
AWLOCK[1:0]	Master	Lock type. This signal provides additional information about the atomic characteristics of the transfer. See Table 6-1 on page 6-2.
AWCACHE[3:0]	Master	Cache type. This signal indicates the bufferable, cacheable, write-through, write-back, and allocate attributes of the transaction. See Table 5-1 on page 5-3.
AWPROT[2:0]	Master	Protection type. This signal indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access. See *Protection unit support* on page 5-5.
AWVALID	Master	Write address valid. This signal indicates that valid write address and control information are available: 1 = address and control information available 0 = address and control information not available. The address and control information remain stable until the address acknowledge signal, **AWREADY**, goes HIGH.
AWREADY	Slave	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals: 1 = slave ready 0 = slave not ready.

0 means 1 beat

AxLEN[7:0] for AXI4 (up to 256 beats)

AxLOCK[1] is not used for AXI4



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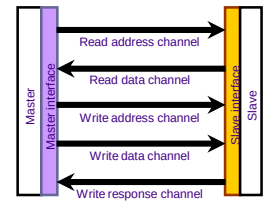
Write address signals (AXI4)

Signal	Source	Description
AWID	Master	Write address ID. This signal is the identification tag for the write address group of signals. See *Transaction ID* on page A5-79.
AWADDR	Master	Write address. The write address gives the address of the first transfer in a write burst transaction. See *Address structure* on page A3-46.
AWLEN	Master	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address. This changes between AXI3 and AXI4. See *Burst length* on page A3-46.
AWSIZE	Master	Burst size. This signal indicates the size of each transfer in the burst. See *Burst size* on page A3-47.
AWBURST	Master	Burst type. The burst type and the size information, determine how the address for each transfer within the burst is calculated. See *Burst type* on page A3-47.
AWLOCK	Master	Lock type. Provides additional information about the atomic characteristics of the transfer. This changes between AXI3 and AXI4. See *Locked accesses* on page A7-99.
AWCACHE	Master	Memory type. This signal indicates how transactions are required to progress through a system. See *Memory types* on page A4-67.
AWPROT	Master	Protection type. This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or an instruction access. See *Access permissions* on page A4-73.
AWQOS	Master	*Quality of Service*, QoS. The QoS identifier sent for each write transaction. Implemented only in AXI4. See *QoS signaling* on page A8-102.
AWREGION	Master	Region identifier. Permits a single physical interface on a slave to be used for multiple logical interfaces. Implemented only in AXI4. See *Multiple region signaling* on page A8-103.
AWUSER	Master	User signal. Optional User-defined signal in the write address channel. Supported only in AXI4. See *User-defined signaling* on page A8-104.
AWVALID	Master	Write address valid. This signal indicates that the channel is signaling valid write address and control information. See *Channel handshake signals* on page A3-40.
AWREADY	Slave	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals. See *Channel handshake signals* on page A3-40.

0 means 1 beat

AxLEN[7:0] for AXI4 (up to 256 beats)

AxLOCK[1] is not used for AXI4



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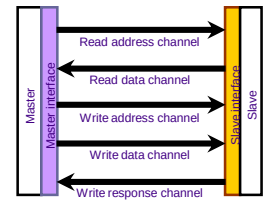
Write data signals (AXI3, AXI4)

Signal	Source	Description
WID[3:0]	Master	Write ID tag. This signal is the ID tag of the write data transfer. The **WID** value must match the **AWID** value of the write transaction.
WDATA[31:0]	Master	Write data. The write data bus can be 8, 16, 32, 64, 128, 256, 512, or 1024 bits wide.
WSTRB[3:0]	Master	Write strobes. This signal indicates which byte lanes to update in memory. There is one write strobe for each eight bits of the write data bus. Therefore, **WSTRB[n]** corresponds to **WDATA[(8 × n) + 7:(8 × n)]**.
WLAST	Master	Write last. This signal indicates the last transfer in a write burst.
WVALID	Master	Write valid. This signal indicates that valid write data and strobes are available: 1 = write data and strobes available 0 = write data and strobes not available.
WREADY	Slave	Write ready. This signal indicates that the slave can accept the write data: 1 = slave ready 0 = slave not ready.

Unique for write data channel

Signal	Source	Description
WID	Master	Write ID tag. This signal is the ID tag of the write data transfer. Supported only in AXI3. See *Transaction ID* on page A5-79.
WDATA	Master	Write data.
WSTRB	Master	Write strobes. This signal indicates which byte lanes hold valid data. There is one write strobe bit for each eight bits of the write data bus. See *Write strobes* on page A3-52.
WLAST	Master	Write last. This signal indicates the last transfer in a write burst. See *Write data channel* on page A3-41.
WUSER	Master	User signal. Optional User-defined signal in the write data channel. Supported only in AXI4. See *User-defined signaling* on page A8-104.
WVALID	Master	Write valid. This signal indicates that valid write data and strobes are available. See *Channel handshake signals* on page A3-40.
WREADY	Slave	Write ready. This signal indicates that the slave can accept the write data. See *Channel handshake signals* on page A3-40.



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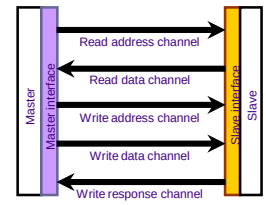
Write response signals

Signal	Source	Description
BID[3:0]	Slave	Response ID. The identification tag of the write response. The **BID** value must match the **AWID** value of the write transaction to which the slave is responding.
BRESP[1:0]	Slave	Write response. This signal indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
BVALID	Slave	Write response valid. This signal indicates that a valid write response is available: 1 = write response available 0 = write response not available.
BREADY	Master	Response ready. This signal indicates that the master can accept the response information. 1 = master ready 0 = master not ready.

Signal	Source	Description
BID	Slave	Response ID tag. This signal is the ID tag of the write response. See *Transaction ID* on page A5-79.
BRESP	Slave	Write response. This signal indicates the status of the write transaction. See *Read and write response structure* on page A3-57.
BUSER	Slave	User signal. Optional User-defined signal in the write response channel. Supported only in AXI4. See *User-defined signaling* on page A8-104.
BVALID	Slave	Write response valid. This signal indicates that the channel is signaling a valid write response. See *Channel handshake signals* on page A3-40.
BREADY	Master	Response ready. This signal indicates that the master can accept a write response. See *Channel handshake signals* on page A3-40.

- **OKAY** (2'b00) Normal access success. Indicates that a normal access has been successful. Can also indicate an exclusive access has failed.
- **EXOKAY** (2'b01) Exclusive access okay. Indicates that either the read or write portion of an exclusive access has been successful.
- **SLVERR** (2'b10) Slave error. Used when the access has reached the slave successfully, but the slave wishes to return an error condition to the originating master.
- **DECERR** (2'b11) Decode error. Generated, typically by an interconnect component, to indicate that there is no slave at the transaction address.



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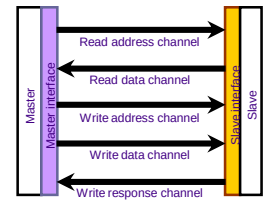
Read address signals

Signal	Source	Description
ARID[3:0]	Master	Read address ID. This signal is the identification tag for the read address group of signals.
ARADDR[31:0]	Master	Read address. The read address bus gives the initial address of a read burst transaction. Only the start address of the burst is provided and the control signals that are issued alongside the address detail how the address is calculated for the remaining transfers in the burst.
ARLEN[3:0]	Master	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address. See Table 4-1 on page 4-3.
ARSIZE[2:0]	Master	Burst size. This signal indicates the size of each transfer in the burst. See Table 4-2 on page 4-4.
ARBURST[1:0]	Master	Burst type. The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated. See Table 4-3 on page 4-5.
ARLOCK[1:0]	Master	Lock type. This signal provides additional information about the atomic characteristics of the transfer. See Table 6-1 on page 6-2.
ARCACHE[3:0]	Master	Cache type. This signal provides additional information about the cacheable characteristics of the transfer. See Table 5-1 on page 5-3.
ARPROT[2:0]	Master	Protection type. This signal provides protection unit information for the transaction. See *Protection unit support* on page 5-5.
ARVALID	Master	Read address valid. This signal indicates, when HIGH, that the read address and control information is valid and will remain stable until the address acknowledge signal, **ARREADY**, is high. 1 = address and control information valid 0 = address and control information not valid.
ARREADY	Slave	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals: 1 = slave ready 0 = slave not ready.

0 means 1 beat

AxLEN[7:0] for AXI4 (up to 256 beats)

AxLOCK[1] is not used for AXI4



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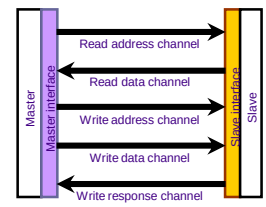
Read address signals (AXI4)

Signal	Source	Description
ARID	Master	Read address ID. This signal is the identification tag for the read address group of signals. See *Transaction ID* on page A5-79.
ARADDR	Master	Read address. The read address gives the address of the first transfer in a read burst transaction. See *Address structure* on page A3-46.
ARLEN	Master	Burst length. This signal indicates the exact number of transfers in a burst. This changes between AXI3 and AXI4. See *Burst length* on page A3-46.
ARSIZE	Master	Burst size. This signal indicates the size of each transfer in the burst. See *Burst size* on page A3-47.
ARBURST	Master	Burst type. The burst type and the size information determine how the address for each transfer within the burst is calculated. See *Burst type* on page A3-47.
ARLOCK	Master	Lock type. This signal provides additional information about the atomic characteristics of the transfer. This changes between AXI3 and AXI4. See *Locked accesses* on page A7-99.
ARCACHE	Master	Memory type. This signal indicates how transactions are required to progress through a system. See *Memory types* on page A4-67.
ARPROT	Master	Protection type. This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or an instruction access. See *Access permissions* on page A4-73.
ARQOS	Master	*Quality of Service*, QoS. QoS identifier sent for each read transaction. Implemented only in AXI4. See *QoS signaling* on page A8-102.
ARREGION	Master	Region identifier. Permits a single physical interface on a slave to be used for multiple logical interfaces. Implemented only in AXI4. See *Multiple region signaling* on page A8-103.
ARUSER	Master	User signal. Optional User-defined signal in the read address channel. Supported only in AXI4. See *User-defined signaling* on page A8-104.
ARVALID	Master	Read address valid. This signal indicates that the channel is signaling valid read address and control information. See *Channel handshake signals* on page A3-40.
ARREADY	Slave	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals. See *Channel handshake signals* on page A3-40.

0 means 1 beat

AxLEN[7:0] for AXI4 (up to 256 beats)

AxLOCK[1] is not used for AXI4



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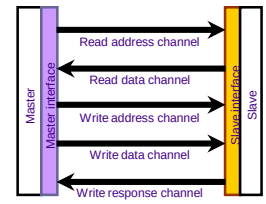
Read data signals

Signal	Source	Description
RID[3:0]	Slave	Read ID tag. This signal is the ID tag of the read data group of signals. The **RID** value is generated by the slave and must match the **ARID** value of the read transaction to which it is responding.
RDATA[31:0]	Slave	Read data. The read data bus can be 8, 16, 32, 64, 128, 256, 512, or 1024 bits wide.
RRESP[1:0]	Slave	Read response. This signal indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
RLAST	Slave	Read last. This signal indicates the last transfer in a read burst.
RVALID	Slave	Read valid. This signal indicates that the required read data is available and the read transfer can complete: 1 = read data available 0 = read data not available.
RREADY	Master	Read ready. This signal indicates that the master can accept the read data and response information: 1= master ready 0 = master not ready.

Signal	Source	Description
RID	Slave	Read ID tag. This signal is the identification tag for the read data group of signals generated by the slave. See *Transaction ID* on page A5-79.
RDATA	Slave	Read data.
RRESP	Slave	Read response. This signal indicates the status of the read transfer. See *Read and write response structure* on page A3-57.
RLAST	Slave	Read last. This signal indicates the last transfer in a read burst. See *Read data channel* on page A3-41.
RUSER	Slave	User signal. Optional User-defined signal in the read data channel. Supported only in AXI4. See *User-defined signaling* on page A8-104.
RVALID	Slave	Read valid. This signal indicates that the channel is signaling the required read data. See *Channel handshake signals* on page A3-40.
RREADY	Master	Read ready. This signal indicates that the master can accept the read data and response information. See *Channel handshake signals* on page A3-40.

- **OKAY** (2'b00) Normal access success. Indicates that a normal access has been successful. Can also indicate an exclusive access has failed.
- **EXOKAY** (2'b01) Exclusive access okay. Indicates that either the read or write portion of an exclusive access has been successful.
- **SLVERR** (2'b10) Slave error. Used when the access has reached the slave successfully, but the slave wishes to return an error condition to the originating master.
- **DECERR** (2'b11) Decode error. Generated, typically by an interconnect component, to indicate that there is no slave at the transaction address.



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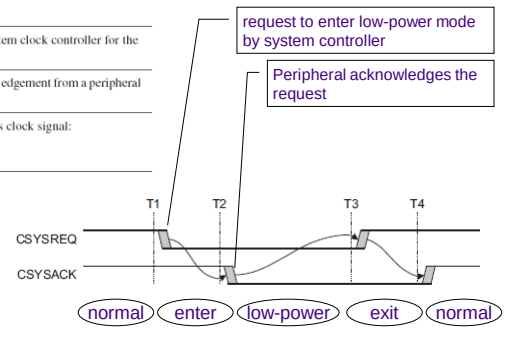
Low power interface signals

Signal	Source	Description
CSYSREQ	Clock controller	System low-power request. This signal is a request from the system clock controller for the peripheral to enter a low-power state.
CSYSACK	Peripheral device	Low-power request acknowledgement. This signal is the acknowledgement from a peripheral of a system low-power request.
CACTIVE	Peripheral device	Clock active. This signal indicates that the peripheral requires its clock signal: 1 = peripheral clock required 0 = peripheral clock not required.

- The primary signal in the clock control interface is **CACTIVE**. The peripheral uses this signal to indicate when it requires its clock to be enabled. The peripheral asserts **CACTIVE** to indicate that it requires the clock, and the system clock controller must enable the clock immediately. The peripheral deasserts **CACTIVE** to indicate that it does not require the clock. The system clock controller can then determine whether to enable or disable the peripheral clock.
- A peripheral that can have its clock enabled or disabled at any time can drive **CACTIVE** LOW permanently.
- A peripheral that must have its clock always enabled must drive **CACTIVE** HIGH permanently.



- For normal clocked operation, both **CSYSREQ** and **CSYSACK** are HIGH
- For requesting to put the peripheral in a low-power state, the system clock controller de-asserts **CSYSREQ.**
  - The peripheral acknowledges the request by de-asserting **CSYSACK**.
- To exit from the low-power state, the system clock controller asserts **CSYSREQ.**
  - The peripheral asserts **CSYSACK** to acknowledge the exit.

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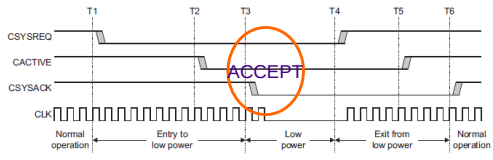
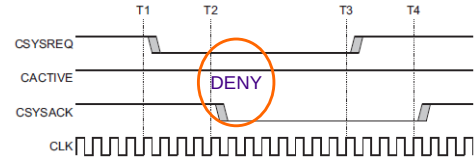
Low power accept and deny

- The peripheral can accept or deny the request for a low-power state from the system clock controller. The level of the **CACTIVE** signal when the peripheral acknowledges the request by de-asserting **CSYSACK** indicates the acceptance or denial of the request.

Acceptance of a low-power request



Denial of a low-power request



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QoS signals (AXI4)

- AXI4 interface functionality is extended to support two 4-bit QoS identifiers:
  - **AWQOS[3:0]** 4-bit QoS identifier sent on the write address channel for each write tr ansaction
  - **ARQOS[3:0]** 4-bit QoS identifier sent on the read address channel for each read tra nsaction.
- The exact use of the QoS identifier is not specified by the protocol. The preferre d use of the **AWQOS** and **ARQOS** identifiers is as a priority indicator for the as sociated write or read transaction. A higher value will indicate a higher priority tr ansaction.
  - A default value of 4'b0000 indicates that the interface is not actively participating in t he QoS scheme.

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Agenda

- AMBA AXI4-Lite

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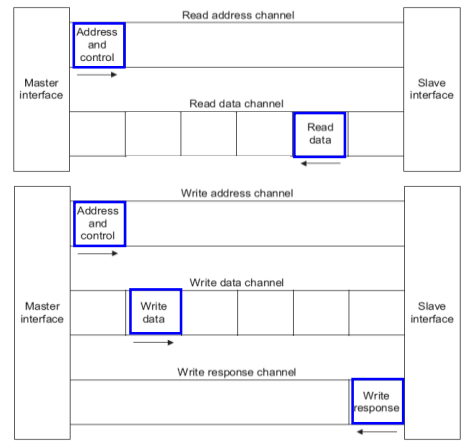
AMBA AXI4-Lite

- AXI-Lite key feature
  - burst length 1 only
  - no partial data access, i.e. all data access are the same size as the width of data bus
  - 32-bit (or 64-bit) data bus only
  - all accesses are 'device non-bufferable'
  - exclusive access not supported
  - no AXI ID, all transactions must be in order → all access use a single fixed ID value.



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AMBA AXI4-Lite

- AXI-Lite not required signals
  - EXOKAY or RRESP/BRESP
  - AxLEN: burst length 1 → stuck to 0
  - AxSIZE: no partial → width of the data bus
  - AxBURST: burst length 1 → stuck to 1
  - AxLOCK: all normal access → stuck to 0
  - AxCACHE: non-modifiable, non-bufferable → stuck to 0
  - xLAST: burst length 1 → stuck to 1

- Required signals

Global	Write address channel	Write data channel	Write response channel	Read address channel	Read data channel
ACLK	AWVALID	WVALID	BVALID	ARVALID	RVALID
ARESETn	AWREADY	WREADY	BREADY	ARREADY	RREADY
–	AWADDR	WDATA	BRESP	ARADDR	RDATA
–	AWPROT	WSTRB	–	ARPROT	RRESP

- Interoperability

Master	Slave	Interoperability
AXI	AXI	Fully operational.
AXI	AXI4-Lite	AXI ID reflection is required. Conversion might be required.
AXI4-Lite	AXI	Fully operational.
AXI4-Lite	AXI4-Lite	Fully operational.

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References

- AMBA® AXI Protocol v1.0 Specification, IHI 0022B, ARM Limited, 2004.
- AMBA® AXI Protocol Version: 2.0 Specification, IHI 0022C (ID030510), ARM Limited, 2010.
- AMBA® AXI and ACE Protocol Specification, IHI 0022D (ID102711), ARM Limited, 2011. (AXI3, AXI3, and AXI4-Lite, ACE and ACE-Lite)
- AMBA® 4 AXI4-Stream Protocol Version: 1.0 Specification, IHI 0051A (ID030510), ARM Limited, 2010.

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