Integrated Logic Analyzer (ILA) with GPIO with AMBA APB interface

2020

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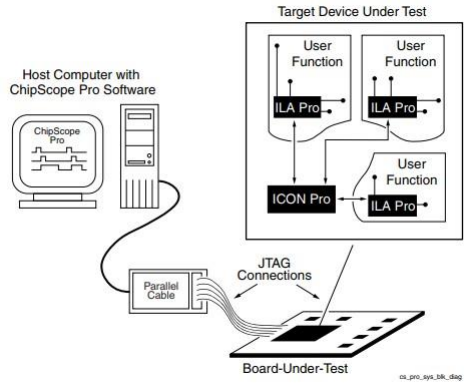
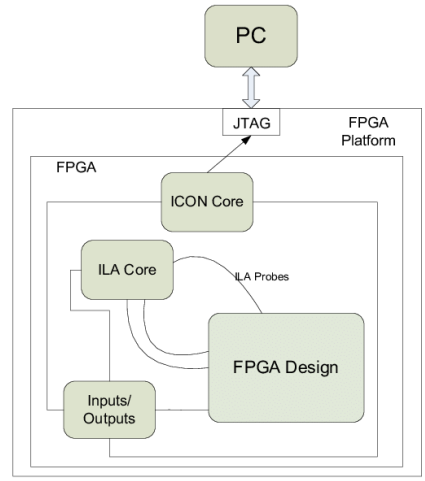
Integrated Logic Analyzer (ILA)

- ChipScope for ISE
- ILA for Vivado



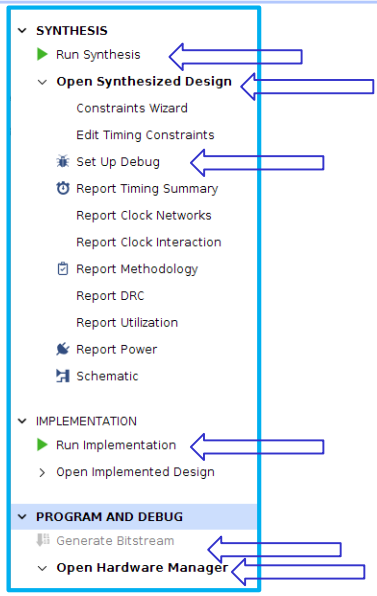


To specify nets to monitor in the source code

- prepend following pragma at the line of code.
  - (* mark_debug="true" *)

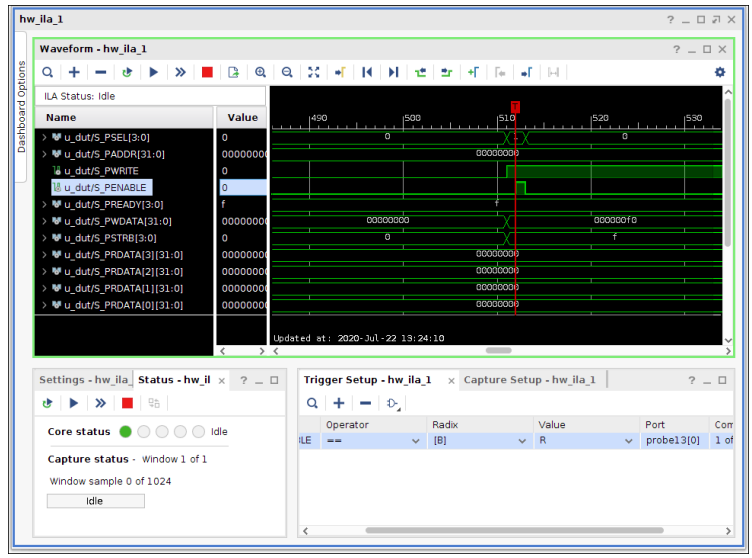
```
(* mark_debug="true" *) wire [31:0]              S_PADDR;
(* mark_debug="true" *) wire                     S_PENABLE;
(* mark_debug="true" *) wire                     S_PWRITE;
(* mark_debug="true" *) wire [31:0]              S_PWDATA;
(* mark_debug="true" *) wire [NUM_PSLAVE-1:0]    S_PSEL;
(* mark_debug="true" *) wire [31:0]              S_PRDATA[0:NUM_PSLAVE-1];
                        `ifdef AMBA_APB3
(* mark_debug="true" *) wire [NUM_PSLAVE-1:0]    S_PREADY;
(* mark_debug="true" *) wire [NUM_PSLAVE-1:0]    S_PSLVERR;
                        `endif
                        `ifdef AMBA_APB4
(* mark_debug="true" *) wire [ 3:0]              S_PSTRB;
(* mark_debug="true" *) wire [ 2:0]              S_PPROT;
                        `endif
(* mark_debug="true" *) wire [31:0]              S0_PRDATA=S_PRDATA[0];
(* mark_debug="true" *) wire [31:0]              S1_PRDATA=S_PRDATA[1];
(* mark_debug="true" *) wire [31:0]              S2_PRDATA=S_PRDATA[2];
(* mark_debug="true" *) wire [31:0]              S3_PRDATA=S_PRDATA[3];
```


Overall steps



1. '1. 'Run synthesis'
   - Takes time
2. 2. Expand 'Open Synthesized Design' menu
3. 3. 'Set up Debug'
   - Pics all nets to monitor
4. 4. 'Run Implementation'
   - Takes time even more
5. 5. 'Generate Bitstream'
6. 6. 'Open Hardware Manager'
7. 7. 'Open Target'
8. 8. 'Program device'
   - 'project_1/project_1.runs/impl_1/fpga.bit'
   - 'project_1/project_1.runs/impl_1/fpga.ltx'

Example screen shot



For GPIO APB

- go to ‘ex_gpio_apb_fpga/pnr’
- run ‘make’ with ‘ILA=1’ macro
  - $ make ILA=1
- do follow the overall steps

- 1. ‘Run synthesis’
  - Takes time
- 2. Expand ‘Open Synthesized Design’ menu
- 3. ‘Set up Debug’
  - Pics all nets to monitor
- 4. ‘Run Implementation’
  - Takes time even more
- 5. ‘Generate Bitstream’
- 6. ‘Open Hardware Manager’
- 7. ‘Open Target’
- 8. ‘Program device’
  - ‘project_1/project_1.runs/impl_1/fpga.bit’
  - ‘project_1/project_1.runs/impl_1/fpga.ltx’