Engineering Program on RTL Design for FPGA Accelerator

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Goals and objectives

- Understanding of RTL design flow
- Acquiring the working knowledge of RTL design
- Practicing development of RTL design using FPGA
- Understanding of Verilog HDL
- Understanding of FPGA
- Understanding of FPGA development environment
- Understanding of what can and cannot using FPGA

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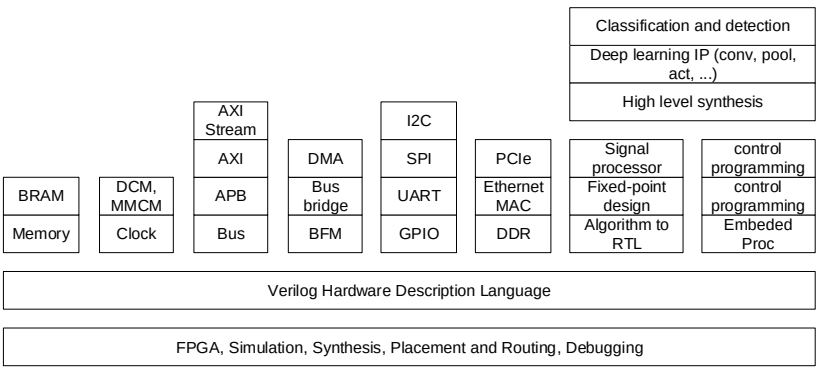
Topics



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Lecture schedule

- Two or three hours per day
- Two or three days per week
- Thursday and Friday

Coding guidelines

- Module name and file name should be the same
- Each directory should have directory clean-up script: Clean.bat, Clean.sh, Makefile
- Each HW IP would contain the following sub-directories

directory		remarks
bench	Test-bench	
	c/verilog/vhdl/systemc	Test-bench written in the specific language
beh	behavioral model if applicable	
	c/verilog/vhdl/systemc	behavioral model written in the specific language
doc	manual and other helpful document	
api (drv)	device driver if applicable and would contains the following sub-directory	
	c	
rtl (design)	RTL model if applicable and would contains sub-directory like 'beh'	
	verilog/vhdl/systemc/c	RTL model written in the specific language
sim	simulation related if applicable	
	modelsim/vcs/ncsim	Sub-directories for HDL simulator
syn	synthesis related if applicable	
	xst/synp/dc/fc/vivado	Sub-directories for logic synthesizer

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