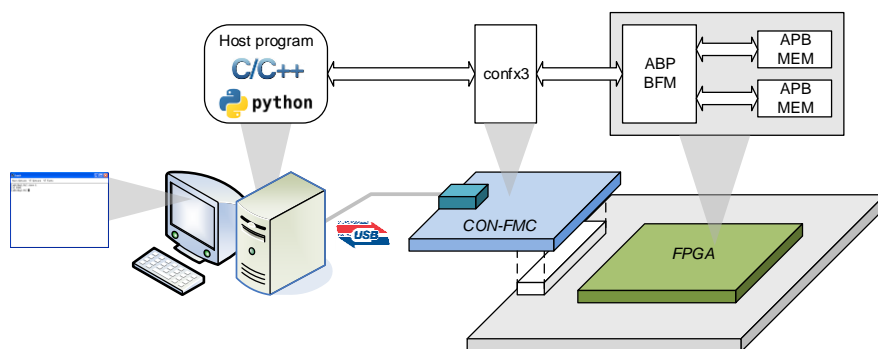


# AMBA APB Memory on FPGA

2020

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## Overall view



## Required packages

❏ Vivado

❏ CON-FMC

◆ 1. Get the package

❖ \$ git clone https://github.com/github-fds/confmc.x86\_64.linux.2020.06.git

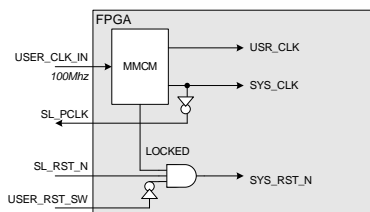
◆ 2. Install the package

❖ \$ cd confmc.x86\_64.linux.2020.06

❖ \$ sudo ./coinstall.sh

## Clock and reset

❏ Directory structure



- ex\_mem\_apb\_fpga
  - beh
    - verilog
  - bench
    - verilog
  - design
    - verilog
  - doc
  - iplib
    - bfm\_apb
    - mem\_apb
  - pnr
    - vivado.zed.lpc
  - sim
    - xsim
  - sw.native
    - test\_mem
      - obj
      - Project1
      - src

## Simulation

❏ Note that there are four 'mem\_apb' blocks with 1Kbyte each

◆ starting address:

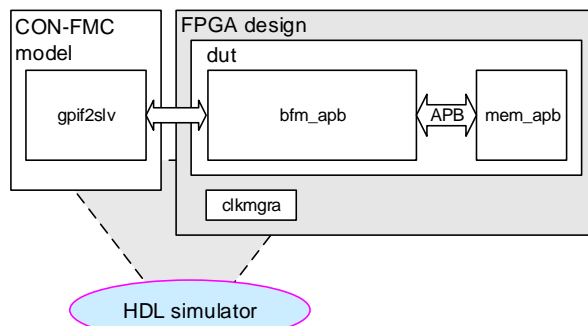
◆ 0x0000\_0000, 0x0001\_0000, 0x0001\_0000, 0x0001\_0000

❏ Go to '...../ex\_mem\_apb\_fpga/sim/xsim' directory and run 'make'

◆ Do not forget to source followings before running

◆ \$ source /tools/Xilinx/Vivado/2018.3/settings64.sh

◆ \$ source /opt/confmc/2020.06/settins.sh



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## P&R (implementation) and program FPGA

❏ Go to '...../ex\_mem\_apb\_fpga/pnr/vivado.zed.lpc' directory and run 'make'

◆ \$ make

◆ or

◆ \$ make GUI=1

❏ Setup FPGA board as shown in the following slide

❏ When 'fpga.bit' is ready, download it through USB-JTAG connection

◆ Go to '...../ex\_mem\_apb\_fpga/pnr/vivado.zed.lpc/download' directory and run 'make'

◆ or invoke 'Hardware manger' from GUI and then download the bit-stream.

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## FPGA board setup



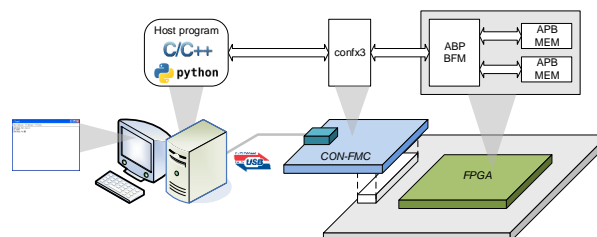
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## Testing program

See 'ex\_mem\_apb\_fpga/sw.native/test\_mem/src/mem\_api.c'

```
# define MEM_WRITE(A, B)    BfmWrite(handle, (unsigned int)(A), &(B), 4, 1)
# define MEM_READ(A, B)    BfmRead (handle, (unsigned int)(A), &(B), 4, 1)
# define MEM_WRITE_G(A,D,S,L) BfmWrite(handle, (A), (D), (S), (L))
# define MEM_READ_G(A,D,S,L) BfmRead(handle, (A), (D), (S), (L))
```



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## Running the design

- Go to native software directory and then run 'make'
  - ◆ (do not forget to source 'CON-FMC' settings.sh)
  - ◆ \$ cd ..... ex\_mem\_apb\_fpga/sw.native/test\_mem
  - ◆ \$ make
  - ◆ \$ make run

## Project

- Prepare 'mem\_apb' using BRAM
- Run following steps.
  - ◆ Simulation
  - ◆ P&R
  - ◆ FPGA running