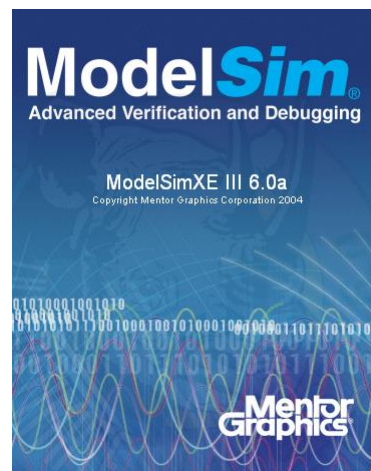
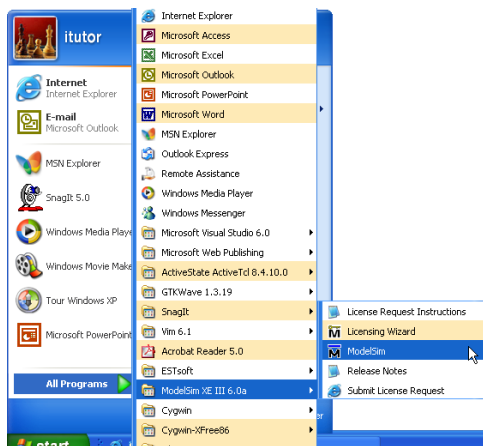


Running ModelSim GUI - Full-Adder Example Case -

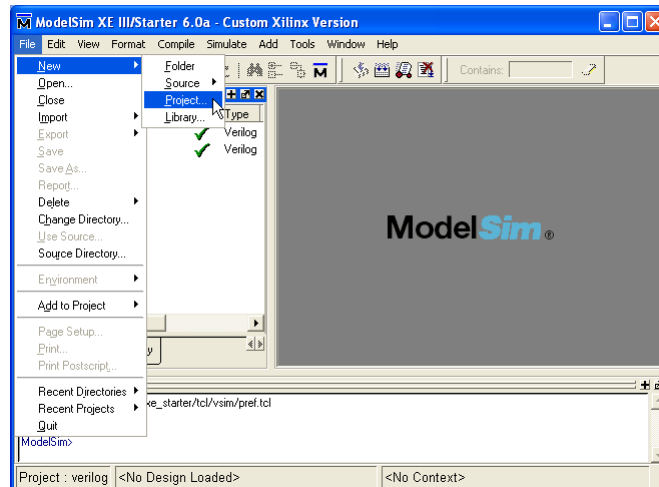
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Oct. 2005.

Invoking ModelSim from start menu



File->New->Project

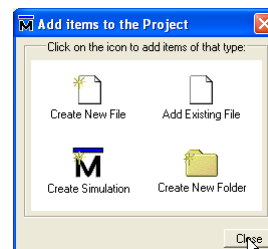
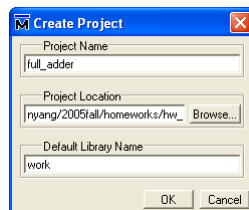


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Specify project name and location

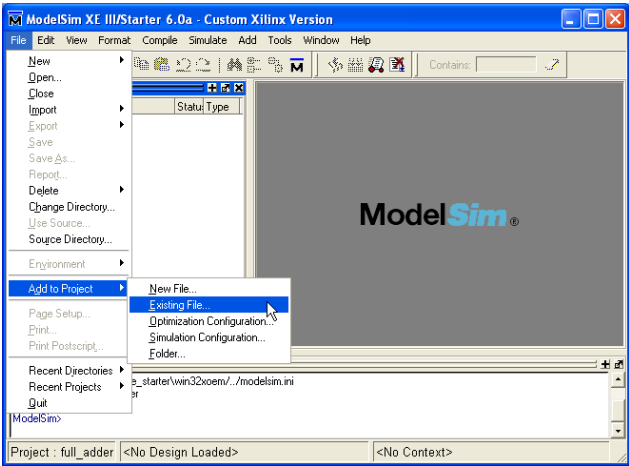


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File->Add to Project->Existing File



ModelSim XE III/Starter 6.0a - Custom Xilinx Version

File Edit View Format Compile Simulate Add Tools Window Help

New Open... Close Import Export Save Save As... Report... Delete Change Directory... Use Source... Source Directory... Environment

Add to Project

- New File...
- Existing File...
- Optimization Configuration...
- Simulation Configuration...
- Folder...


Recent Directories: _starter\win32xoen\...\modelsim.ini

Recent Projects

Quit

ModelSim

Project: full_adder <No Design Loaded> <No Context>

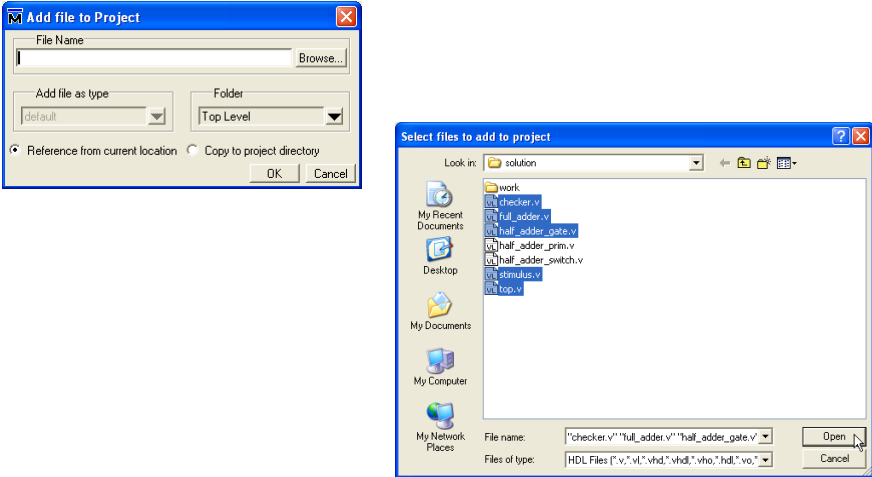


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Add files



Add file to Project

File Name: Browse...

Add file as type: default

Folder: Top Level

☒ Reference from current location ☐ Copy to project directory

OK Cancel

Select files to add to project

Look in: solution

work


- checker.v
- full_adder.v
- half_adder_gate.v
- half_adder_prin.v
- half_adder_switch.v
- stimulus.v
- top.v

My Recent Documents Desktop My Documents My Computer My Network Places

File name: "checker.v" "full_adder.v" "half_adder_gate.v"

Files of type: HDL Files (*.v;*.vhd;*.vhdl;*.vho;*.hdl;*.vo;*)

Open Cancel



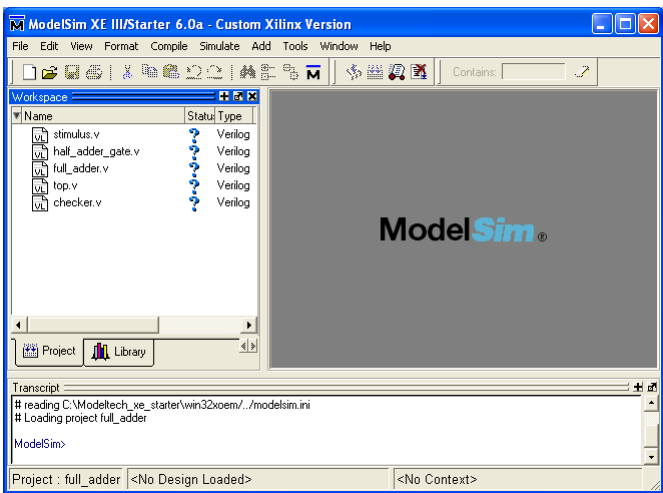
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After adding files



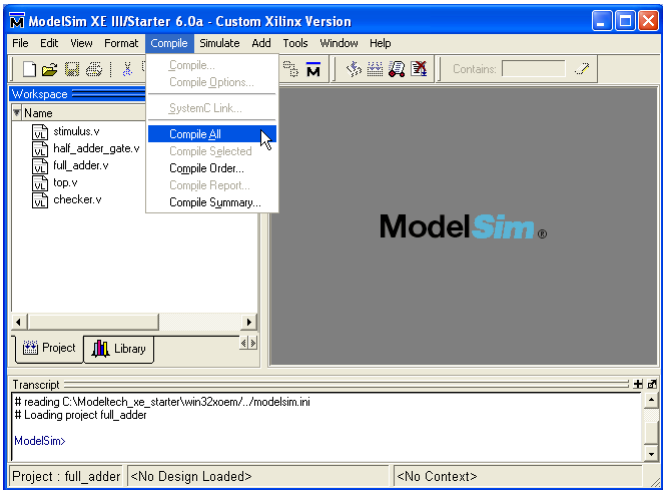
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Compile->Compile All



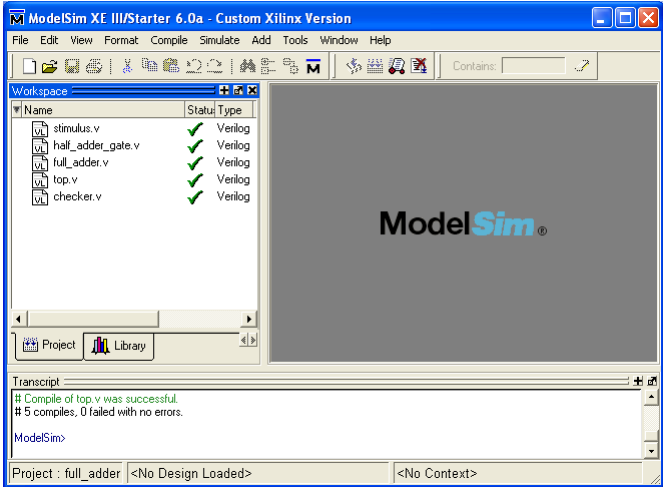
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8

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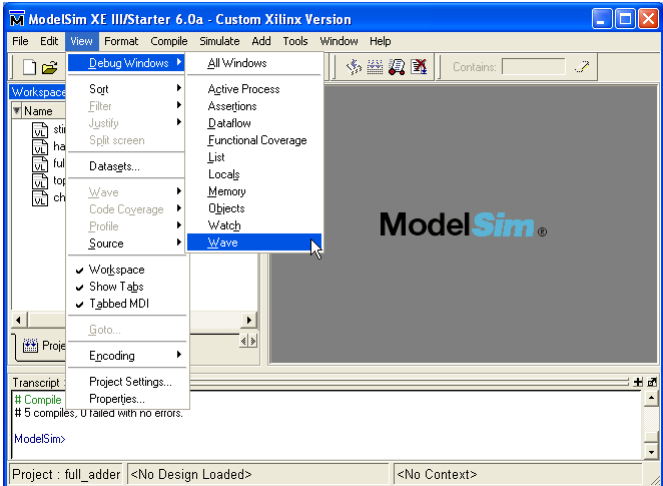
After compilation



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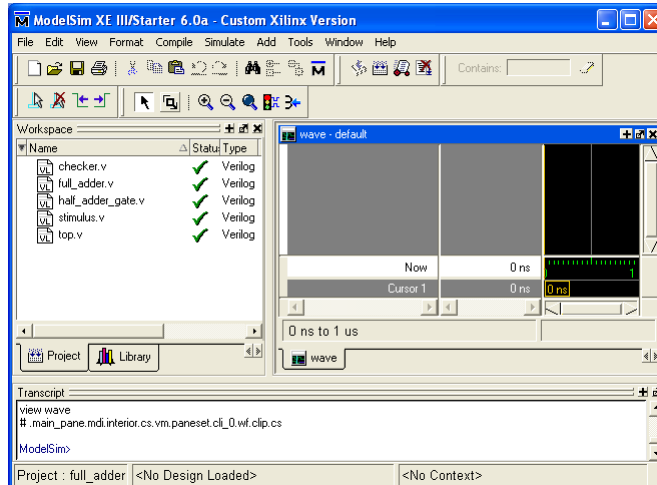


View->Debug Windows->Wave

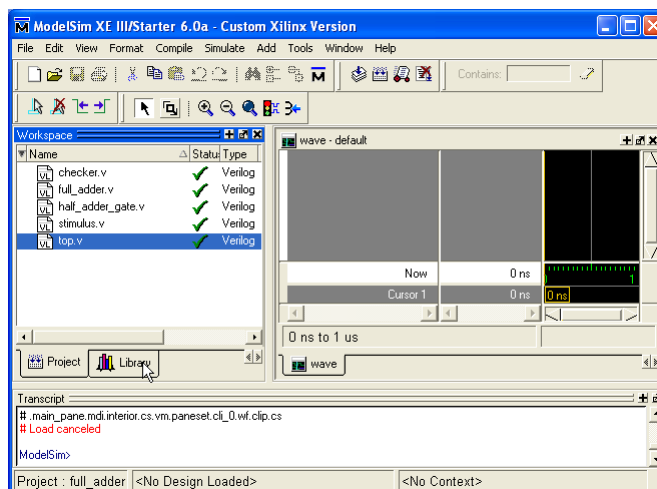


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After adding wave window

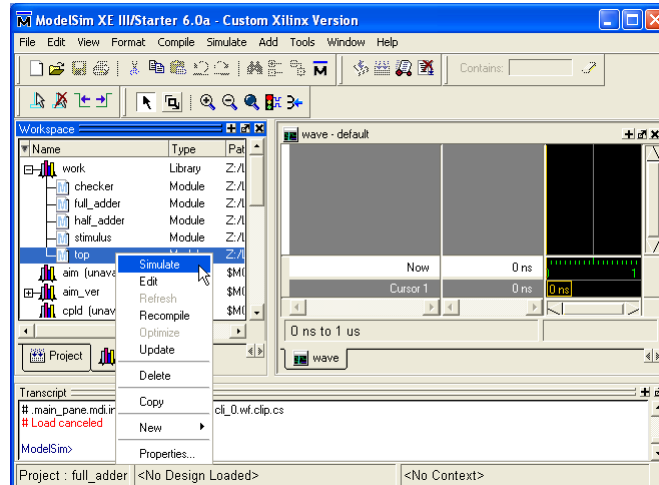


Select Library tab





Run simulation with top-level



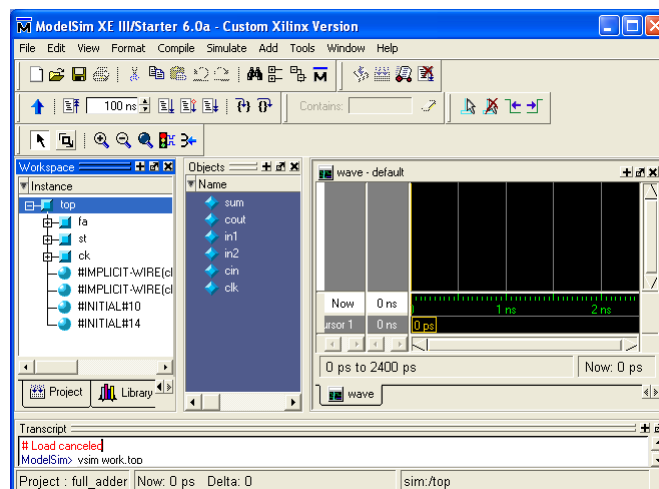
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13

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After simulation

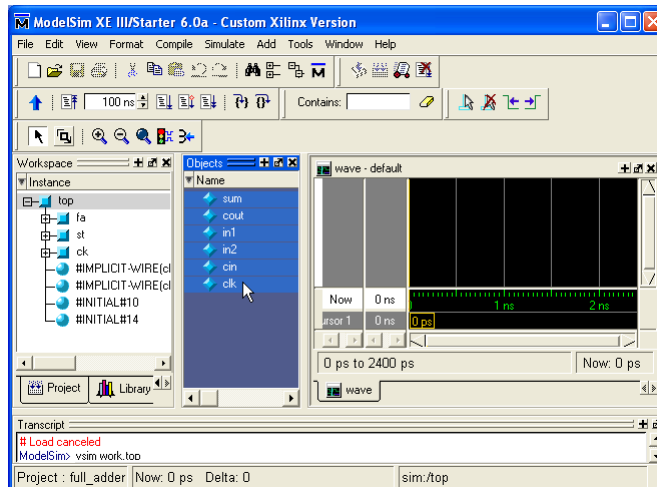


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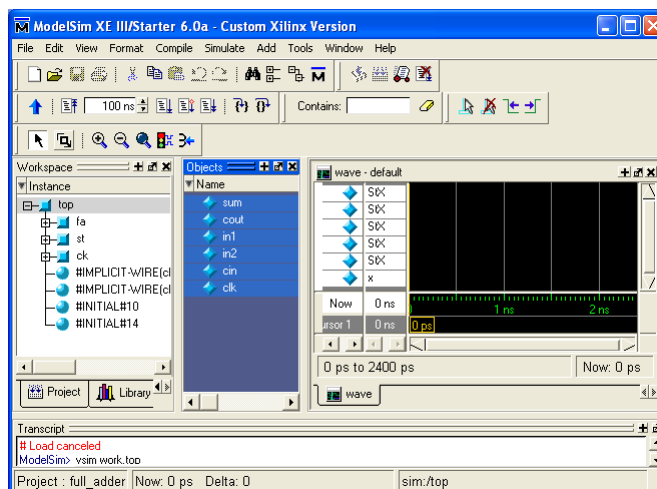
14

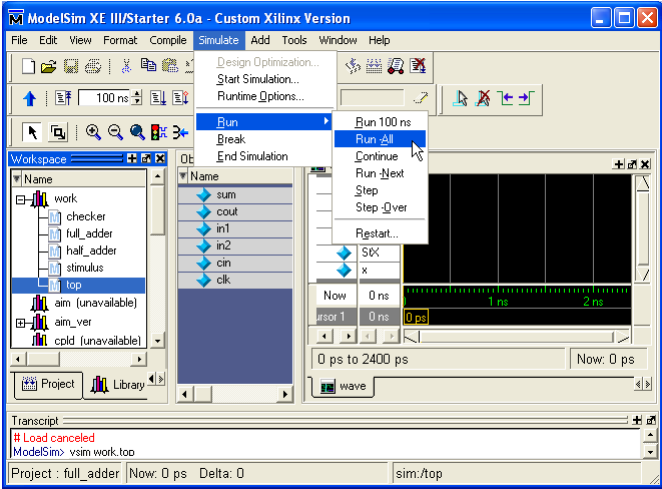
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Selecting signals to be view




After selection






The screenshot shows the ModelSim XE III/Starter 6.0a - Custom Xilinx Version interface. The 'Run' menu is open, showing options like 'Run 100 ns', 'Run -all', 'Continue', 'Run -next', 'Step', 'Step -over', and 'Restart...'. The 'Run -all' option is highlighted. The workspace shows a project named 'full_adder' with a hierarchy of components: 'work' (containing 'checker', 'full_adder', 'half_adder', 'stimulus', 'top'), 'aim' (unavailable), 'aim_ver' (unavailable), and 'cpld' (unavailable). The 'top' component is selected. The 'Name' list shows 'sum', 'cout', 'in1', 'in2', 'cin', and 'clk'. The 'Transcript' window shows the command 'Load canceled' and 'ModelSim> vsim work.top'. The status bar indicates 'Project : full_adder | Now: 0 ps | Delta: 0 | sim:/top'.



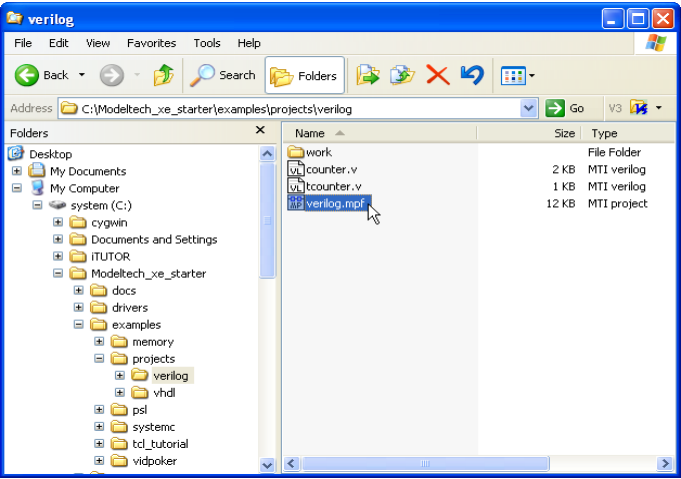
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17

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Invoke ModelSim project (2/9)



The screenshot shows a file explorer window titled 'verilog'. The address bar shows the path 'C:\Modeltech_xe_starter\examples\projects\verilog'. The file list shows the following files and folders:

Name	Size	Type
work		File Folder
counter.v	2 KB	MTI verilog
tccounter.v	1 KB	MTI verilog
verilog.mpf	12 KB	MTI project

The 'verilog.mpf' file is selected. The left pane shows the folder structure, including 'Desktop', 'My Documents', 'My Computer', 'My System (C:)', 'cygwin', 'Documents and Settings', 'ITUTOR', 'Modeltech_xe_starter', 'docs', 'drivers', 'examples', 'memory', 'projects', 'verilog', 'vhdl', 'psl', 'systemc', 'td_tutorial', and 'vidpoker'.

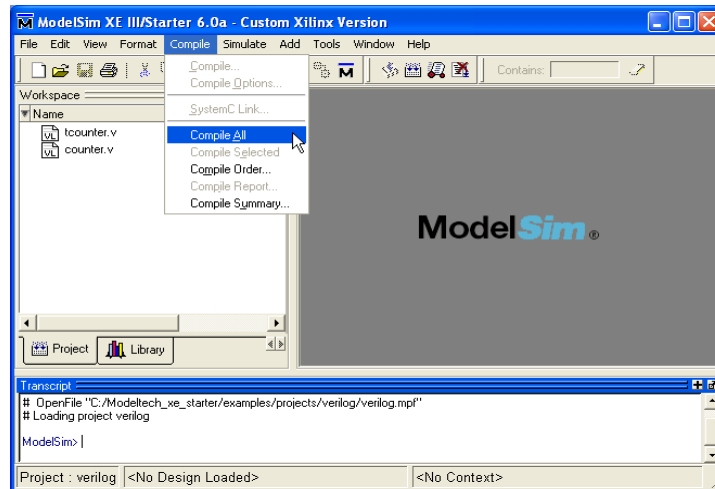


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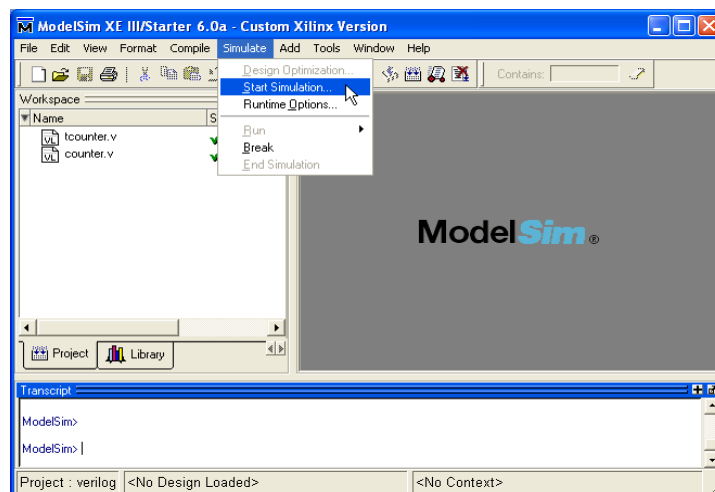
18

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Compile (3/9)

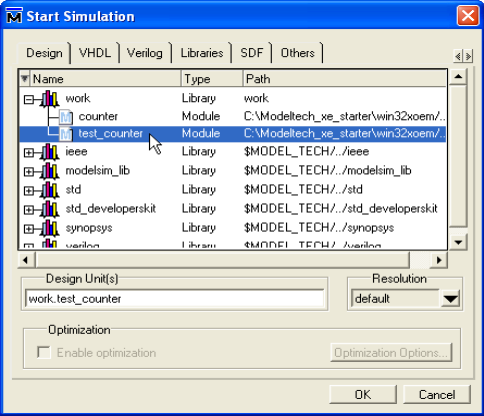


Start simulation (4/9)

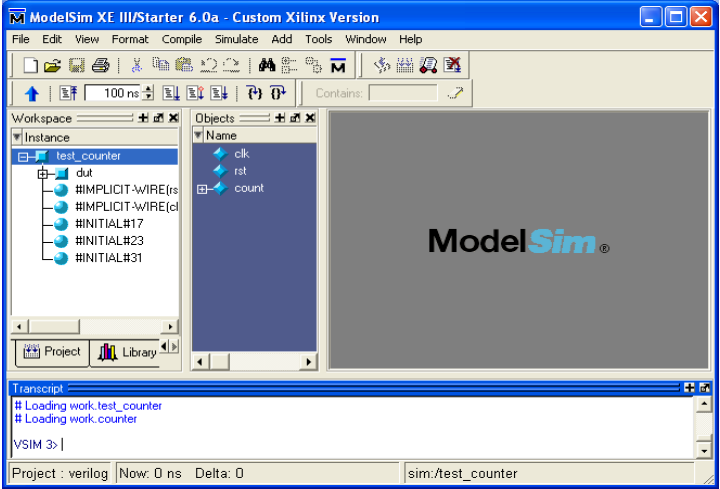




Select top-level (5/9)




After simulation (6/9)



Activate waveform window (7/9)

The screenshot shows the ModelSim XE III/Starter 6.0a - Custom Xilinx Version interface. The 'Debug Windows' menu is open, and the 'Wave' option is highlighted. The main workspace is empty, and the status bar at the bottom shows 'Project : verilog | Now: 0 ns Delta: 0 | sim:/test_counter'.




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Display waveform (8/9)

The screenshot shows the ModelSim XE III/Starter 6.0a - Custom Xilinx Version interface with the 'wave - default' window open. The 'wave - default' window displays a waveform for the 'count' signal, showing a sequence of values: 00000101, 00000000, 00000010, 00000011, 00000100. The status bar at the bottom shows 'Project : verilog | Now: 100 ns Delta: 4'.

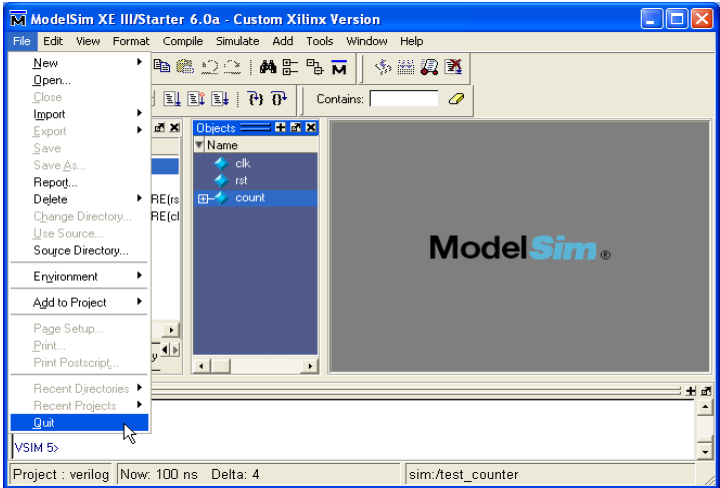



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Exiting ModelSim (9/9)






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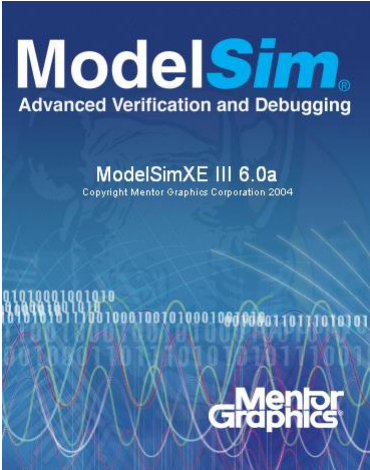
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25

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Invoking ModelSim from desktop icon







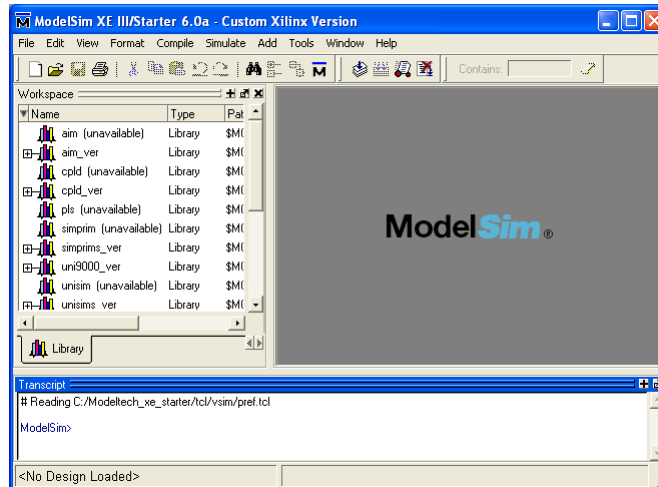
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26

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ModelSim



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