**PCI-EXPRESS FA SNIFFER FPGA DESIGN REGISTER MAPPING**

**Device Control and Status Register (DCSR) - (000H, R/W)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Field** | **Bit(s)** | **Initial**  **Value** | **RO/RW** | **Description** |
| Initiator  Reset | 0 | 0 | W | Initiator Reset:  1’b1 = Reset all PCI Express interface core modules.  Self cleared. |
| Firmware  Version | [15: 0] | Value | RO | Firmware Build Number. |
| Interface  Type | [19:16] | 0x2 | RO | Core Data Path Width:  Hardwired to its initial value. |
| R0 | [23:20] | 0 | RO | Reserved. |
| FPGA  Family | [31:24] | Value | RO | FPGA Family:  0x13: Virtex-5  0x20: Spartan-6 |

**Device DMA Control Status Register (DDMACSR) – (004H, R/W)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Field** | **Bit(s)** | **Initial**  **Value** | **RO/RW** | **Description** |
| Write DMA  Start | 0 | 0 | W | Start Write DMA Operation;  1'b1 = Start the Write DMA Engine.  Self cleared. |
| Write DMA  Stop | 1 | 0 | W | Stop Write DMA Operation;  1'b1 = Stop the Write DMA Engine.  Self cleared. |
| R0 | [ 4: 2] | 0 | RO | Reserved. |
| Write DMA Relaxed Ordering | 5 | 0 | W | Sets Relaxed Ordering attribute bit on TLP. |
| Write DMA  No Snoop | 6 | 0 | W | Sets No Snoop attribute bit on TLP. |
| Write DMA  Interrupt Disable | 7 | 0 | W | 1'b1 = Disable transmission of interrupts. |
| R1 | [31: 8] | 0 | RO | Reserved. |

**Write DMA Host Lower Address (WDMATLPA) (008H, R/W)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Field** | **Bit(s)** | **Initial**  **Value** | **RO/RW** | **Description** |
| Write DMA Host Low Address | [31: 0] | 0 | R/W | Lower Write DMA address on Host PC. |

**Write DMA TLP Size (WDMATLPS) (00CH, R/W)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Field** | **Bit(s)** | **Initial**  **Value** | **RO/RW** | **Description** |
| Write DMA  TLP Size | [ 9: 0] | 0 | R/W | Write DMA TLP Payload Length in DWORDS (1 DWORD = 4 Bytes). |
| R0 | [15:10] | 0 | RO | Reserved |
| Write DMA  Traffic Class | [18:16] | 0 | RW | Memory Write TLP Traffic Class. s; Controls Traffic Class field of the generated TLP. |
| 64-bit Write TLP  Enable | [19] | 0 | R/W | 1'b1 = Enables 64b Memory Write TLP generation. |
| Write DMA  Phantom Disable | [20] | 0 | R/W | 1'b1 = Disables it. ?? |
| R1 | [23: 0] | 0 | RO | Reserved |
| Write DMA Host High Address | [31:24] |  | R/W | Higher Write DMA address on Host PC. |
|  |  |  |  |  |

**Write DMA TLP Count (WDMATLPC) (010H, R/W)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Field** | **Bit(s)** | **Initial**  **Value** | **RO/RW** | **Description** |
| Write DMA Frame  TLP Count | [15: 0] | 0 | WO | Number of TLPs Required to DMA  Single CC Buffer. |

**Write DMA Block Length (WDMABLEN) (WDMADATP) (014H, R/W)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Field** | **Bit(s)** | **Initial**  **Value** | **RO/RW** | **Description** |
| Write DMA  Block Length | [15: 0] | 0 | WO | Number of CC Frames to be transferred into DMA Buffer on host buffer. |

**Communication Controller FAI Value (CCFAICFGVAL) (080H, RW)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Field** | **Bit(s)** | **Initial**  **Value** | **RO/RW** | **Description** |
| FAI Configuration  Value | [31: 0] | 0 | RW | Controls FAI interface for Communication Controller. |

**Write DMA Status Register (WDMASTAT) (084H, RO)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Field** | **Bit(s)** | **Initial**  **Value** | **RO/RW** | **Description** |
| Write DMA Engine Status | [ 3: 0] | 0 | RO | Write DMA Engine Status information on IRQ.  4'b0001 = Completed the dma, and next dma is in progress.  4'b0011 = Completed the dma, next dma is not valid.  4'b0010 = No dma taken place, next dma is not valid.  4'b0100 = User intervention for stop.  4'b1000 = Communication Controller timed out (no incoming data for 300us). |
| R0 | [ 7: 4] | 0 | RO | Reserved. |
| Write DMA  Buffer Pointer | [23: 8] | 0 | RO | Write index for the frame number in host buffer. |
| R1 | [31:24] | 0 | RO | Reserved. |

**Communication Controller Link Status (LINKSTATUS) (088H, RO)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Field** | **Bit(s)** | **Initial**  **Value** | **RO/RW** | **Description** |
| RX Link Up | 0 | 0 | RO | CC RX Link Up. |
| Data Timeout | 1 | 0 | RO | CC Data Receive Timout |
| R0 | [ 7: 2] | 0 | RO | Reserved |
| RX Link Partner | [17: 9] | 0 | RO | CC RX Link Partner ID. |
| R1 | [31:18] | 0 | RO | Reserved. |

**Communication Controller Frame Error Status (FRAMEERRCNT) (08C, RO)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Field** | **Bit(s)** | **Initial**  **Value** | **RO/RW** | **Description** |
| CC Frame Error Count | [31: 0] | 0 | RO | Communication Controller RX Frame Error Count. |

**Communication Controller Soft Error Status (SOFTERRCNT) (090, RO)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Field** | **Bit(s)** | **Initial**  **Value** | **RO/RW** | **Description** |
| CC Soft Error Count | [31: 0] | 0 | RO | Communication Controller RX Soft Error Count. |

**Communication Controller Hard Error Status (HARDERRCNT) (094, RO)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Field** | **Bit(s)** | **Initial**  **Value** | **RO/RW** | **Description** |
| CC Hard Error Count | [31: 0] | 0 | RO | Communication Controller RX Hard Error Count. |

**Communication Controller Node ID (NODEID) (098, RO)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Field** | **Bit(s)** | **Initial**  **Value** | **RO/RW** | **Description** |
| CC Node ID | [9: 0] | 0 | RW | Communication Controller Node ID. |
| Reserved | [31:10] | 0 | RO | Reserved. |

**Communication Controller Timeframe Length (TIMEFRAMELEN) (09C, RO)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Field** | **Bit(s)** | **Initial**  **Value** | **RO/RW** | **Description** |
| CC Timeframe Length | [15: 0] | 0 | RW | CC Timeframe Length in terms of clock ticks. |
| Reserved | [31:16] | 0 | RO | Reserved. |