DXP-xMAP: Mapping Buffer Specification

In mapping mode, the DXP-xMAP uses two completely separate memory buffers, enabling the system to take data into one buffer while the other buffer can be read out y the host. The size of each buffer is 2MB, organized as 1Mword by 16 bits. Several mapping modes will be supported, including mapping with full spectra, mapping with multiple regions of interest (ROI's), and list mode readout.

For all timing modes, the buffer starts out with a buffer header, containing general information about the data contained in the memory block. For all timing modes involving sequential pixels, there is also a pixel header block, typically containing statistics information (used to make pileup corrections on a pixel by pixel basis).

The format of the data contained in the buffers is described in detail in the following sections.

Buffer Header

For all timing applications that use the dual buffers, the buffer header will have a fixed, 256-word length (the word size is 16 bits in this mode). The contents of the header are defined below:

Word Number	Contents
0	Tag Word 0: 0x55AA
1	Tag Word 1: 0xAA55
2	Buffer Header Size (=256)
3	Mapping Mode: 1: Full Spectrum 2: Multiple ROI 3: List Mode
4	Run Number
5 to 6	Sequential Buffer Number (low word first)
7	BufferID (0:A, 1:B)
8	Number of Pixels in buffer
9 to 10	Starting Pixel Number (low word first)
11	Module Serial Number?/Module #

Word Number	Contents
12	Detector Channel 0 (set by host in DSP)
13	Det. Element, Ch0
14	Detector Channel 1 (set by host in DSP)
15	Det. Element, Ch1
16	Detector Channel 2 (set by host in DSP)
17	Det. Element, Ch2
18	Detector Channel 3 (set by host in DSP)
19	Det. Element, Ch3
20	Channel 0 Size (number of words)
21	Channel 1 Size (number of words)
22	Channel 2 Size (number of words)
23	Channel 3 Size (number of words)
24	Buffer errors: Buffer overrun 0: No error >0: Number of extra pixels combined with last pixel in buffer
25-31	Reserved (set to 0)
32-63	32 User words (set in USER array in DSP)
64-95	Channel Statistics for Mapping mode 4 (sparse list mode); Reserved (set to 0) otherwise. Statistics recorded in channel order (Channel 0, 1, 2, 3) Realtime, Livetime, Triggers, Output Events, 2 words each, low word first.
95-255	Reserved (set to 0)

Pixel Data Block

For all mapping modes based upon pixels, the data block for each pixel will start with a pixel header, followed by the data collected for the pixel. The header can differ in size for different mapping applications; in general, the header contains the statistics data required to make pileup corrections ona pixel by pixel basis (livetime, realtime, input triggers, and output events). The full data blocks are described below for the various mapping modes.

Mapping Mode 1: Full Spectrum Mapping

The pixel header for full spectrum mapping mode is described below; due to the constraint that the spectra sizes are a multiple of 256 and must start on an even multiple of 256, the size of the pixel header is 256 words in this mode.

The data block for full spectrum mapping mode contains four sections; each section holds the spectrum from one of the four detector channels in the module. The length of the spectra are constrained to be a multiple of 256, and must start on a memory location that is a multiple of 256. For (at least) the first version of the mapping firmware, the spectra must be the same size for all channels in a system (and will in general equal 256 * 2^n, ie 256, 512, 1024, 2048, etc). The format for the entire pixel block is described in the table below.

Word Number	Contents
0	Tag Word 0: 0x33CC
1	Tag Word 1: 0xCC33
2	Pixel Header Size (=256)
3	Mapping Mode (=1)
4 to 5	Pixel Number (low word first) In the case of a mapping error where one pixel record combines data from several pixels, this is the number of the last pixel recorded.
6 to 7	Total Pixel Block size in words (including header) (low word first)
8	Channel 0 Size (K words)

Word Number	Contents
9	Channel 1 Size (L words)
10	Channel 2 Size (M words)
11	Channel 3 Size (N words)
12 to 31	Reserved (set to 0)
Word Number	Contents
32 to 39	Channel 0 Statistics: Realtime (2 words, low word first) Livetime (2 words) Triggers (2 words) Output events (2 words)
40 to 47	Channel 1 Statistics
48 to 55	Channel 2 Statistics
56 to 63	Channel 3 Statistics
64 to 255	Reserved (set to 0)
256 to (256 + K – 1)	Channel 0 Spectrum
(256 + K) to (256 + K + L – 1)	Channel 1 Spectrum
(256 + K + L) to (256 + K + L + M – 1)	Channel 2 Spectrum
(256 + K + L + M) to (256 + K + L + M + N – 1)	Channel 3 Spectrum

Mapping Mode 2: Multiple SCA Mapping

The pixel header for multiple SCA (or ROI, for Region Of Interest) mapping mode is described below; there is no constraint on the data alignment in the buffer, so the header length is shorter than the 256 words required for full spectrum mapping.

There are four sections in the pixel data block for this mode, containing the SCA totals for each of the four detector channels. Up to 64 SCA's can be defined for each channel. A 16K word array is used to hold the mapping between MCA bins and SCA regions; the user can either select to have all channels use the same SCA definitions for all channels (which supports the full maximum MCA length of 16K channels), or use separate definitions of the SCA regions for each channel (where the maximum supported MCA length is 4K channels). This format specification does allow differences in the number of SCA's between channels. Two words (32 bits total) are used to store the total number of events in each SCA region; the low word is stored first in memory.

The format for the entire pixel data block is described in the table below.

Word Number	Contents
0	Tag Word 0: 0x33CC
1	Tag Word 1: 0xCC33
2	Pixel Header Size (=64)
3	Mapping Mode (=2)
4 to 5	Pixel Number (low word first) In the case of a mapping error where one pixel record combines data from several pixels, this is the number of the last pixel recorded.
6 to 7	Total Pixel block size in words (including header) (low word first)
8	Number of ROI, Channel 0 (K ROI's)
9	Number of ROI, Channel 1 (L ROI's)
10	Number of ROI, Channel 2 (M ROI's)
11	Number of ROI, Channel 3 (N ROI's)
12	ROI Size in words (=2)
13 to 31	Reserved (set to 0)

Word Number	Contents
32 to 39	Channel 0 Statistics: Realtime (2 words, low word first) Livetime (2 words) Triggers (2 words) Output events (2 words)
40 to 47	Channel 1 Statistics (as above)
48 to 55	Channel 2 Statistics (as above)
56 to 63	Channel 3 Statistics (as above)
64 to (64 + 2*K – 1)	Channel 0 ROI data
(64 + 2*K) to (64 + 2*K + 2*L – 1)	Channel 1 ROI data
(64 + 2*K + 2*L) to (64 + 2*K + 2*L + 2*M – 1)	Channel 2 ROI data
(64 + 2*K + 2*L + 2*M) to (64 + 2*K + 2*L + 2*M + 2*N – 1)	Channel 3 ROI data

Mapping Mode 3: Standard List Mode Mapping

The pixel header for standard list mode mapping is described below; there is no constraint on the data alignment in the buffer, so the header length is shorter than the 256 words required for full spectrum mapping. Note that in list mode, the data for all channels is mixed; the channel number is embedded into the data word itself.

For the data block in list mode, each word contains data for a single event. The events are stored in the order they are processed, and so the data are not separated according to channel. The channel number information is embedded into the upper two bits of the data word; the lower 14 bits are sued to store energy information (typically MCA channel number). Note that the channel number recorded in the data word is the local module channel number (0 through 3); data from the buffer header can be used to translate the local channel number into the system detector channel (for a multiple module system).

Word Number	Contents
0	Tag Word 0: 0x33CC
1	Tag Word 1: 0xCC33
2	Pixel Header Size (=64)
3	Mapping Mode (=3)
4 to 5	Pixel Number (low word first) In the case of a mapping error where one pixel record combines data from several pixels, this is the number of the last pixel recorded.
6 to 7	Total Pixel block size in words (including header) (low word first)
8	Number of Channel 0 Events (K)
9	Number of Channel 1 Events (L)
10	Number of Channel 2 Events (M)
11	Number of Channel 3 Events (N)
12	Status: 0: OK 1: Pixel continued in next buffer 2: Pixel continued from last buffer
12 to 31	Reserved (set to 0)

Word Number	Contents
32 to 39	Channel 0 Statistics: Realtime (2 words, low word first) Livetime (2 words) Triggers (2 words) Output events (2 words)
40 to 47	Channel 1 Statistics
48 to 55	Channel 2 Statistics
56 to 63	Channel 3 Statistics
64 to (64 + K + L + M + N -1)	Event data (One 16-bit word per event) Note that the channel number is encoded into the top two bits of each data word (channels 0-3); the bottom 14 bits contain the MCA bin number.

Mapping Mode 4: Sparse List Mode Mapping

Sparse list mode mapping is designed to address situations where the pixel dwell times are very short, and there are typically very few (if any) events recorded for each pixel. For the short dwell times, it is impossible to record the counting statistics for each pixel, both because it takes too long to read out the statistics as well as because the size of the pixel header containing the statistics would overwhelm the event data. For sparse list mode, the energy and the lower word of the pixel number are recorded for each event, with no formal pixel header. The full pixel number (two 16-bit words) is recorded in the buffer header; if the pixel number overflows during the course of the buffer processing, a special event (event energy word 0xFFFF followed by the high order pixel word) will be recorded in the buffer to indicate the need to increment the high order pixel word. In addition, the last two words stored in the buffer will be the same special event energy word followed by the high pixel number word at the time of the end of the buffer. Note that in order to guarantee that that event energy is unique, the MCA size in fast list mode is restricted to 8k bins; the MCA bin will be stored in bits 0 through 12, and the channel number will be stored in bits 13 and 14. In order to allow a pixel-averaged pileup correction, the event statistics are recorded in the buffer header (words 64-95) for the entire collection time corresponding to that buffer.

The buffer data block for sparse list mode mapping is described in the table below.

Word Number	Contents
0-255	Buffer Header (see above)
256	Event energy: Bits 0-12: MCA bin Bits 13-14: Module channel number Bit 15: 0
257	Event pixel, low word
…	Event by event data continues
2K	Event energy
2K + 1	Event pixel, low word
…	Event by event data continues
2L	Pixel number rollover indicator: 0xFFFF
2L+1	Pixel number, new high word
…	Event by event data continues
2M	Event energy
2M + 1	Event pixel, low word
…	Event by event data continues
LastWord – 1	0xFFFF
LastWord	Pixel number, high word at end of buffer