RFM69

Doxygen 1.8.8

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Contents

Chapter 1

1.1

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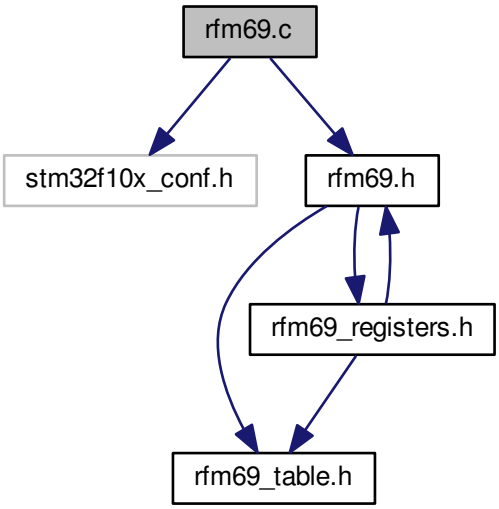
Chapter 2

2.1 rfm69.c

```
#include "stm32f10x_conf.h"
#include "rfm69.h"
```

rfm69.c:



- void EXTI2_IRQHandler (void)
- void EXTI1_IRQHandler (void)
- void EXTI0_IRQHandler (void)
- void TIM2_IRQHandler (void)
- void rfm69_write (uint8_t address, uint8_t data)
- uint8_t rfm69_read (uint8_t address)
- void rfm69_write_burst (uint8_t address, uint8_t *data, uint8_t ndata)
- void rfm69_read_burst (uint8_t address, uint8_t *data, uint8_t ndata)
- void rfm69_mcu_init (void)
- int rfm69_init (void)
- int rfm69_transmit_start (uint8_t packet_size_loc, uint8_t address)

- void rfm69_receive_start (void)
- int rfm69_receive_small_packet (void)
- void rfm69_sleep (void)
- void rfm69_stby (void)
- void rfm69_clear_fifo (void)

- uint8_t packet_buffer [64]
- uint8_t rfm69_condition
- uint8_t packet_size
- uint8_t internal_packet_buffer [64]
- uint8_t internal_pack_size

2.1.1

2.1.1.1 void EXTI0_IRQHandler (void)

2.1.1.2 void EXTI1_IRQHandler (void)

2.1.1.3 void EXTI2_IRQHandler (void)

2.1.1.4 void rfm69_clear_fifo (void)

2.1.1.5 int rfm69_init (void)

2.1.1.6 void rfm69_mcu_init (void)

2.1.1.7 uint8_t rfm69_read (uint8_t *address*)

2.1.1.8 void rfm69_read_burst (uint8_t *address*, uint8_t * *data*, uint8_t *ndata*)

2.1.1.9 int rfm69_receive_small_packet (void)

2.1.1.10 void rfm69_receive_start (void)

2.1.1.11 void rfm69_sleep (void)

2.1.1.12 void rfm69_stby (void)

2.1.1.13 int rfm69_transmit_start (uint8_t *packet_size_loc*, uint8_t *address*)

2.1.1.14 void rfm69_write (uint8_t *address*, uint8_t *data*)

2.1.1.15 void rfm69_write_burst (uint8_t *address*, uint8_t * *data*, uint8_t *ndata*)

2.1.1.16 void TIM2_IRQHandler (void)

2.1.2

2.1.2.1 uint8_t internal_pack_size

2.1.2.2 uint8_t internal_packet_buffer[64]

2.1.2.3 uint8_t packet_buffer[64]

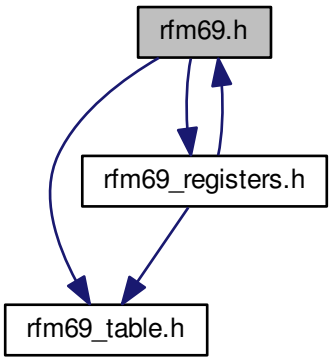
2.1.2.4 uint8_t packet_size

2.1.2.5 uint8_t rfm69_condition

2.2 rfm69.h

```
#include "rfm69_table.h"
#include "rfm69_registers.h"
```

rfm69.h:



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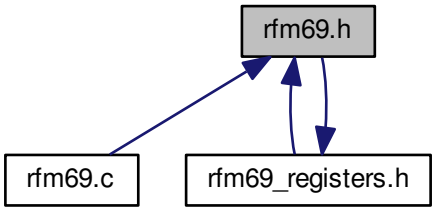


- #define OOK 0x08
- #define FSK 0x00
- #define BITRATE 9600
- #define CARRIER_FREQ 868250000
- #define OUTPUT_POWER 13

- #define RX_BW 65
- #define RX_BW_AFC 130
- #define OCP_CURRENT 95
- #define MODUL_TYPE FSK

  modulation
- #define DEVIATION 20000

  FSK parametres.
- #define RISE_FALL_TIME_FSK 50
- #define OOK_PEAK_THRES_STEP 1

  OOK parametres.
- #define OOK_PEAK_THRESH_DEC 1
- #define OOKFIXEDTHRESH 6
- #define PREAMBLE 4

  Packet handler configuration.
- #define SYNC_WORD_SIZE 4
- #define SYNC_WORD 0x753be1ca753be1ca
- #define SYNCTOL 2
- #define RX_ADDRESS 0x05
- #define BROADCAST_ADDRESS 0xff
- #define AUTO_RESTART_RX_DELAY 1
- #define RSSI_THRESH 88
- #define FIFO_THRESHOLD 32
- #define CUT_OFF_FREQ 4
- #define CUT_OFF_FREQ_AFC 4
- #define FXOSC 32000000
- #define FSTEP 61
- #define PI 3.14159265359
- #define RFM69_BUFFER_SIZE 66
- #define REGOPMODE_DEF (0<<SEQUENCEROFF | 0<<LISTENON | SLEEP_MODE)
- #define REGDATAMODUL_DEF (PACKET_MODE | MODUL_TYPE | GAUSS_BT10)
- #define REGFDEVMSB_DEF ((FDEV_CALC(DEVIATION) & 0xff00) >> 8)
- #define REGFDEVLSB_DEF (FDEV_CALC(DEVIATION) & 0x00ff)
- #define REGBITRATEMSB_DEF ((BITRATE_CALC(BITRATE) & 0xff00) >> 8)
- #define REGBITRATELSB_DEF (BITRATE_CALC(BITRATE) & 0x00ff)
- #define REGFRFMSB_DEF ((FRF_CALC(CARRIER_FREQ) & 0xff0000) >> 16)
- #define REGFRFMID_DEF ((FRF_CALC(CARRIER_FREQ) & 0x00ff00) >> 8)
- #define REGFRFLSB_DEF (FRF_CALC(CARRIER_FREQ) & 0x0000ff)
- #define REGAFCCTRL_DEF (0<<(AFCLOWBETAON))
- #define REGLISTEN1_DEF (0x00)
- #define REGLISTEN2_DEF (0x00)
- #define REGLISTEN3_DEF (0x00)
- #define REGPALEVEL_DEF (1<<PA0ON | 0<<PA1ON | 0<<PA2ON | (OUT_POWER_CALC(OUTPU↩T_POWER)))
- #define REGPARAMP_DEF (PARAMP)
- #define REGOCP_DEF (1<<OCPON | (OCP_CURRENT_CALC(OCP_CURRENT)))
- #define REGLNA_DEF (1<<LNAZIN | LNAGAIN_AUTO)
- #define REGRXBW_DEF (DCCFREQ | RXBW)
- #define REGAFCBW_DEF (DCCFREQAFC | RXBWAFC)
- #define REGOOKPEAK_DEF (0x00)
- #define REGOOKAVG_DEF (0x00)
- #define REGOOKFIX_DEF (0x00)
- #define REGAFCFEI_DEF ((1<<AFCAUTOCLEAR) | (1<<AFCAUTOON))
- #define REGDIOMAPPING1_DEF (DIO0MAP0 | DIO1MAP0 | DIO2MAP2 | DIO3MAP1)
- #define REGDIOMAPPING2_DEF (DIO5MAP0 | CLKOUT8M)

- #define REGRSSITHRESH_DEF (RSSI_THRESH_CALC(RSSI_THRESH))
- #define REGPREAMBLEMSB_DEF ((PREAMBLE & 0xff00) >> 8)
- #define REGPREAMBLELSB_DEF (PREAMBLE & 0x00ff)
- #define REGSYNCCONFIG_DEF (SYNC_WORD_ON | 0<<FIFOFILLCOND | SYNCSIZE_CALC(SYNC↩_WORD_SIZE) | (SYNCTOL&0x07))
- #define REGSYNCVALUE1_DEF (SYNC_WORD & 0x00000000000000ff)
- #define REGSYNCVALUE2_DEF ((SYNC_WORD & 0x000000000000ff00) >> 8)
- #define REGSYNCVALUE3_DEF ((SYNC_WORD & 0x0000000000ff0000) >> 16)
- #define REGSYNCVALUE4_DEF ((SYNC_WORD & 0x00000000ff000000) >> 24)
- #define REGSYNCVALUE5_DEF ((SYNC_WORD & 0x000000ff00000000) >> 32)
- #define REGSYNCVALUE6_DEF ((SYNC_WORD & 0x0000ff0000000000) >> 40)
- #define REGSYNCVALUE7_DEF ((SYNC_WORD & 0x00ff000000000000) >> 48)
- #define REGSYNCVALUE8_DEF ((SYNC_WORD & 0xff00000000000000) >> 56)
- #define REGPACKETCONFIG1_DEF (1<<PACKETFORMAT | ENCODING_OFF | 1<<CRCON | 0<<CRCAUTOCLEAROFF | NODE_BROADCAST_ADDR)
- #define REGPAYLOADLENGHT_DEF (0xff)
- #define REGNODEADRS_DEF (RX_ADDRESS)
- #define REGBROADCASTADRS_DEF (BROADCAST_ADDRESS)
- #define REGAUTOMODES_DEF (0x00)
- #define REGFIFOTHRES_DEF (1<<TXSTARTCOND | (FIFO_THRESHOLD&0x7f))
- #define REGPACKETCONFIG2_DEF (INTERPACKETRXDELAY | 1<<AUTORXRESTARTON | 0<<A↩ESON)
- #define REGAESKEY1_DEF (0x00)
- #define REGAESKEY2_DEF (0x00)
- #define REGAESKEY3_DEF (0x00)
- #define REGAESKEY4_DEF (0x00)
- #define REGAESKEY5_DEF (0x00)
- #define REGAESKEY6_DEF (0x00)
- #define REGAESKEY7_DEF (0x00)
- #define REGAESKEY8_DEF (0x00)
- #define REGAESKEY9_DEF (0x00)
- #define REGAESKEY10_DEF (0x00)
- #define REGAESKEY11_DEF (0x00)
- #define REGAESKEY12_DEF (0x00)
- #define REGAESKEY13_DEF (0x00)
- #define REGAESKEY14_DEF (0x00)
- #define REGAESKEY15_DEF (0x00)
- #define REGAESKEY16_DEF (0x00)
- #define CRCOK_PKSent_Line EXTI_Line2
- #define FifoLevel_Line EXTI_Line1
- #define SyncAddr_Line EXTI_Line0
- #define NSS_Port GPIOA
- #define NSS_Pin GPIO_Pin_3
- #define EXTI_Port1 GPIO_PortSourceGPIOB
- #define EXTI_Port23 GPIO_PortSourceGPIOA
- #define EXTI_Pin1 GPIO_PinSource0
- #define EXTI_Pin2 GPIO_PinSource1
- #define EXTI_Pin3 GPIO_PinSource2
- #define RFM69_SYNCADDR_PERIOD PREAMBLE + SYNC_WORD_SIZE + 1

- enum {
  RFM69_SPI_FAILED = 1, RFM69_SLEEP, RFM69_STBY, RFM69_RX,
  RFM69_TX, RFM69_NEW_PACK }

- void rfm69_write (uint8_t address, uint8_t data)
- uint8_t rfm69_read (uint8_t address)
- void rfm69_write_burst (uint8_t address, uint8_t *data, uint8_t ndata)
- void rfm69_read_burst (uint8_t address, uint8_t *data, uint8_t ndata)
- void rfm69_mcu_init (void)
- int rfm69_init (void)
- int rfm69_transmit_start (uint8_t packet_size, uint8_t address)
- void rfm69_receive_start (void)
- int rfm69_receive_small_packet (void)
- void rfm69_sleep (void)
- void rfm69_stby (void)
- void rfm69_clear_fifo (void)

2.2.1

2.2.1.1 #define AUTO_RESTART_RX_DELAY 1

2.2.1.2 #define BITRATE 9600

2.2.1.3 #define BROADCAST_ADDRESS 0xff

2.2.1.4 #define CARRIER_FREQ 868250000

2.2.1.5 #define CRCOK_PKSent_Line EXTI_Line2

2.2.1.6 #define CUT_OFF_FREQ 4

2.2.1.7 #define CUT_OFF_FREQ_AFC 4

2.2.1.8 #define DEVIATION 20000

FSK parametres.

2.2.1.9 #define EXTI_Pin1 GPIO_PinSource0

2.2.1.10 #define EXTI_Pin2 GPIO_PinSource1

2.2.1.11 #define EXTI_Pin3 GPIO_PinSource2

2.2.1.12 #define EXTI_Port1 GPIO_PortSourceGPIOB

2.2.1.13 #define EXTI_Port23 GPIO_PortSourceGPIOA

2.2.1.14 #define FIFO_THRESHOLD 32

2.2.1.15 #define FifoLevel_Line EXTI_Line1

2.2.1.16 #define FSK 0x00

2.2.1.17 #define FSTEP 61

2.2.1.18 #define FXOSC 32000000

2.2.1.19 #define MODUL_TYPE FSK

modulation

2.2.1.20 #define NSS_Pin GPIO_Pin_3

2.2.1.21 #define NSS_Port GPIOA

2.2.1.22 #define OCP_CURRENT 95

2.2.1.23 #define OOK 0x08

2.2.1.24 #define OOK_PEAK_THRES_STEP 1

OOK parametres.

2.2.1.25 #define OOK_PEAK_THRESH_DEC 1

2.2.1.26 #define OOKFIXEDTHRESH 6

2.2.1.27 #define OUTPUT_POWER 13

2.2.1.28 #define PI 3.14159265359

2.2.1.29 #define PREAMBLE 4

Packet handler configuration.

2.2.1.30 #define REGAESKEY10_DEF (0x00)

2.2.1.31 #define REGAESKEY11_DEF (0x00)

2.2.1.32 #define REGAESKEY12_DEF (0x00)

2.2.1.33 #define REGAESKEY13_DEF (0x00)

2.2.1.34 #define REGAESKEY14_DEF (0x00)

2.2.1.35 #define REGAESKEY15_DEF (0x00)

2.2.1.36 #define REGAESKEY16_DEF (0x00)

2.2.1.37 #define REGAESKEY1_DEF (0x00)

2.2.1.38 #define REGAESKEY2_DEF (0x00)

2.2.1.39 #define REGAESKEY3_DEF (0x00)

2.2.1.40 #define REGAESKEY4_DEF (0x00)

2.2.1.41 #define REGAESKEY5_DEF (0x00)

2.2.1.42 #define REGAESKEY6_DEF (0x00)

2.2.1.43 #define REGAESKEY7_DEF (0x00)

2.2.1.44 #define REGAESKEY8_DEF (0x00)

2.2.1.45 #define REGAESKEY9_DEF (0x00)

2.2.1.46 #define REGAFCBW_DEF (DCCFREQAFC | RXBWAFC)

2.2.1.47 #define REGAFCCTRL_DEF (0<<(AFCLOWBETAON))

2.2.1.48 #define REGAFCFEI_DEF ((1<<AFCAUTOCLEAR) | (1<<AFCAUTOON))

2.2.1.49 #define REGAUTOMODES_DEF (0x00)

2.2.1.50 #define REGBITRATELSB_DEF (BITRATE_CALC(BITRATE) & 0x00ff)

2.2.1.51 #define REGBITRATEMSB_DEF ((BITRATE_CALC(BITRATE) & 0xff00) >> 8)

2.2.1.52 #define REGBROADCASTADRS_DEF (BROADCAST_ADDRESS)

2.2.1.53 #define REGDATAMODUL_DEF (PACKET_MODE | MODUL_TYPE | GAUSS_BT10)

2.2.1.54 #define REGDIOMAPPING1_DEF (DIO0MAP0 | DIO1MAP0 | DIO2MAP2 | DIO3MAP1)

2.2.1.55 #define REGDIOMAPPING2_DEF (DIO5MAP0 | CLKOUT8M)

2.2.1.56 #define REGFDEVLSB_DEF (FDEV_CALC(DEVIATION) & 0x00ff)

2.2.1.57 #define REGFDEVMSB_DEF ((FDEV_CALC(DEVIATION) & 0xff00) >> 8)

2.2.1.58 #define REGFIFOTHRES_DEF (1<<TXSTARTCOND | (FIFO_THRESHOLD&0x7f))

2.2.1.59 #define REGFRFLSB_DEF (FRF_CALC(CARRIER_FREQ) & 0x0000ff)

2.2.1.60 #define REGFRFMID_DEF ((FRF_CALC(CARRIER_FREQ) & 0x00ff00) >> 8)

2.2.1.61 #define REGFRFMSB_DEF ((FRF_CALC(CARRIER_FREQ) & 0xff0000) >> 16)

2.2.1.62 #define REGLISTEN1_DEF (0x00)

2.2.1.63 #define REGLISTEN2_DEF (0x00)

2.2.1.64 #define REGLISTEN3_DEF (0x00)

2.2.1.65 #define REGLNA_DEF (1<<LNAZIN | LNAGAIN_AUTO)

2.2.1.66 #define REGNODEADRS_DEF (RX_ADDRESS)

2.2.1.67 #define REGOCP_DEF (1<<OCPON | (OCP_CURRENT_CALC(OCP_CURRENT)))

2.2.1.68 #define REGOOKAVG_DEF (0x00)

2.2.1.69 #define REGOOKFIX_DEF (0x00)

2.2.1.70 #define REGOOKPEAK_DEF (0x00)

2.2.1.71 #define REGOPMODE_DEF (0<<SEQUENCEROFF | 0<<LISTENON | SLEEP_MODE)

2.2.1.72 #define REGPACKETCONFIG1_DEF (1<<PACKETFORMAT | ENCODING_OFF | 1<<CRCON | 0<<CRCAUTOCLEAROFF | NODE_BROADCAST_ADDR)

2.2.1.73 #define REGPACKETCONFIG2_DEF (INTERPACKETRXDELAY | 1<<AUTORXRESTARTON | 0<<AESON)

2.2.1.74 #define REGPALEVEL_DEF (1<<PA0ON | 0<<PA1ON | 0<<PA2ON | (OUT_POWER_CALC(OUTPUT_↩ POWER)))

2.2.1.75 #define REGPARAMP_DEF (PARAMP)

2.2.1.76 #define REGPAYLOADLENGHT_DEF (0xff)

2.2.1.77 #define REGPREAMBLELSB_DEF (PREAMBLE & 0x00ff)

2.2.1.78 #define REGPREAMBLEMSB_DEF ((PREAMBLE & 0xff00) >> 8)

2.2.1.79 #define REGRSSITHRESH_DEF (RSSI_THRESH_CALC(RSSI_THRESH))

2.2.1.80 #define REGRXBW_DEF (DCCFREQ | RXBW)

2.2.1.81 #define REGSYNCCONFIG_DEF (SYNC_WORD_ON | 0<<FIFOFILLCOND | SYNCSIZE_CALC(SYNC_WORD_SIZE) | (SYNCTOL&0x07))

2.2.1.82 #define REGSYNCVALUE1_DEF (SYNC_WORD & 0x00000000000000ff)

2.2.1.83 #define REGSYNCVALUE2_DEF ((SYNC_WORD & 0x000000000000ff00) >> 8)

2.2.1.84 #define REGSYNCVALUE3_DEF ((SYNC_WORD & 0x0000000000ff0000) >> 16)

2.2.1.85 #define REGSYNCVALUE4_DEF ((SYNC_WORD & 0x00000000ff000000) >> 24)

2.2.1.86 #define REGSYNCVALUE5_DEF ((SYNC_WORD & 0x000000ff00000000) >> 32)

2.2.1.87 #define REGSYNCVALUE6_DEF ((SYNC_WORD & 0x0000ff0000000000) >> 40)

2.2.1.88 #define REGSYNCVALUE7_DEF ((SYNC_WORD & 0x00ff000000000000) >> 48)

2.2.1.89 #define REGSYNCVALUE8_DEF ((SYNC_WORD & 0xff00000000000000) >> 56)

2.2.1.90 #define RFM69_BUFFER_SIZE 66

2.2.1.91 #define RFM69_SYNCADDR_PERIOD PREAMBLE + SYNC_WORD_SIZE + 1

2.2.1.92 #define RISE_FALL_TIME_FSK 50

2.2.1.93 #define RSSI_THRESH 88

2.2.1.94 #define RX_ADDRESS 0x05

2.2.1.95 #define RX_BW 65

2.2.1.96 #define RX_BW_AFC 130

2.2.1.97 #define SYNC_WORD 0x753be1ca753be1ca

2.2.1.98 #define SYNC_WORD_SIZE 4

2.2.1.99 #define SyncAddr_Line EXTI_Line0

2.2.1.100 #define SYNCTOL 2

2.2.2

2.2.2.1 anonymous enum

RFM69_SPI_FAILED

RFM69_SLEEP

RFM69_STBY

RFM69_RX

RFM69_TX

RFM69_NEW_PACK

2.2.3

2.2.3.1 void rfm69_clear_fifo (void)

2.2.3.2 int rfm69_init (void)

2.2.3.3 void rfm69_mcu_init (void)

2.2.3.4 uint8_t rfm69_read (uint8_t *address*)

2.2.3.5 void rfm69_read_burst (uint8_t *address*, uint8_t * *data*, uint8_t *ndata*)

2.2.3.6 int rfm69_receive_small_packet (void)

2.2.3.7 void rfm69_receive_start (void)

2.2.3.8 void rfm69_sleep (void)

2.2.3.9 void rfm69_stby (void)

2.2.3.10 int rfm69_transmit_start (uint8_t *packet_size*, uint8_t *address*)

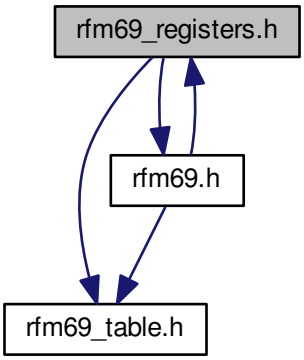
2.2.3.11 void rfm69_write (uint8_t *address*, uint8_t *data*)

2.2.3.12 void rfm69_write_burst (uint8_t *address*, uint8_t * *data*, uint8_t *ndata*)

2.3 rfm69_registers.h

```
#include "rfm69_table.h"
#include "rfm69.h"
```

rfm69_registers.h:



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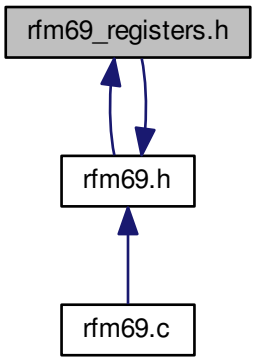

- #define REGFIFO 0x00
- #define REGOPMODE 0x01
- #define SEQUENCEROFF 7
- #define LISTENON 6
- #define LISTENABORT 5
- #define RX_MODE 0x10
- #define TX_MODE 0x0c
- #define FS_MODE 0x08
- #define STBY_MODE 0x04
- #define SLEEP_MODE 0x00
- #define REGDATAMODUL 0x02

- #define CONT_MODE 0x60
- #define CONT_SYNCH_MODE 0x40
- #define PACKET_MODE 0x00
- #define GAUSS_BT03 0x03
- #define GAUSS_BT05 0x02
- #define GAUSS_BT10 0x01
- #define NO_SHAPING 0x00
- #define REGBITRATEMSB 0x03
- #define REGBITRATELSB 0x04
- #define BITRATE_CALC(br_par) FXOSC/(br_par)
- #define REGFDEVMSB 0x05
- #define REGFDEVLSB 0x06
- #define FDEV_CALC(fdev_par) (fdev_par)/FSTEP
- #define REGFRFMSB 0x07
- #define REGFRFMID 0x08
- #define REGFRFLSB 0x09
- #define FRF_CALC(frf_par) (frf_par)/FSTEP
- #define REGOSC1 0x0a
- #define RCCALSTART 7
- #define RCCALDONE 6
- #define REGAFCCTRL 0x0b
- #define AFCLOWBETAON 5
- #define REGLISTEN1 0x0d
- #define LISTENIDLE262M 0xc0
- #define LISTENIDLE4M1 0x80
- #define LISTENIDLE64U 0x40
- #define LISTENRX262M 0x30
- #define LISTENRX4M1 0x20
- #define LISTENRX64U 0x10
- #define LISTENCRITERIA 3
- #define LISTENEND1 0x00
- #define LISTENEND2 0x02
- #define LISTENEND3 0x04
- #define LISTENEND4 0x06
- #define REGLISTEN2 0x0e
- #define REGLISTEN3 0x0f
- #define REGVERSION 0x10
- #define REGPALEVEL 0x11
- #define PA0ON 7
- #define PA1ON 6
- #define PA2ON 5
- #define OUT_POWER_CALC(power_par) 0x1f&(18 + (power_par))
- #define REGPARAMP 0x12
- #define REGOCP 0x13
- #define OCPON 4
- #define OCP_CURRENT_CALC(ocp_param) 0x0f&(((ocp_param)/5) - 9)
- #define REGLNA 0x18
- #define LNAZIN 7
- #define LNAGAIN_AUTO 0x00
- #define LNAGAIN_0DB 0x01
- #define LNAGAIN_6DB 0x02
- #define LNAGAIN_12DB 0x03
- #define LNAGAIN_24DB 0x04
- #define LNAGAIN_36DB 0x05
- #define LNAGAIN_48DB 0x06

- #define REGRXBW 0x19
- #define REGAFCBW 0x1a
- #define REGOOKPEAK 0x1b
- #define OOKTHRESFIXED 0x00
- #define OOKTHRESPEAK 0x40
- #define OOKTHRESAVERAGE 0x80
- #define REGOOKAVG 0x1c
- #define REGOOKFIX 0x1d
- #define REGAFCFEI 0x1e
- #define FEIDONE 6
- #define FEISTART 5
- #define AFCDONE 4
- #define AFCAUTOCLEAR 3
- #define AFCAUTOON 2
- #define AFCCLEAR 1
- #define AFCSTART 0
- #define REGAFCMSB 0x1f
- #define REGAFCLSB 0x20
- #define AFC_VALUE(afc_par) (afc_par)∗FSTEP
- #define REGFEIMSB 0x21
- #define REGFEILSB 0x22
- #define FEI_VALUE(fei_par) (fei_par)∗FSTEP
- #define REGRSSICONFIG 0x23
- #define RSSIDONE 1
- #define RSSISTART 0
- #define REGRSSIVALUE 0x24
- #define RSSI_VALUE(rssi_par) (rssi_par)/2
- #define REGDIOMAPPING1 0x25
- #define DIO0MAP0 0x00
- #define DIO0MAP1 0x40
- #define DIO0MAP2 0x80
- #define DIO0MAP3 0xc0
- #define DIO1MAP0 0x00
- #define DIO1MAP1 0x10
- #define DIO1MAP2 0x20
- #define DIO1MAP3 0x30
- #define DIO2MAP0 0x00
- #define DIO2MAP1 0x04
- #define DIO2MAP2 0x08
- #define DIO2MAP3 0x0c
- #define DIO3MAP0 0x00
- #define DIO3MAP1 0x01
- #define DIO3MAP2 0x02
- #define DIO3MAP3 0x03
- #define REGDIOMAPPING2 0x26
- #define DIO5MAP0 0x00
- #define DIO5MAP1 0x10
- #define DIO5MAP2 0x20
- #define DIO5MAP3 0x30
- #define CLKOUT32M 0x00
- #define CLKOUT16M 0x01
- #define CLKOUT8M 0x02
- #define CLKOUT4M 0x03
- #define CLKOUT2M 0x04
- #define CLKOUT1M 0x05

- #define CLKOUT_RC 0x06
- #define CLKOUT_OFF 0x07
- #define REGIRQFLAGS1 0x27
- #define MODEREADY 7
- #define RXREADY 6
- #define TXREADY 5
- #define PLLLOCK 4
- #define RSSI_I 3
- #define TIMEOUT 2
- #define AUTOMODE 1
- #define SYNCADDRMATCH 0
- #define REGIRQFLAGS2 0x28
- #define FIFOISFULL 7
- #define FIFONOTEMPTY 6
- #define FIFOLEVEL 5
- #define FIFOOVERRUN 4
- #define PACKETSENT 3
- #define PAYLOADREADY 2
- #define CRCOK 1
- #define REGRSSITHRESH 0x29
- #define RSSI_THRESH_CALC(rssi_parr) (rssi_parr)∗2
- #define REGRXTIMEOUT1 0x2a
- #define REGRXTIMEOUT2 0x2b
- #define REGPREAMBLEMSB 0x2c
- #define REGPREAMBLELSB 0x2d
- #define REGSYNCCONFIG 0x2e
- #define SYNCON 7
- #define FIFOFILLCOND 6
- #define SYNCSIZE_CALC(syncsize_par) ((((syncsize_par) - 1) & 0x07) << 3)
- #define SYNC_WORD_ON 0x80
- #define REGSYNCVALUE1 0x2f
- #define REGSYNCVALUE2 0x30
- #define REGSYNCVALUE3 0x31
- #define REGSYNCVALUE4 0x32
- #define REGSYNCVALUE5 0x33
- #define REGSYNCVALUE6 0x34
- #define REGSYNCVALUE7 0x35
- #define REGSYNCVALUE8 0x36
- #define REGPACKETCONFIG1 0x37
- #define PACKETFORMAT 7
- #define ENCODING_OFF 0x00
- #define MANCHESTER_ENC 0x20
- #define DATA_WHITENING 0x40
- #define CRCON 4
- #define CRCAUTOCLEAROFF 3
- #define ADDRESS_OFF 0x00
- #define NODE_ADDRESS_ONLY 0x02
- #define NODE_BROADCAST_ADDR 0X04
- #define REGPAYLOADLENGHT 0x38
- #define REGNODEADRS 0x39
- #define REGBROADCASTADRS 0x3a
- #define REGAUTOMODES 0x3b
- #define REGFIFOTHRES 0x3c
- #define TXSTARTCOND 7
- #define REGPACKETCONFIG2 0x3d

- #define RESTARTRX 2
- #define AUTORXRESTARTON 1
- #define AESON 0
- #define REGAESKEY1 0x3e
- #define REGAESKEY2 0x3f
- #define REGAESKEY3 0x40
- #define REGAESKEY4 0x41
- #define REGAESKEY5 0x42
- #define REGAESKEY6 0x43
- #define REGAESKEY7 0x44
- #define REGAESKEY8 0x45
- #define REGAESKEY9 0x46
- #define REGAESKEY10 0x47
- #define REGAESKEY11 0x48
- #define REGAESKEY12 0x49
- #define REGAESKEY13 0x4a
- #define REGAESKEY14 0x4b
- #define REGAESKEY15 0x4c
- #define REGAESKEY16 0x4d
- #define REGTEMP1 0x4e
- #define TEMPMEASSTART 3
- #define TEMPMEASRUNNING 2
- #define REGTEMP2 0x4f
- #define RETESTLNA 0x58

  test registers
- #define NORMAL_SENS_BOOST_MODE 0x1b
- #define HIGH_SENS_BOOST_MODE 0x2d
- #define REGTESTPA1 0x5a
- #define PA1_NORMAL_RX_MODE 0x55
- #define PA1_13DBM_RX_MODE 0x5d
- #define PA1_PA0_OR_RX 0x55
- #define REGTESTPA2 0x5c
- #define PA2_NORMAL_RX_MODE 0x55
- #define PA2_13DBM_RX_MODE 0x5d
- #define PA2_PA0_OR_RX 0x55
- #define REGTESTDAGC 0x6f
- #define AFC_NORMAL_MODE 0x00
- #define AFC_LOW_BETA_ON 0x20
- #define AFC_LOW_BETA_OFF 0x30
- #define REGTESTAFC 0x71
- #define LOW_BETA_AFC_OFFSET_CALC(afcoff_par) (afcoff_par)∗448

2.3.1

2.3.1.1 #define ADDRESS_OFF 0x00

2.3.1.2 #define AESON 0

2.3.1.3 #define AFC_LOW_BETA_OFF 0x30

2.3.1.4 #define AFC_LOW_BETA_ON 0x20

2.3.1.5 #define AFC_NORMAL_MODE 0x00

2.3.1.6 #define AFC_VALUE(*afc_par*) (afc_par)∗FSTEP

2.3.1.7 #define AFCAUTOCLEAR 3

2.3.1.8 #define AFCAUTOON 2

2.3.1.9 #define AFCCLEAR 1

2.3.1.10 #define AFCDONE 4

2.3.1.11 #define AFCLOWBETAON 5

2.3.1.12 #define AFCSTART 0

2.3.1.13 #define AUTOMODE 1

2.3.1.14 #define AUTORXRESTARTON 1

2.3.1.15 #define BITRATE_CALC(*br_par*) FXOSC/(br_par)

2.3.1.16 #define CLKOUT16M 0x01

2.3.1.17 #define CLKOUT1M 0x05

2.3.1.18 #define CLKOUT2M 0x04

2.3.1.19 #define CLKOUT32M 0x00

2.3.1.20 #define CLKOUT4M 0x03

2.3.1.21 #define CLKOUT8M 0x02

2.3.1.22 #define CLKOUT_OFF 0x07

2.3.1.23 #define CLKOUT_RC 0x06

2.3.1.24 #define CONT_MODE 0x60

2.3.1.25 #define CONT_SYNCH_MODE 0x40

2.3.1.26 #define CRCAUTOCLEAROFF 3

2.3.1.27 #define CRCOK 1

2.3.1.28 #define CRCON 4

2.3.1.29 #define DATA_WHITENING 0x40

2.3.1.30 #define DIO0MAP0 0x00

2.3.1.31 #define DIO0MAP1 0x40

2.3.1.32 #define DIO0MAP2 0x80

2.3.1.33 #define DIO0MAP3 0xc0

2.3.1.34 #define DIO1MAP0 0x00

2.3.1.35 #define DIO1MAP1 0x10

2.3.1.36 #define DIO1MAP2 0x20

2.3.1.37 #define DIO1MAP3 0x30

2.3.1.38 #define DIO2MAP0 0x00

2.3.1.39 #define DIO2MAP1 0x04

2.3.1.40 #define DIO2MAP2 0x08

2.3.1.41 #define DIO2MAP3 0x0c

2.3.1.42 #define DIO3MAP0 0x00

2.3.1.43 #define DIO3MAP1 0x01

2.3.1.44 #define DIO3MAP2 0x02

2.3.1.45 #define DIO3MAP3 0x03

2.3.1.46 #define DIO5MAP0 0x00

2.3.1.47 #define DIO5MAP1 0x10

2.3.1.48 #define DIO5MAP2 0x20

2.3.1.49 #define DIO5MAP3 0x30

2.3.1.50 #define ENCODING_OFF 0x00

2.3.1.51 #define FDEV_CALC(*fdev_par*) (fdev_par)/FSTEP

2.3.1.52 #define FEI_VALUE(*fei_par*) (fei_par)∗FSTEP

2.3.1.53 #define FEIDONE 6

2.3.1.54 #define FEISTART 5

2.3.1.55 #define FIFOFILLCOND 6

2.3.1.56 #define FIFOISFULL 7

2.3.1.57 #define FIFOLEVEL 5

2.3.1.58 #define FIFONOTEMPTY 6

2.3.1.59 #define FIFOOVERRUN 4

2.3.1.60 #define FRF_CALC(*frf_par*) (frf_par)/FSTEP

2.3.1.61 #define FS_MODE 0x08

2.3.1.62 #define GAUSS_BT03 0x03

2.3.1.63 #define GAUSS_BT05 0x02

2.3.1.64 #define GAUSS_BT10 0x01

2.3.1.65 #define HIGH_SENS_BOOST_MODE 0x2d

2.3.1.66 #define LISTENABORT 5

2.3.1.67 #define LISTENCRITERIA 3

2.3.1.68 #define LISTENEND1 0x00

2.3.1.69 #define LISTENEND2 0x02

2.3.1.70 #define LISTENEND3 0x04

2.3.1.71 #define LISTENEND4 0x06

2.3.1.72 #define LISTENIDLE262M 0xc0

2.3.1.73 #define LISTENIDLE4M1 0x80

2.3.1.74 #define LISTENIDLE64U 0x40

2.3.1.75 #define LISTENON 6

2.3.1.76 #define LISTENRX262M 0x30

2.3.1.77 #define LISTENRX4M1 0x20

2.3.1.78 #define LISTENRX64U 0x10

2.3.1.79 #define LNAGAIN_0DB 0x01

2.3.1.80 #define LNAGAIN_12DB 0x03

2.3.1.81 #define LNAGAIN_24DB 0x04

2.3.1.82 #define LNAGAIN_36DB 0x05

2.3.1.83 #define LNAGAIN_48DB 0x06

2.3.1.84 #define LNAGAIN_6DB 0x02

2.3.1.85 #define LNAGAIN_AUTO 0x00

2.3.1.86 #define LNAZIN 7

2.3.1.87 #define LOW_BETA_AFC_OFFSET_CALC(*afcoff_par*) (afcoff_par)∗448

2.3.1.88 #define MANCHESTER_ENC 0x20

2.3.1.89 #define MODEREADY 7

2.3.1.90 #define NO_SHAPING 0x00

2.3.1.91 #define NODE_ADDRESS_ONLY 0x02

2.3.1.92 #define NODE_BROADCAST_ADDR 0X04

2.3.1.93 #define NORMAL_SENS_BOOST_MODE 0x1b

2.3.1.94 #define OCP_CURRENT_CALC(*ocp_param*) 0x0f&(((ocp_param)/5) - 9)

2.3.1.95 #define OCPON 4

2.3.1.96 #define OOKTHRESAVERAGE 0x80

2.3.1.97 #define OOKTHRESFIXED 0x00

2.3.1.98 #define OOKTHRESPEAK 0x40

2.3.1.99 #define OUT_POWER_CALC(*power_par*) 0x1f&(18 + (power_par))

2.3.1.100 #define PA0ON 7

2.3.1.101 #define PA1_13DBM_RX_MODE 0x5d

2.3.1.102 #define PA1_NORMAL_RX_MODE 0x55

2.3.1.103 #define PA1_PA0_OR_RX 0x55

2.3.1.104 #define PA1ON 6

2.3.1.105 #define PA2_13DBM_RX_MODE 0x5d

2.3.1.106 #define PA2_NORMAL_RX_MODE 0x55

2.3.1.107 #define PA2_PA0_OR_RX 0x55

2.3.1.108 #define PA2ON 5

2.3.1.109 #define PACKET_MODE 0x00

2.3.1.110 #define PACKETFORMAT 7

2.3.1.111 #define PACKETSENT 3

2.3.1.112 #define PAYLOADREADY 2

2.3.1.113 #define PLLLOCK 4

2.3.1.114 #define RCCALDONE 6

2.3.1.115 #define RCCALSTART 7

2.3.1.116 #define REGAESKEY1 0x3e

2.3.1.117 #define REGAESKEY10 0x47

2.3.1.118 #define REGAESKEY11 0x48

2.3.1.119 #define REGAESKEY12 0x49

2.3.1.120 #define REGAESKEY13 0x4a

2.3.1.121 #define REGAESKEY14 0x4b

2.3.1.122 #define REGAESKEY15 0x4c

2.3.1.123 #define REGAESKEY16 0x4d

2.3.1.124 #define REGAESKEY2 0x3f

2.3.1.125 #define REGAESKEY3 0x40

2.3.1.126 #define REGAESKEY4 0x41

2.3.1.127 #define REGAESKEY5 0x42

2.3.1.128 #define REGAESKEY6 0x43

2.3.1.129 #define REGAESKEY7 0x44

2.3.1.130 #define REGAESKEY8 0x45

2.3.1.131 #define REGAESKEY9 0x46

2.3.1.132 #define REGAFCBW 0x1a

2.3.1.133 #define REGAFCCTRL 0x0b

2.3.1.134 #define REGAFCFEI 0x1e

2.3.1.135 #define REGAFCLSB 0x20

2.3.1.136 #define REGAFCMSB 0x1f

2.3.1.137 #define REGAUTOMODES 0x3b

2.3.1.138 #define REGBITRATELSB 0x04

2.3.1.139 #define REGBITRATEMSB 0x03

2.3.1.140 #define REGBROADCASTADRS 0x3a

2.3.1.141 #define REGDATAMODUL 0x02

2.3.1.142 #define REGDIOMAPPING1 0x25

2.3.1.143 #define REGDIOMAPPING2 0x26

2.3.1.144 #define REGFDEVLSB 0x06

2.3.1.145 #define REGFDEVMSB 0x05

2.3.1.146 #define REGFEILSB 0x22

2.3.1.147 #define REGFEIMSB 0x21

2.3.1.148 #define REGFIFO 0x00

2.3.1.149 #define REGFIFOTHRES 0x3c

2.3.1.150 #define REGFRFLSB 0x09

2.3.1.151 #define REGFRFMID 0x08

2.3.1.152 #define REGFRFMSB 0x07

2.3.1.153 #define REGIRQFLAGS1 0x27

2.3.1.154 #define REGIRQFLAGS2 0x28

2.3.1.155 #define REGLISTEN1 0x0d

2.3.1.156 #define REGLISTEN2 0x0e

2.3.1.157 #define REGLISTEN3 0x0f

2.3.1.158 #define REGLNA 0x18

2.3.1.159 #define REGNODEADRS 0x39

2.3.1.160 #define REGOCP 0x13

2.3.1.161 #define REGOOKAVG 0x1c

2.3.1.162 #define REGOOKFIX 0x1d

2.3.1.163 #define REGOOKPEAK 0x1b

2.3.1.164 #define REGOPMODE 0x01

2.3.1.165 #define REGOSC1 0x0a

2.3.1.166 #define REGPACKETCONFIG1 0x37

2.3.1.167 #define REGPACKETCONFIG2 0x3d

2.3.1.168 #define REGPALEVEL 0x11

2.3.1.169 #define REGPARAMP 0x12

2.3.1.170 #define REGPAYLOADLENGHT 0x38

2.3.1.171 #define REGPREAMBLELSB 0x2d

2.3.1.172 #define REGPREAMBLEMSB 0x2c

2.3.1.173 #define REGRSSICONFIG 0x23

2.3.1.174 #define REGRSSITHRESH 0x29

2.3.1.175 #define REGRSSIVALUE 0x24

2.3.1.176 #define REGRXBW 0x19

2.3.1.177 #define REGRXTIMEOUT1 0x2a

2.3.1.178 #define REGRXTIMEOUT2 0x2b

2.3.1.179 #define REGSYNCCONFIG 0x2e

2.3.1.180 #define REGSYNCVALUE1 0x2f

2.3.1.181 #define REGSYNCVALUE2 0x30

2.3.1.182 #define REGSYNCVALUE3 0x31

2.3.1.183 #define REGSYNCVALUE4 0x32

2.3.1.184 #define REGSYNCVALUE5 0x33

2.3.1.185 #define REGSYNCVALUE6 0x34

2.3.1.186 #define REGSYNCVALUE7 0x35

2.3.1.187 #define REGSYNCVALUE8 0x36

2.3.1.188 #define REGTEMP1 0x4e

2.3.1.189 #define REGTEMP2 0x4f

2.3.1.190 #define REGTESTAFC 0x71

2.3.1.191 #define REGTESTDAGC 0x6f

2.3.1.192 #define REGTESTPA1 0x5a

2.3.1.193 #define REGTESTPA2 0x5c

2.3.1.194 #define REGVERSION 0x10

2.3.1.195 #define RESTARTRX 2

2.3.1.196 #define RETESTLNA 0x58

test registers

2.3.1.197 #define RSSI_I 3

2.3.1.198 #define RSSI_THRESH_CALC(*rssi_parr*) (rssi_parr)∗2

2.3.1.199 #define RSSI_VALUE(*rssi_par*) (rssi_par)/2

2.3.1.200 #define RSSIDONE 1

2.3.1.201 #define RSSISTART 0

2.3.1.202 #define RX_MODE 0x10

2.3.1.203 #define RXREADY 6

2.3.1.204 #define SEQUENCEROFF 7

2.3.1.205 #define SLEEP_MODE 0x00

2.3.1.206 #define STBY_MODE 0x04

2.3.1.207 #define SYNC_WORD_ON 0x80

2.3.1.208 #define SYNCADDRMATCH 0

2.3.1.209 #define SYNCON 7

2.3.1.210 #define SYNCSIZE_CALC(*syncsize_par*) ((((syncsize_par) - 1) & 0x07) << 3)

2.3.1.211 #define TEMPMEASRUNNING 2

2.3.1.212 #define TEMPMEASSTART 3

2.3.1.213 #define TIMEOUT 2

2.3.1.214 #define TX_MODE 0x0c

2.3.1.215 #define TXREADY 5

2.3.1.216 #define TXSTARTCOND 7

2.4 rfm69_table.h

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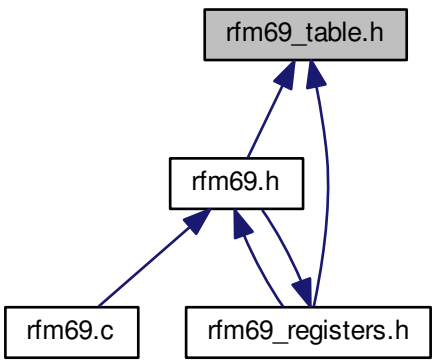

- #define PARAMP 0x00
- #define CUT_OFF_FREQ_M100 CUT_OFF_FREQ∗100
- #define RX_BW_M10 RX_BW∗10
- #define RXBW 0x17
- #define CUT_OFF_FREQ_AFC_M100 CUT_OFF_FREQ_AFC∗100
- #define RX_BW_AFC_M10 RX_BW_AFC∗10
- #define OOK_PEAK_THRESH_STEP_M10 OOK_PEAK_THRESH_STEP∗10
- #define OOK_PEAK_THRESH_DEC_M100 OOK_PEAK_THRESH_DEC∗100
- #define INTERPACKETRXDELAY 0x00

2.4.1

2.4.1.1 #define CUT_OFF_FREQ_AFC_M100 CUT_OFF_FREQ_AFC∗100

2.4.1.2 #define CUT_OFF_FREQ_M100 CUT_OFF_FREQ∗100

2.4.1.3 #define INTERPACKETRXDELAY 0x00

2.4.1.4 #define OOK_PEAK_THRESH_DEC_M100 OOK_PEAK_THRESH_DEC∗100

2.4.1.5 #define OOK_PEAK_THRESH_STEP_M10 OOK_PEAK_THRESH_STEP∗10

2.4.1.6 #define PARAMP 0x00

2.4.1.7 #define RX_BW_AFC_M10 RX_BW_AFC∗10

2.4.1.8 #define RX_BW_M10 RX_BW∗10

2.4.1.9 #define RXBW 0x17