DIGITAL SYSTEM DESIGN

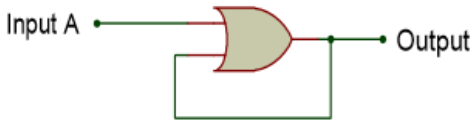
1.1 Introduction:

The sequential logic studies digital circuits which functions in such a way that their outputs logic states depend not only on the logical combination of their inputs states, but also on the memory of the circuit. In fact, at a given instant, sequential circuits always store the status of their output and that status cannot change unless new logic signals are sent to its inputs: this is the memory effect. The simplest sequential logic circuit is the latch which is a circuit capable of storing one bit of information. It has two outputs, one being the reverse of the other. A flip-flop is an edge triggered latch; it means that it cannot function unless the right signal edge (either rising or falling edge) is available at its clock input. This chapter is an

introduction to sequential logic; it is focused on the study of latches and flip-flops which are tools used in the designing of sequential circuits.

1.2 Multivibrators

Let us consider the following circuit:



According to the functioning of the OR gate, if A = 1, the output must be 1. However, if A is in low logic state, we cannot guarantee the logic state of the output. Since the output feeds back to one of the OR gate inputs, this circuit will “latch” (That is to remain unchanged) in the 1 output state after any time that A is 1. In fact, when A = 0, the output could be 0 or 1 depending on the circuit previous state. So the output maintains (or memorises) its last state when A is 0. The truth table of our circuit can be given as follow.

Input A	Output
0	latch
1	1

Any circuit employing feed back is called multivibrator. A bistable multivibrator can hold stable in one of two possible states (either 0 or 1). Monostable multivibrator holds stable only in one output state, the other state being momentary. Astable multivibrator has no stable state. It oscillates back and forth between an output of 0 and 1. One of the most common multivibrators is the integrated circuit NE555, which can work as well as monostable or astable.

1.2.1 Latches:

Many latches exist, but their common characteristic is that they can store one bit of information.

1.2.1.1 The S-R latch:

The S-R latch is a bistable multivibrator having two stable states: Set and Reset. So S-R latch means Set-Reset latch. To create an S-R latch, can wire two NOR gates in such a way that the output of one feeds back the input of another, and vice versa.

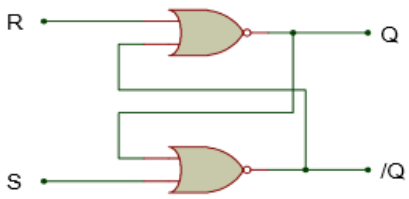


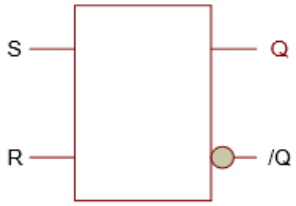
Figure 1.1: Principle diagram of an S-R latch

Truth table:

S	R	Q	/Q
0	0	Latch	
0	1	0	1
1	0	1	0
1	1	invalid	

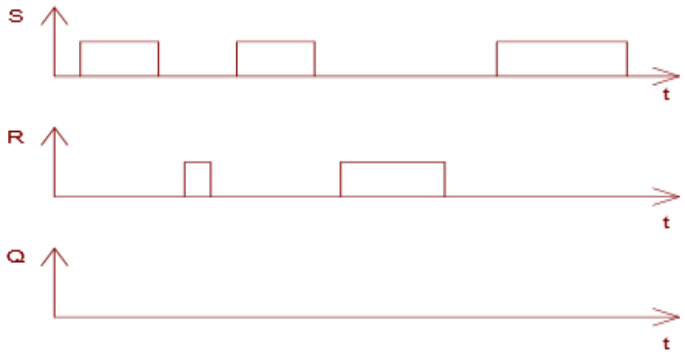
- The outputs Q and /Q should always be in opposite logic states.
- Making both S and R inputs equal to 1 results in both Q and /Q being 0: this is why this inputs combination is forbidden, it produces an invalid or illegal state.
- Making S = 1 and R = 0 sets the multivibrator so that Q = 1 and /Q = 0.
- Making R = 1 and S = 0 resets the multivibrator so that /Q = 1 and Q = 0.
- When R = 0 and S = 0 the multivibrator outputs lath in their previous states.

Circuit diagram:

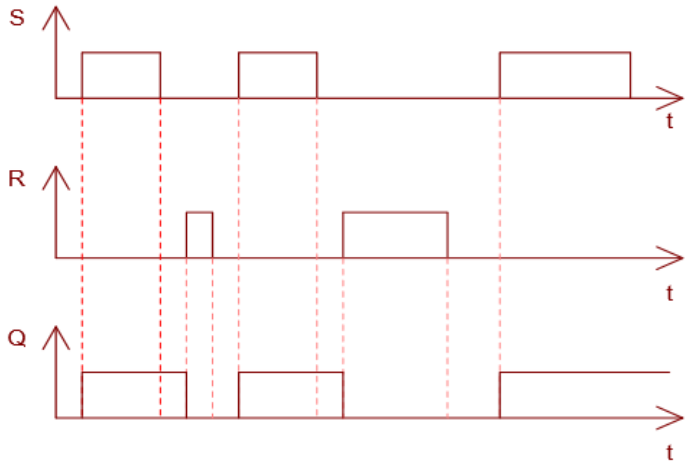


Exercise 1.1:

The following waveforms are applied at the inputs of an S-R latch. Deduce the waveform of the output assuming that the initial state of the output is Q = 0.



The waveforms of the output Q of the exercise above can be given as follows:



1.2.1.2 The gated S-R latch:

The gated S-R latch has an enable input E which must be activated in order to allow the latch to take into consideration the combinations available at its inputs. The latch would not function properly unless the right logic level is sent to the input E. The principle diagram of a gated S-R latch is given bellow.

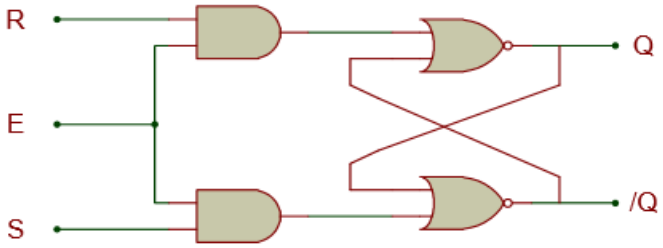


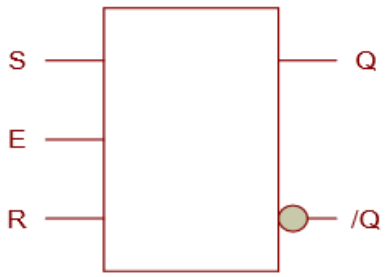
Figure 1.2: Principle diagram of a gated S-R latch.

Truth table:

E	S	R	Q	/Q
0	X	X	Latch	
1	0	0	Latch	
1	0	1	0	1
1	1	0	1	0
1	1	1	Invalid	

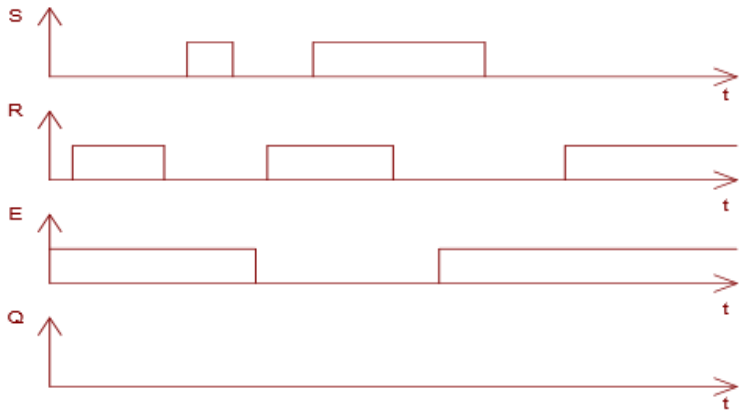
When E = 0, the outputs of the two AND gates are forced to 0, regardless of the states of either S or R. The previous states of the outputs are therefore memorised. Only when the enable input is activated (by sending a 1 to it) will the latch respond to the S an R inputs.

Circuit diagram:



Exercise 1.2:

The following waveforms are applied at the inputs of a gated S-R latch. Deduce the waveform of the output assuming that the initial state of the output is Q = 0.



The waveform of the output Q of the exercise 7.2 above can be given as follows: