7.2.2.2 S-R Flip-flop:

An S-R flip flop is an edge triggered S-R latch. A pulse detector is connected to its enable input in order to detect rising or falling edges of the clock signal. The principle diagram is as follows.

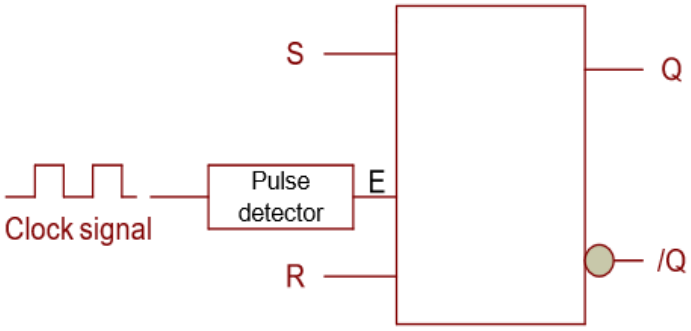


Figure 1.5: Principle diagram of an S-R flip-flop.

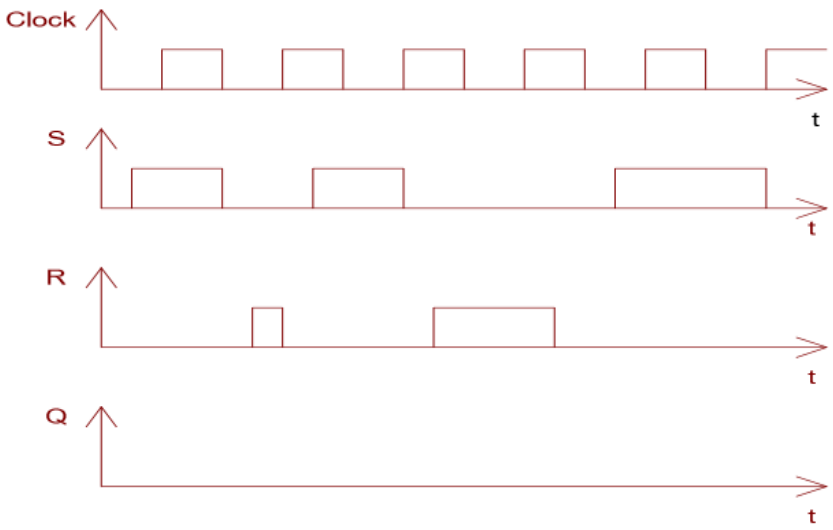
Truth table:

Clock	S	R	Q	/Q
↓	X	X	Latch	
↑	0	0	Latch	
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	Invalid	

Only when the clock signal is transitioning from low to high is the circuit responsive to the S and R inputs. For any other condition of the clock signal, the circuit will be latched.

Exercise 1.5:

The following waveforms are applied at the inputs of an S-R flip-flop. Determine that of the output Q assuming that it is initially at low logic state.



1.2.2.3 The J-K flip-flop:

The J-K flip flop is a modified version of an S-R flip-flop with no invalid output state. When J = 1 and K = 1,and the clock input is pulsed, instead of an invalid state at the output, the circuit will toggle to a state opposite of that was previously available at its output: if the output was previously 1, it toggles to 0 and vice versa. The principle diagram of a J-K flip-flop is given as follows:

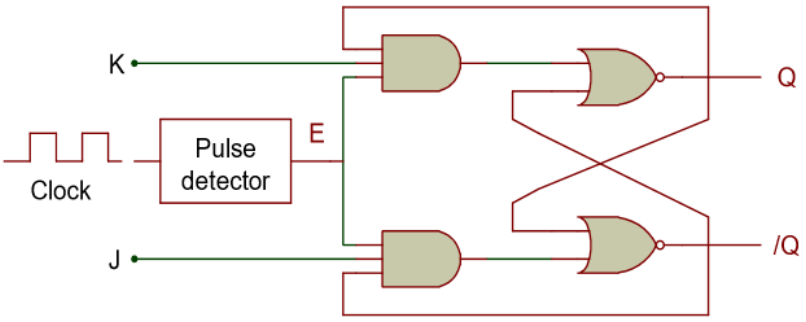


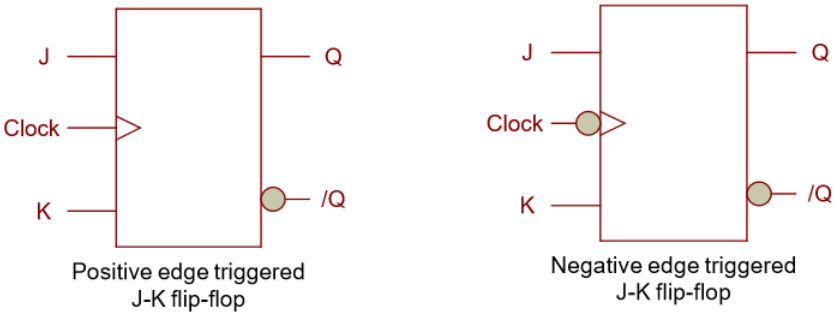
Figure 1.6: Principle diagram of a J-K flip-flop.

What used to be S and R inputs are now J and K inputs respectively. The previous two inputs AND gates have been replaced by three inputs AND gates. The third input of each gate receives feedback from Q and /Q outputs.

Truth table:

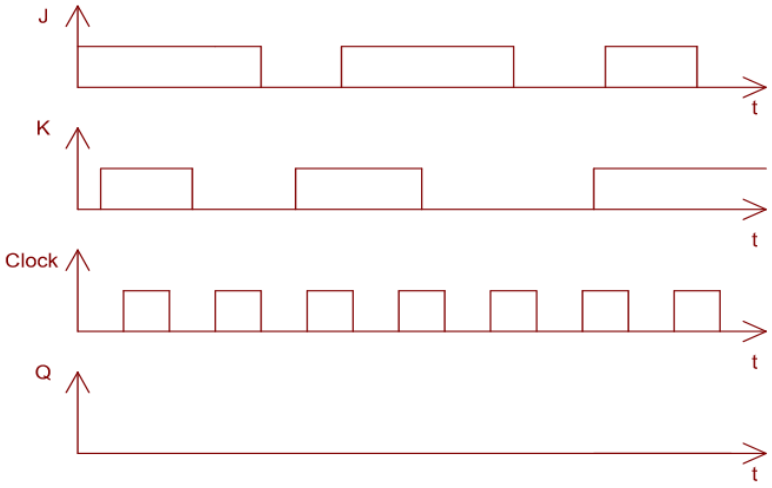
Clock	J	K	Q	/Q
↓	X	X	Latch	
↑	0	0	Latch	
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	Toggle	

Circuit diagram:

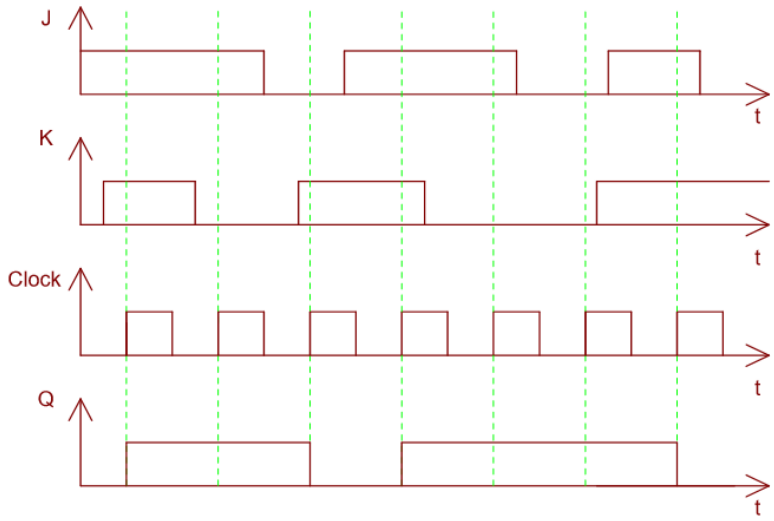


Exercise 1.6:

The following waveforms are applied at the inputs of a positive edge triggered J-K flip-flop. Determine that of the output Q assuming that it is initially at low logic state.

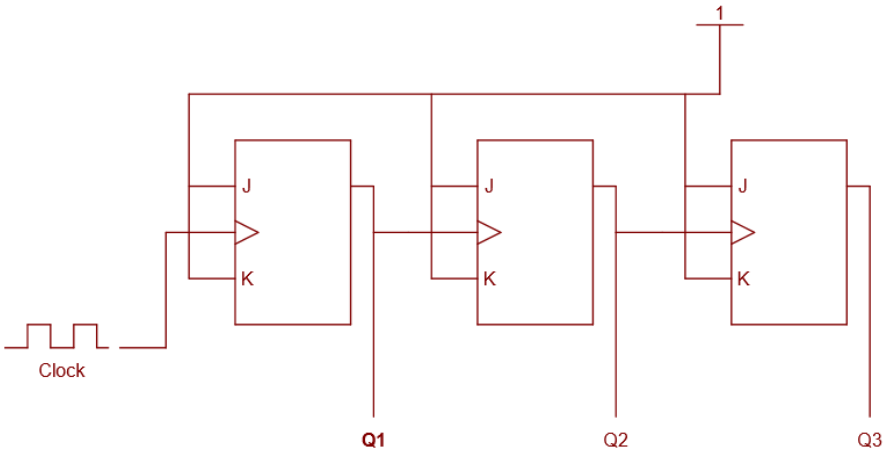


The waveform of the output Q of the exercise 7.6 above can be given as follows:



Exercise 1.7:

Let us consider the following digital system:



1.2.3 Asynchronous flip-flop's inputs:

The normal data inputs to a flip-flop (D, S and R or J and K) are referred to as synchronous inputs because they have effect on the outputs (Q and /Q) only in synchronism with the clock signal transitions. Asynchronous inputs are some types of extra inputs which can set or reset the flip-flop regardless of the status of the clock signal. Typically, they are called PRESET and CLEAR.

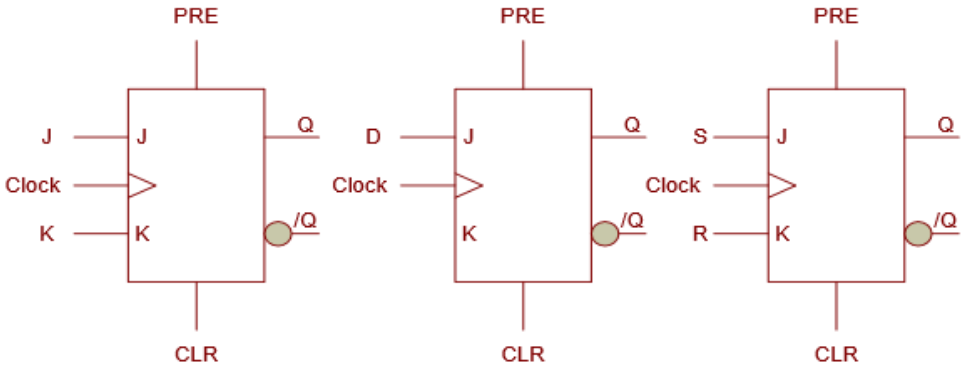


Figure 1.7: Asynchronous flip-flop's inputs.

When the preset input is activated, the flip-flop will be set (Q = 1, /Q = 0) regardless of the status of any of the synchronous inputs or the clock. When the clear input is activated, the flip-flop will be reset (Q = 0, /Q = 1) regardless of the status of any of the synchronous inputs or the clock. If both preset and clear inputs are activated, we have an invalid state on the outputs where Q and /Q go to the same state. Preset and clear inputs find their use in the designing of counters (asynchronous and synchronous). Asynchronous inputs, just like synchronous inputs can be engineered to be active high or active low. If they are active low, there will be an inverting bubble at that input lead on the block symbol.

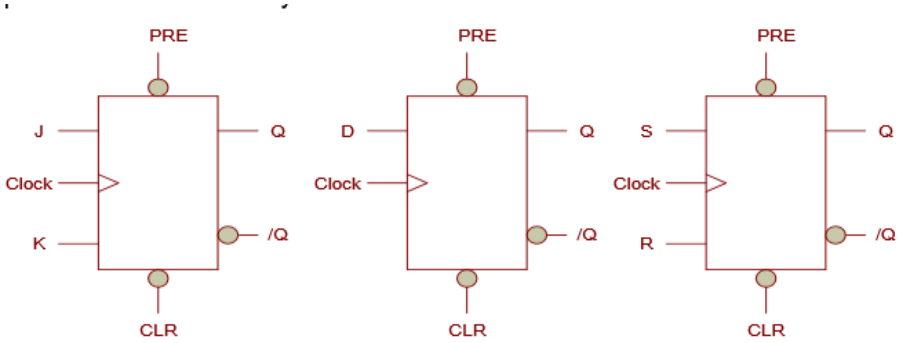


Figure 1.8: Asynchronous inputs active low.