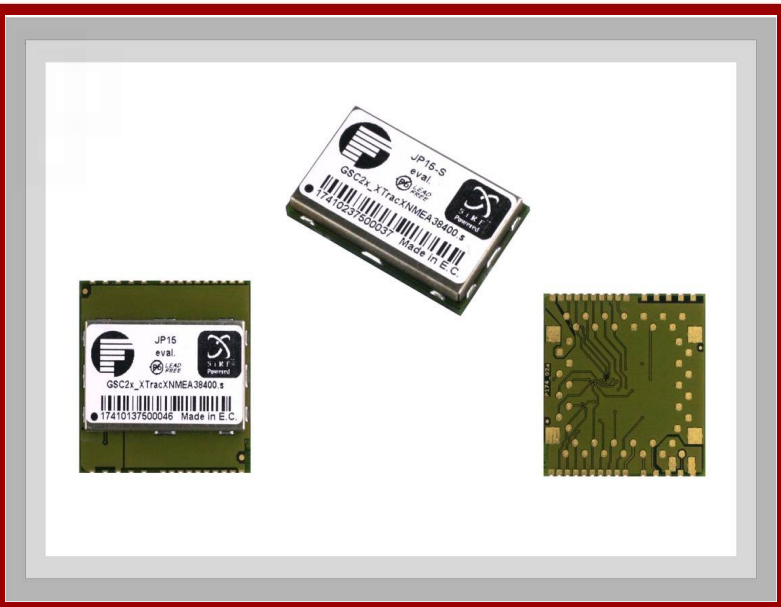
FALCOM
WIRELESS COMMUNICATIONS GMBH

JP15 Family

JP15-T, JP15-B & JP15-S GPS-Receivers

Pb LEAD FREE Lead-free products

Hardware description



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VERSION HISTORY

Version number	Author	Changes	Release date
1.0.0	F. Beqiri	- Initial version	15/11/2005
1.0.1	F. Beqiri	- Throughout this document, the description of the DATA0, 15, 2 and 3 lines revised (each line has an internal 100 kΩ pull-up resistor instead of no internal pull up resistors in the prior document version)	18/11/2005
1.0.2	F. Beqiri	- Figure 4 replaced by a new one, see chapter 6.1, page 19.	15/12/2005
1.0.3	F. Beqiri	- The ordering name JP15 has been replaced by JP15-T. - The ordering name JP15-X has been replaced by JP15-T-X. - The JP15-ROM receiver has been completely removed from the ordering list with the standard options (only the JP15-B-ROM and JP15-S-ROM versions remain available).	12/01/2005
1.0.4	F. Beqiri	- Added Figure 9 - with hint JP15-T is compatible with JP7-T in PCB layout. - Throughout this manual changed the output configuration code for ROM-based modules - *see table 13 in chapter 7.2.1*. - Added APM Mode (for XTracX2.2.0 software only - see chapter 5.5 page 17) - Changed input messages for ATP and PTF modes – see chapter 5.4 page 15.	27/06/2006
1.0.5	F. Beqiri	- Changed name and description of **PIN 3** and **PIN 27** on Table 6 page **19** (**DATA0** (PIN 3) and **DATA15** (PIN 27) changed to **BOOT_SELECT** and **GPIO0** respectively)	12/07/2006
1.0.6	F. Beqiri	- Corrected **Configuration 5** – UART B not supported by the **XTracX2.2.0** software – see chapter 7.2.1 page 27. - Changed **Configuration 6** – UART B supports RTCM 9600 instead of SiRF binary 38400 – see chapter 7.2.1 page 27.	21/11/2006
1.0.7	F. Beqiri	- Updated soldering profile – see Figure 13, page 36 and read the note below.	02/03/2007
1.0.8	F. Beqiri	- JP15 modules can accept only one reflow process.	25/09/2007

Cautions

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Please, read carefully the safety precautions.

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1 INTRODUCTION

1.1 General

This description is focussed on the GPS receiver of the FALCOM JP15 family series from FALCOM GmbH.

The JP15 family is an excellent device designed for a wide variety of system solutions and offers an easy integration in various ways on the user application platform. Units of the JP15 family based on a 0.13 micron CMOS process of the SiRFstarIIx – GSC2x – architecture are single-board solutions with 12 parallel channel receiver, which offers SiRFstarII class performance. The GSC2x is an integrated GPS baseband, RF, 4 Mbit ROM and 1 Mbit SRAM for GPS navigation in a single solution.

The JP15 family is a GPS Single board receiver based on SiRFstarII architecture with both ROM and Flash variant. The JP15 family features two operating modes – a ROM operating mode, and a Flash-operating mode. The ROM operating mode supports four different user-selectable configurations. These configurations feature various popular protocols, baud-rates, and output schemes designed to give GPS status via LED's. This makes the software more usable to a larger cross-section of GPS customers. The Flash memory is also pre-loaded with either the high sensitivity solution XTracX2.2.0 or GSW2.4.0 standard software. Based on the power up hardware configuration, the JP15 family will run from either its ROM based configuration or Flash. Table **13**, in chapter 7.2.1 represents an overview of the different output configuration options supported by the ROM and FLASH based software.

The JP15 family is designed for location applications requiring strong outdoor performance and simplified integration. The full power operation is also dramatically reduced from 220 mW on the JP7-T family (based on the SiRFstarIIe/LP) to 100 mW on the JP15 family (based on the SiRFstarIIx) and TricklePower is reduced from 80 mW to 30 mW. JP15 family GPS receivers can be used to deliver real-time location and navigation capabilities in a simpler, smaller design with extended battery life.

The JP15 family delivers major advancements in GPS performance, accuracy, integration, computing power and flexibility.

The JP15 family consists of two members - the JP15-T, JP15-B and JP15-S. These products have identical electrical and RF-performance, however, offers different sizes, pin-out and mounting features to the target application platform. All GPS units introduce new generation of hardware and software of the SiRFstarII class performance.

These single board solutions are offered as 30-pin (25.5 mm x 25.5 mm) edge contacts, 52-pin (25.5 mm x 25.5 mm) and 50-pin (25.5 mm x 16.0 mm) BGA.

Compared to the JP15-T and JP15-B, the JP15-S is optimized for location applications requiring high performance in a very small form factor - ideal for devices with limited onboard processing power. The single board solution is offered as a 50-pin (25.5 mm x 16.0 mm) BGA.

The JP15 family concept builds perfect basis for the design of high-sensitive, low-power, compact and cost efficient state-of-the-art GPS enabled system solutions for target platforms such as mobile phones, automotive systems, portable computing devices, and embedded consumer devices. The FALCOM JP15 family is also designed to be entire products such as AVL tracking units, handheld GPS.

The internal software completes the package providing flexible system architecture for standalone GPS based products.

1.2 Order options

Before you start up the receiver, make sure that your package includes the following items. If any item is missing or damaged, please contact your vendor immediately. According to your requirements you can choose the desired unit.

Figure 1: The FALCOM JP15 (left) and JP15-B (right) GPS receivers (top and bottom views)

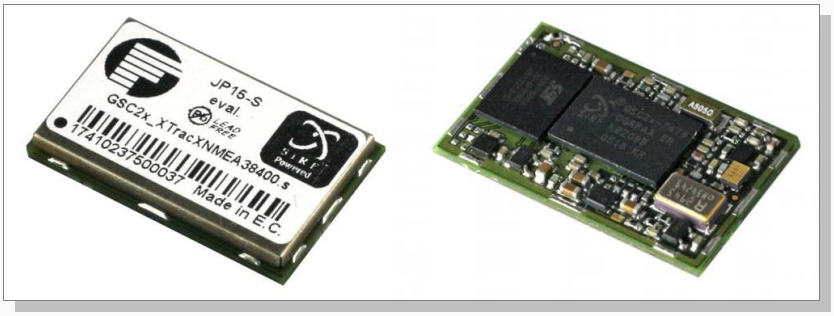


Figure 2: The FALCOM JP15-S GPS receiver (top view; with and without shielding)

The table below contains the order options of JP15 family.

Ordering Name	Options	Sizes	Running software
JP15-T (Versions)			
JP15-T	30-pin (edge contacts) package	25.5mm x 25.5mm x 3mm	GSW2.4.0 software with Configuration 6 (FLASH based)
JP15-TX			XTracX2.2.0 software with Configuration 5 (FLASH based)
JP15-B (Versions)			
JP15-B	48-pin BGA package	25.5mm x 25.5mm x 3mm	Up to 4 configuration (ROM based) **&** GSW2.4.0 software with Configuration 6 (FLASH based)
JP15-B-ROM			Up to 4 configuration (ROM based, only)
JP15-BX			Up to 4 configuration (ROM based) **&** XTracX2.2.0 software with Configuration 5 (FLASH based)
JP15-S (Versions)			
JP15-S	52-pin BGA package	25.5mm x 16.0mm x 3mm	Up to 4 configuration (ROM based) **&** GSW2.4.0 software with Configuration 6 (FLASH based)
JP15-S-ROM			Up to 4 configuration (ROM based, only)
JP15-SX			Up to 4 configuration (ROM based) **&** XTracX2.2.0 software with Configuration 5 (FLASH based)

Table 1: Ordering options

Users are advised to proceed quickly to the chapter "Security" and read the hints carefully to secure its optimal use.

1.3 Used abbreviations

Abbreviation	Description
BGA	Ball Grid Array
DGPS	Differential GPS
DOP	Dilution of Precision
GPS	Global Positioning System
GGA	GPS Fixed Data
LNA	Low Noise Amplifier
NMEA	National Maritime Electronics Association
PRN	Pseudo - Random Noise Number – The Identity of GPS satellites
RF	Radio Frequency
RP	Receive Protocol
RTC	Real Time Clock
RTCM	Radio Technical Commission for Maritime Services
SDI	Data input
SDO	Data output
SA	Selective Availability
SSTE	Satellite Signal Tracking Engine
WAAS	Wide Area Augmentation System
MSK	Minimum Shift Keying
PCB	Printed Circuit Board
PRN	Pseudo-random noise
IF	Intermediate Frequency
A/D	Analog/Digital

Table 2: Abbreviations

1.4 Related documents

1) SiRF binary and NMEA protocol specification;
   www.falcom.de | Support | Download | Documentation | Sirf | SiRFmessages.zip
2) SiRF-demo software and manual;
   www.falcom.de | Support | Download | Documentation | Sirf | SiRFdemo.pdf
   www.falcom.de | Support | Download | Software & Tools | Sirf | SiRFdemo.zip

2 SECURITY

This chapter contains important information for the safe and reliable use of the GPS receiver. Please, read this chapter carefully before starting to use the GPS receiver.

2.1 General information

The Global Positioning System uses satellite navigation, an entirely new concept in navigation. GPS has become established in many areas, for example, in civil aviation or deep-sea shipping. It is making deep inroads in vehicle manufacturing and before long every one of us will use it this way or another.

The GPS system is operated by the government of the United States of America, which also has sole responsibility for the accuracy and maintenance of the system. The system is constantly being improved and may entail modifications effecting the accuracy and performance of the GPS equipment.

2.2 Restricted use

Certain restrictions on the use of the GPS receiver may have to be observed on board a plane, in hospitals, public places or government institutions, laboratories etc. Follow these instructions.

2.3 Children

Do not allow children to play with the GPS receiver. It is not a toy and children could hurt themselves or others. The GPS receiver consists of many small parts, which can come loose and could be swallowed by small children. Thoughtless handling can damage the GPS receiver.

2.4 Operation/antenna

Operate the GPS receiver with an antenna connected to it and with no obstruction between the receiver and the satellite.

Make absolutely sure that the antenna socket or antenna cable is not shorted as this would render the GPS receiver disfunctional.

Do not use the receiver with a damaged antenna. Replace a damaged antenna without delay. Use only a manufacturer-approved antenna. Use only the supplied or an approved antenna with your GPS receiver. Antennas from other manufacturers, which are not authorized by the supplier, can damage the GPS receiver.

Technical modifications and additions may contravene local radio-frequency emission regulations or invalidate the type approval.

Authorized GPS antennas: FAL-ANT-3 (active antenna)

2.5 Electrostatic Discharge (ESD)

The JP15/-S GPS receivers contain class 1 devices. The following Electrostatic Discharge (ESD) precautions are recommended:

-Protective outer garments.

-Handle device in ESD safeguarded work area.

-Transport device in ESD shielded containers.

-Monitor and test all ESD protection equipment.

-Treat the JP15/-S GPS receivers as extremely sensitive to ESD.

3 SAFETY STANDARDS

The GPS receiver meets the safety standards for RF receivers and the standards and recommendations for the protection of public exposure to RF electromagnetic energy established by government bodies and professional organizations, such as directives of the European Community, Directorate General V in matters of radio frequency electromagnetic energy.

4 TECHNICAL DATA

4.1 FEATURES

-OEM single board 12 channel GPS receiver

-Size:	JP15-T/-B : 25.5 x 25.5 x 3.0 mm (B x L x H) JP15-S : 25.5 x 16.0 x 3.0 mm (B x L x H)
-Weight:	JP15-T/-B : 2.8 g JP15-S : 1.8 g
-Casing:	Fully shielded
-TCXO:	± 0.5 ppm
-Memory:	8 Mbit FLASH, on-chip 4 Mbit ROM and 1 Mbit SRAM.
-Operating voltage:	+3 to 3.3 V DC
-Power consumption:	120 mW @ 3.3 V (continuous mode) 100 mW @ 3.0 V (continuous mode)
-Power management:	Adaptive Trickle-Power™ (ATP)* Push-to-Fix (PTF)* Advanced Power Management (APM)*
-Temperature range: storage).	-40 to +85 °C (operation, transportation and
-Protocols: 7.2.1)	SDI1/ SDO1 (See table 13 [UART A] in chapter SDI2/ SDO2 (See table 13 [UART B] in chapter 7.2.1)

* For more details see chapter 5.4 page 15 and chapter 5.5 page 17.

5 TECHNICAL DESCRIPTION

5.1 Receiver Architecture

The JP15-T/-S OEM GPS receivers from FALCOM are new OEM GPS receiver products that feature the SiRFstarIIx single chipset. The core of JP15-T/-S units is comprised of the GSC2x single chip, which consists of two key sections. The first is a GPS and SBAS (WAAS and EGNOS) DSP that connects directly to the RF. This DSP correlates the incoming signals with locally generated codes. Wide parallel search architecture enables simultaneous search of 1920 time/frequency bins. The second section is the Satellite Signal Tracking Engine (SSTE). The SSTE handles all high-rate interrupts and feeds back tracking control to all 12 channels. After initialization from the navigation code, the SSTE handles acquisition, tracking, and reacquisition tasks autonomously. The SSTE also contains a built-in data demodulator for GPS and SBAS signal structures.

The JP15 family is an integrated GPS baseband, RF, ROM and FALSH in a single package. Two types of GPS software are available for the JP15 family– GSW2.4.0 and XTracX2.2.0. By default, the JP15 family is loaded with upto 4 configurations (ROM based software) and with GSW2.4.0 or XTracX2.2.0 (Flash based software).

The JP15 family will start running based on the power up configuration. Based on your power up configuration, the JP15 family will run from either its ROM based configuration or Flash memory. The Internal Program Code resides on 4Mb of ROM embedded in the chip. The ROM supports four different user-selectable configurations. This GSW2.4.0 code supports many of the same features as Flash based software. ROM cannot be modified to support custom user code. The JP15 family will also run from the Flash memory. This allows customers to use internal ROM for standard products and Flash for customized products. The JP15 family achieves overall low power and good performance by using a 0.13um CMOS process for the baseband and a 0.35um BiCMOS SiGe process for the RF section.

The JP15 family is designed for location applications requiring strong outdoor performance and simplified integration. The JP15 family contains a small block of battery-backed SRAM, which contains all necessary GPS information for hot starts and a small amount for user configuration variables. The on-chip 1-Mbit SRAM size (32Kx32) memory can be used for either instructions or data. The SRAM is designed for a combination of low power and high speed, and can support single cycle read for all bus speeds. In many applications, the 8 Mbit FLASH completely eliminates the need for external data memory. Figure 3 below shows the block diagram of the JP15-T/-S architecture.

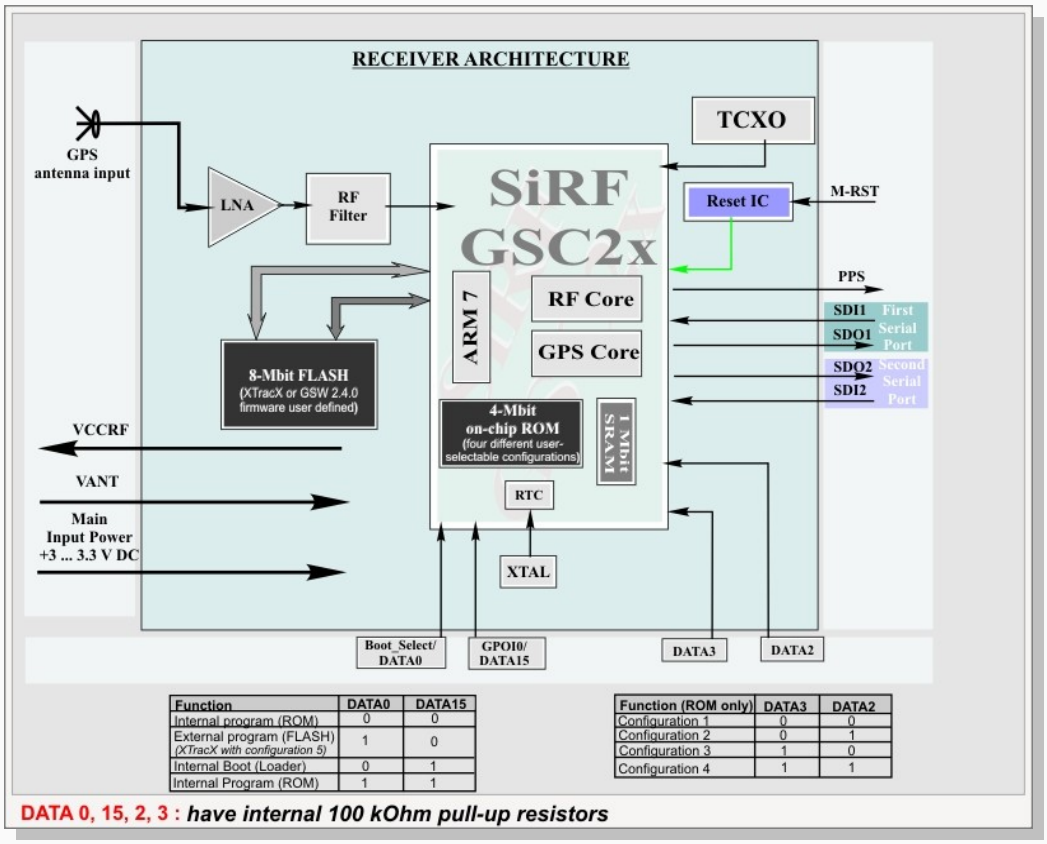


Figure 3: Architecture of the JP15-T/-B/-S GPS receivers.

5.2 Technical specifications

5.2.1 Electrical Characteristics

5.2.1.1 General

Frequency	L1, 1575.42 MHz
C/A code	1.023 MHz chip rate
Channels	12
Max. update rate	1 Hz
Processor speed	6, 12.5, 25 and 49 MHz
Data bus	16 bit

5.2.1.2 Accuracy

Position	Autonomous: 10 meters CEP without SA
	SBAS: < 5 meter
Velocity	0.1 meters/second, without SA
Time	1 microsecond synchronized to GPS time

5.2.1.3 DGPS Accuracy

Position	1 to 5 meters, typical

Velocity	0.05 meters/second, typical

5.2.1.4Datum

WGS-84

5.2.1.5Time to First Position

Snap start	< 3 sec., average
Hot start	< 8 sec., average
Warm start	< 35 sec., average
Cold start	< 45 sec., average

5.2.1.6Sensitivity

Running Software	**XTracX2.2.0**	**GSW2.4.0**
Hot Start	23 dBHz	28 dBHz
Warm Start	28 dBHz	30 dBHz
Cold Start	32 dBHz	32 dBHz
Tracking	16 dBHz	26 dBHz

5.2.1.7Dynamic Conditions

Altitude	18,000 meters (60,000 feet) max.
Velocity	<515 meters/second (1000 knots) max.
Acceleration	4 g, max.
Jerk	20 meters/second³, max.

5.2.1.8DC Power (Average power consumption)

Main power	+ 3 to 3.3 V DC
Continuous mode	35 mA @ 3.3 V DC; 33 mA @ 3 V DC
Backup battery power	+3 V DC ±5%

5.2.1.9Serial Port

Electrical interface	full duplex serial communication, CMOS level.

Protocol messages	Depends on the configuration of the software already running.
	- SiRF binary and NMEA-0183.
	  - SiRF binary – position, velocity, altitude, status. (See also table **13**, in chapter 7.2.1)
	  - Control NMEA – GGA, GLL, GSA, GSV, RMC, VTG. (See also table **13**, in chapter 7.2.1)

5.2.1.10Time – 1PPS Pulse

Level	CMOS
Pulse duration	100 ms
Time reference	At the pulse positive edge
Measurements	Aligned to GPS second, ± microsecond

5.3 Product applications

-Handheld GPS receiver applications

-Automotive applications

-Marine navigation applications

-Aviation applications

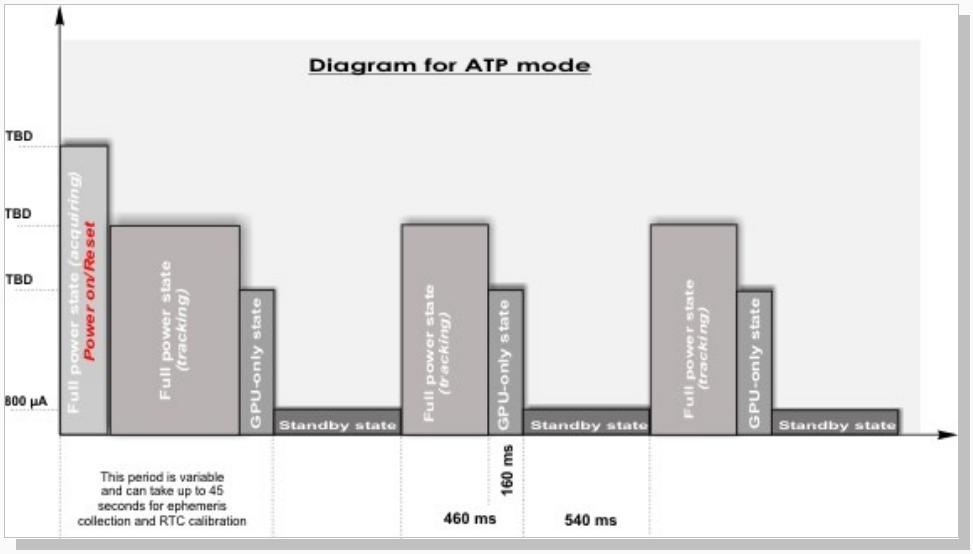
-Timing applications

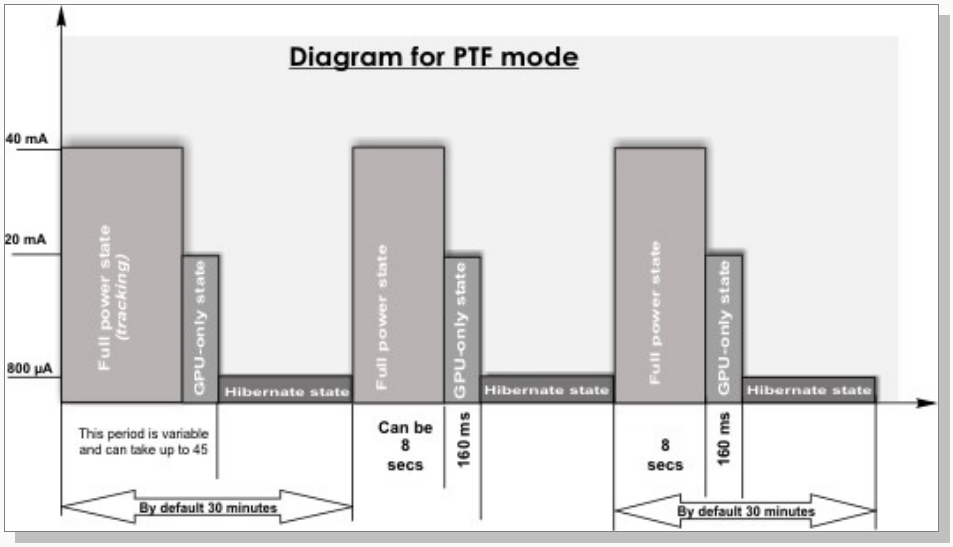
5.4 NMEA input message for ATP & PTF Mode

The input message below sets the FALCOM JP15 family operating with XTracX2.2.0 or GSW2.4.0 software into the (**Adaptive***) **TricklePower**, **Push-To-Fix Mode** or back to **Continuous** Mode. Details about the configuration are given below.

***** ***Adaptive Trickle Power***

When Adaptive TricklePower is enabled, the receiver will maximize the navigation performance while running TricklePower. Under normal tracking conditions, Adaptive TricklePower performs the same as TricklePower, but in harsh tracking environments the receiver automatically switches to Full Power mode to improve navigation performance. When tracking conditions return to normal (four or more satellite signals with C/No of 36 dB or higher), the receiver switches back to TricklePower. This has the effect of improving navigation results in harsh GPS environments at the cost of using more power.





The receiver accepts the input message with following format:

Syntax	$PSRF107,<Mode>,<OnTimeMs*>,<LPInterval*>,<MaxAcqTimeMs>,<MaxOffTimeMs>,<TPAdaptive><*CS><CR><LF>
Examples	$PSRF107,1,400,2000,60000,60000,1*17<CR><LF> $PSRF107,2,400,60000,60000,60000,0*21<CR><LF> $PSRF107,0,0,0,0,0,0*21<CR><LF>

Parameter Description

<Mode>

It defines the mode to be performed. It can be set to:

0 Sets the target receiver back to the Continuous mode (full power).

1 Sets the target receiver into the Adaptive TricklePower (TP) mode.

2 Sets the target receiver into the Push-To-Fix (PTF) mode.

<OnTimeMs*>

It defines the OnTime period in milliseconds the receiver will stay in full power state until a position solution is made and estimated to be reliable. Please note that, in harsh tracking environments the receiver automatically switches to full power state to improve navigation performance even if the defined OnTime has been expired. When the satellites are sorted according their signal strength, the fourth satellite determines if the transition to Standby mode/hibernate state will occur or not. It can be set to a value between:

200 ... **900** OnTime period in milliseconds

<LPInterval*>

It defines the complete interval of time in milliseconds the receiver will stay in full power and Standby mode/hibernate state.

It can be set to a value between:

1000 ... **10000** The interval of time in milliseconds intended for Adaptive TricklePower (ATP) mode.

10000 ... **7200000** The interval of time in milliseconds intended for Push-To-Fix (PTF) mode.

<MaxAcqTimeMs>

It specifies the Maximum Acquire Time in milliseconds how long the target receiver should attempt to acquire satellites and navigate. If this time elapses and no GPS-fix is obtained, the target receiver is set into the sleep mode for up to *MaxOffTime* in ms. It means, the target receiver searches for *MaxAcqTime* in ms, sleeps for *MaxOffTime* in ms, searches again for *MaxAcqTime* in ms, etc. It can be set to a value between:

1000 ... No Limit

<MaxOffTimeMs>

It specifies the Maximum Off Time in milliseconds how long the target receiver should remain off (sleep mode) before making another attempt to navigate. This mode is enabled, if the target receiver is turned on and acquires satellites, but does not navigate. This mode is disabled, if the target receiver is turned on, acquires and navigates. It can be set to a value between:

1000 .. 1800000

<TPAdaptive>

It enables/disables the Adaptive TricklePower (ATP) mode if the value of the <Mode> parameter is set to **1**, otherwise it does not have any effect. It can be set to:

0	Disables the Adaptive TricklePower (ATP) mode.
1	Enables the Adaptive TricklePower (ATP) mode.

<*CS>

CHECKSUM is a two-hex character as defined in the NMEA specification. Use of checksums is required on all input messages. For more detailed information, refer to the chapter 7.3.2.2 page 29.

<CR><LF>

Each message is terminated using Carriage Return (CR) Line Feed (LF), which is hex 0D 0A. Because 0D 0A are not printable ASCII characters, they are omitted from the example strings, but must be sent to terminate the message and cause the receiver to process that input message.

5.5 NMEA input message for APM Mode (XTracX2.2.0 only)

The FALCOM JP15 family operating with XTracX2.2.0 software can also be set into the **Advanced Power Management** (APM) Mode. Details about the configuration are given below.

The receiver accepts the input message with following format:

Syntax	$PSRF107,<*APM_ENABLED*>,<*Num_Fixes*>,<*TIME_BTW_FIXES*>,<*HORI_ERR_MAX*>,<*VERT_ERR_MAX*>,<*RESP_TIME_MAX*>,<*TIME_ACC_PRIORITY*>,<*POWER_DUTY_CYCLE*>,<*TIME_DUTY_CYCLE*><*CS><CRLF>
Examples	$PSRF107,3,0,30,6,6,0,0,50,0*17<CR><LF> $PSRF107,0,0,0,0,0,0,0,0,0*21<CR><LF>

Parameter Description

Parameter Name	Example	Units	Description
APM_ENABLED	3		APM Disable/Enable flag. **0**= Disable APM; **3** = Enable APM

Num Fixes	0		Number of requested APM cycles. May have one or more fix per cycle. Range from **0** to **255**
TIME_BTW_FIXES	30	Seconds	Time between requested fixes. Range from **10** to **180**.
HORI_ERR_MAX	See Table below		Maximum requested horizontal error. GPS shall try to provide a position with horizontal error less than this specified value in 95% of the cases.
VERT_ERR_MAX	See Table below		Maximum requested vertical error. GPS shall try to provide a position with vertical error less than this specified value in 95% of the cases.
RESP_TIME_MAX	0	Seconds	Maximum response time. GPS shall try to provide a position within the specified time.
TIME_ACC_PRIORITY	0		It can be set to 0 .. 2. **0** = No priority imposed. **1** = RESP_TIME_MAX has higher priority. **2** = HORI_ERR_ MAX has higher priority.
POWER_DUTY_CYCLE	50	Percent	Power Duty Cycle, defined as the time in full power to total operation time. **1**…**100**; duty cycle (%).
TIME_DUTY_CYCLE			Time/Power Duty cycle priority. **1** = Time between two consecutive fixes has priority. **2** = Power Duty cycle has higher priority.
<*CS>			CHECKSUM is a two-hex character as defined in the NMEA specification. Use of checksums is required on all input messages. For more detailed information, refer to the chapter 7.3.2.2 page 29.
<CR><LF>			Each message is terminated using Carriage Return (CR) Line Feed (LF), which is hex 0D 0A. Because 0D 0A are not printable ASCII characters, they are omitted from the example strings, but must be sent to terminate the message and cause the receiver to process that input message.

1. A value of zero for the NUM_FIXES value indicates that continuous APM cycling is requested. APM will continue to cycle until power is removed or a new APM command is received.
2. The bounds for the TIME_BTW_FIXES value for the APM is limited from 10 s to 180 s. This is slightly different than the message limits.
3. If a duty-cycle of 0 is entered, it will be rejected as out of range. If a duty-cycle value of 20 is entered, the APM module will be disabled and continuous power operation will resume.

Value	Position Error (in meters)
0	< 1 meter
1	< 5 meters
2	< 10 meters
3	< 20 meters
4	< 40 meters
5	< 80 meters
6	< 160 meters
7	No maximum
8	Reserved

6 HARDWARE INTERFACE AND CONFIGURATION SIGNALS

6.1 Pin-out of the JP15-T(X) GPS receivers

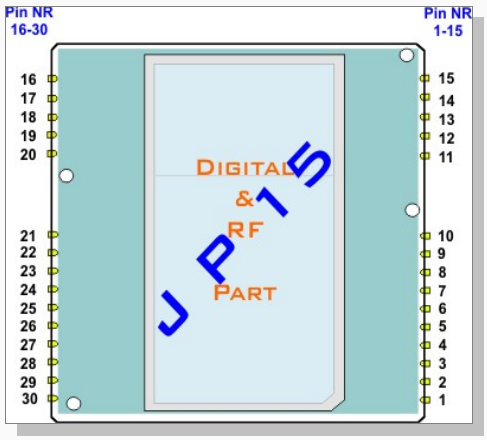


Figure 4: Pin-out of the JP15-T(X) GPS receiver

Pin	Name	I/O	Description	Level
1	VCC*	I	Main power supply. It also powers the RTC and SRAM. See chapter 6.6.	VI = 3.0 V to 3.3 VDC
2	GND*		Digital ground	GND (0 V)
3	Boot-Select	I	Boots the receiver in update mode, if high.	CMOS
4	SDI1	I	Serial Data Input A (first receive line). See chapter 6.5	CMOS 3.3 V DC level
5	SDO1	O	Serial Data Output A (first transmit line). See chapter 6.5	CMOS 3.3 V DC level
6	SDO2	O	Serial Data Output B (second transmit line). See chapter 6.5.	CMOS 3.3 V DC level
7	SDI2	I	Serial Data Input B (second receive line). See chapter 6.5.	CMOS 3.3 V DC level
8	GPIO3	I/O	GPIO Line. The internal software does not support this pin. Do not use, leave it open.	CMOS3.3 V DC level/ Imax < 50 mA
9	VCCGSP2	O	Control output for internal use, only. Do not use, leave it open.	-
10	GND*	-	Digital ground.	GND (0 V)
11	RF_GND*	-	Analog ground.	GND (0 V)
12	RF_GND*	-	Analog ground.	GND (0 V)
13	RF_GND*	-	Analog ground.	GND (0 V)
14	RF_GND*	-	Analog ground.	GND (0 V)
15	RF_GND*	-	Analog ground.	GND (0 V)
16	RF_GND*	-	Analog ground.	GND (0 V)
17	RF_IN	I	GPS RF signal input from connected antenna. See chapter 6.6.	50 Ohms @ 1.575 GHz
18	RF_GND*		Analog ground	GND (0 V)
19	V_ANT	I	Power supply for an active antenna. See chapter 6.6.	Up to +12 V DC/Imax. 25 mA
20	VCCRF	O	Supply voltage of RF section. See chapter 6.6.	+2.85.0 V DC / Imax < 25 mA
21	V_BAT	I	Power for RTC and SRAM.	+3 V DC ±5%
22	M-RST	I	Resets the GPS unit when it is driven LOW. See chapter 6.4.	LOW = 0 V (GND)
23	GPIO10	I/O	GPIO Line. The internal software does not support this pin. Do not use, leave it open.	-
24	GPIO6	I/O	GPIO Line. The internal software does not support this pin. Do not use, leave it open.	-
25	GPIO5	I/O	GPIO Line. The internal software does not support this pin. Do not use, leave it open.	-
26	GPIO7	I/O	GPIO Line. The internal software does not support this pin. Do not use, leave it open.	-
27	GPIO0	I/O	Do not connect; leave it open (floating). Internally controls the	-

			power of the low noise amplifier (LNA).	
Pin	**Name**	**I/O**	**Description**	**Level**
28	GPIO1	I/O	GPIO Line. It can be used as control output. See table 13, in chapter 7.2.1.	CMOS 3.3 V DC level/ Imax < 50 mA
29	PPS	O	1 PPS Time Mark Output. It is not supported, if XTracX software is runing or GPS receiver is set into the ATP mode. See chapter 6.4.	CMOS 3.3 V DC level
30	GND*		Digital ground	GND (0 V)

* **!!! Connect all GND and VCC pins to ensure reliable operation.**

Table 6: Pin assignment of the JP15-T(X) GPS receiver

6.2 Ball assignments of the JP15-B(X)/-ROM GPS receivers

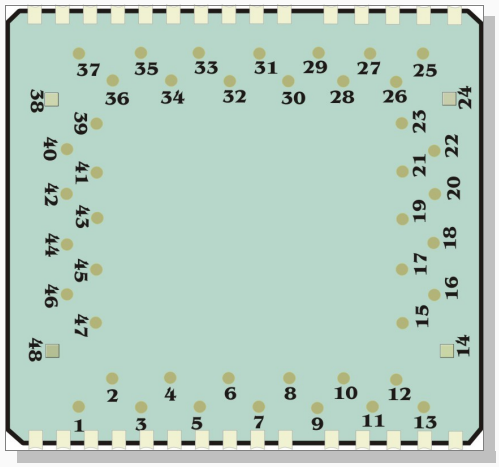


Figure 5: Ball assignments of the JP15-B(X)/-ROM GPS receivers

Ball	Name	I/O	Description	Level
1	GPIO1	I/O	GPIO Line. It can be used as control output. See table 13, in chapter 7.2.1.	CMOS 3.3 V DC level/ Imax < 50 mA
2	DATA15	I/O	Data Line. Read on power-up to determine boot. Do not use external pull up resistor. This pin has an internal 100 kΩ pull-up resistor. See chapter 6.4.	-
3	GPIO7	I/O	GPIO Line. The internal software does not support this pin. Do not use, leave it open.	-
4	GPIO5	I/O	GPIO Line. The internal software does not support this pin. Do not use, leave it open.	.
5	GPIO6	I/O	GPIO Line. The internal software does not support this pin. Do not use, leave it open.	.
6	GPIO10	I/O	GPIO Line. The internal software does not support this pin. Do not use, leave it open.	.
7	M-RST	I	Resets the unit when it is driven LOW. See chapter 6.4.	LOW = 0 V (GND)
8	V_BAT	I	Power for RTC and SRAM.	+3 V DC ±5%
9	VCCRF	O	Supply voltage of RF section. See chapter 6.6.	+2.85 V DC / Imax < 25 mA
10	V_ANT	I	Power supply for an active antenna. See chapter 6.6.	Up to +12 V DC/Imax. 25 mA
11	RF_GND*	-	Analog ground	GND (0 V)
12	RF_GND*	-	Analog ground	GND (0 V)
13	RF_IN	I	GPS RF signal input from connected antenna. See chapter 6.6.	50 Ohms @ 1.575 GHz
14	GND*	-	Digital ground	GND (0 V)
15	GND*	-	Digital ground	GND (0 V)
16	GND*	-	Digital ground	GND (0 V)
17	GND*	-	Digital ground	GND (0 V)
18	GND*	-	Digital ground	GND (0 V)
19	GND*	-	Digital ground	GND (0 V)
20	GND*	-	Digital ground	GND (0 V)

21	GND*	-	Digital ground	GND (0 V)
Ball	**Name**	**I/O**	**Description**	**Level**
22	GND*	-	Digital ground	GND (0 V)
23	GND*	-	Digital ground	GND (0 V)
24	GND*	-	Digital ground	GND (0 V)
25	GND*	-	Digital ground	GND (0 V)
26	GND*	-	Digital ground	GND (0 V)
27	GND*	-	Digital ground	GND (0 V)
28	VDDK	O	Control output for internal use, only. Do not use, leave it open.	-
29	DATA2	I/O	Read on power-up to determine output configuration. Do not use external pull up resistor. This pin has an internal 100 kΩ pull-up resistor. See chapter 6.4.	-
30	DATA3	I/O	Read on power-up to determine output configuration. Do not use external pull up resistor. This pin has an internal 100 kΩ pull-up resistor. See chapter 6.4.	-
31	VCCGSP2	O	Control output for internal use, only. Do not use, leave it open.	-
32	GPIO3	I/O	GPIO Line. It can be used as control output. See table 13, in chapter 7.2.1.	CMOS 3.3 V DC level/ Imax < 50 mA
33	SDI2	I	Serial Data Input B (second receive line). See chapter 6.5	CMOS 3.3 V DC level
34	SDO2	O	Serial Data Output B (second transmit line). See chapter 6.5.	CMOS 3.3 V DC level
35	SDO1	O	Serial Data Output A (first transmit line). See chapter 6.5.	CMOS 3.3 V DC level
36	SDI1	I	Serial Data Input A (first receive line). See chapter 6.5.	CMOS 3.3 V DC level
37	Boot-Select /DATA0	I/O	Data Line. Read on power-up to determine boot. Do not use external pull up resistor. This pin has an internal 100 kΩ pull-up resistor. See chapter 6.4.	-
38	GND*	-	Digital ground	GND (0 V)
39	VCC*	I	Main power supply. It also powers the RTC and SRAM. See chapter 6.6.	VI = 3.0 V to 3.3 VDC
40	VCC*	I	Main power supply. It also powers the RTC and SRAM. See chapter 6.6.	VI = 3.0 V to 3.3 VDC
41	GPIO2	I/O	GPIO Line. It can be used as control output. See table 13, in chapter 7.2.1.	CMOS 3.3 V DC level/ Imax < 50 mA
42	WAKEUP	O	Control output for internal use, only. Do not use, leave it open.	-
43	PWRCTL	O	Control output for internal use, only. Do not use, leave it open.	-
44	GPIO13	I/O	GPIO Line. It can be used as control output. See table 13, in chapter 7.2.1.	CMOS 3.3 V DC level/ Imax < 50 mA
45	GPIO12	I/O	GPIO Line. The internal software does not support this pin. Do not use, leave it open.	-
46	GPIO11	I/O	GPIO Line. The internal software does not support this pin. Do not use, leave it open.	-
47	PPS	O	1 PPS Time Mark Output. It is not supported if XTracX software is runing or GPS receiver is set into the ATP mode. See chapter 6.4.	CMOS 3.3 V DC level
48	GND*		Digital ground	GND (0 V)

* **!!! All GND and VCC pins must be connected to ensure reliable operation.**

Table 7: Ball assignments of the JP15-B(X)/-ROM GPS receivers

6.3 Ball assignments of the JP15-S(X)/-ROM GPS receivers

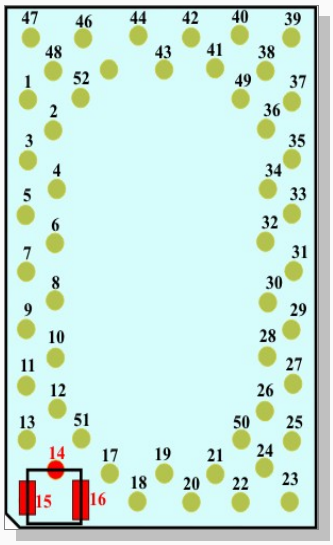


Figure 6: Balls of the JP15-S(X)/-ROM GPS receivers

Ball	Name	I/O	Description	Level
1	GPIO1	I/O	GPIO Line. It can be used as control output. See table 13, in chapter 7.2.1.	CMOS 3.3 V DC level/ Imax < 50 mA
2	GPIO0	I/O	GPIO Lines. The internal software does not support these pins. Do not use, leave these pins open.	-
3	GPIO7	I/O	GPIO Lines. The internal software does not support these pins. Do not use, leave these pins open.	-
4	GPIO5	I/O	GPIO Lines. The internal software does not support these pins. Do not use, leave these pins open.	-
5	GPIO6	I/O	GPIO Lines. The internal software does not support these pins. Do not use, leave these pins open.	-
6	GPIO10	I/O	GPIO Lines. The internal software does not support these pins. Do not use, leave these pins open.	-
7	M-RST	I	Reset the unit, when it is driven Low. See chapter 6.4. If not used leave it open.	LOW = 0V (GND)
8	V_BAT	I	Power for RTC and SRAM.	+3 V DC ±5%
9	GND*	-	Digital ground	GND (0 V)
10	VCCRF	O	Supply voltage of RF section. See chapter 6.6.	+2.85 V DC / Imax < 25 mA
11	V_ANT	I	Power supply for an active antenna. See chapter 6.6.	Up to +12 V DC/Imax. 25 mA
12	RF_GND*	-	Analog ground	GND (0 V)
13	RF_GND*	-	Analog ground	GND (0 V)
14	RF_IN	I	GPS RF signal input from connected GPS antenna. See chapter 6.6.	50 Ohms @ 1.575 GHz
15	RF_GND*	-	Analog ground	GND (0 V)
16	RF_GND*	-	Analog ground	GND (0 V)
17	RF_GND*	-	Analog ground	GND (0 V)
18	GND*	-	Digital ground	GND (0 V)
19	GND*	-	Digital ground	GND (0 V)
20	GND*	-	Digital ground	GND (0 V)
21	GND*	-	Digital ground	GND (0 V)
22	GND*	-	Digital ground	GND (0 V)
23	GPIO2	I/O	GPIO Line. It can be used as control output. See table 13, in chapter 7.2.1.	CMOS 3.3 V DC level/ Imax < 50 mA
24	DATA1	I/O	For internal use, only. Do not use, leave it open.	-
25	DATA15	I/O	Data Line. Read on power-up to determine boot. Do not use external pull up resistor. This pin has an internal 100 kΩ pull-up resistor. See chapter 6.4.	-

Ball	Name	I/O	Description	Level
26	DATA3	I/O	Read on power-up to determine output configuration. Do not use external pull up resistor. This pin has an internal 100 kΩ pull-up resistor. See chapter 6.4.	-
27	JTCK	O	Control pin for internal use, only. Do not use, leave it open.	-
28	VDDK	O	Core power at 1.5 V. Do not use, leave it open.	-
29	JTDI	I	Control pin for internal use, only. Do not use, leave it open.	-
30	GND	-	Digital Ground	GND (0 V)
31	VCCGSP2	O	Control output for internal use, only. Do not use, leave it open.	-
32	GPIO3	I/O	GPIO Line. It can be used as control output. See table 13, in chapter 7.2.1.	CMOS 3.3 V DC level/ Imax < 50 mA
33	SDI2	I	Serial Data Input B (second receive line). See chapter 6.5	CMOS 3.3 V DC level
34	SDO2	O	Serial Data Output B (second transmit line). See chapter 6.5.	CMOS 3.3 V DC level
35	SDO1	O	Serial Data Output A (first transmit line). See chapter 6.5.	CMOS 3.3 V DC level
36	SDI1	I	Serial Data Input A (first receive line). See chapter 6.5.	CMOS 3.3 V DC level
37	Boot_select /DATA0	I/O	Data Line. Read on power-up to determine boot. Do not use external pull up resistor. This pin has an internal 100 kΩ pull-up resistor. See chapter 6.4.	-
38	VCC*	I	Main power supply. It also powers the RTC and SRAM. See chapter 6.6.	VI = 3.0 V to 3.3 VDC
39	GND*	-	Digital Ground	GND (0 V)
40	VCC*	I	Main power supply. It also powers the RTC and SRAM. See chapter 6.6.	VI = 3.0 V to 3.3 VDC Imax < 200 mA
41	GND*	-	Digital Ground	GND (0 V)
42	Wakeup	O	Control output for internal use, only. Do not use, leave it open.	-
43	PWRCTL	O	Control output for internal use, only. Do not use, leave it open.	-
44	GPIO13	I/O	GPIO Line. It can be used as control output. See table 13, in chapter 7.2.1.	CMOS 3.3 V DC level/ Imax < 50 mA
45	GPIO12	I/O	GPIO Line. The internal software does not support this pin. Do not use, leave it open.	-
46	GPIO11	I/O	GPIO Line. The internal software does not support this pin. Do not use, leave it open.	-
47	GND*	-	Digital ground	GND (0 V)
48	PPS	O	1 PPS Time Mark Output. It is not supported, if XTracX software is runing or GPS Receiver is set into the ATP mode. See chapter 6.4.	CMOS 3.3 V DC level
49	VCC*	I	Main power supply. It also powers the RTC and SRAM. See chapter 6.6.	VI = 3.0 V to 3.3 VDC
50	DATA2	I/O	Read on power-up to determine output configuration. Do not use external pull up resistor. This pin has an internal 100 kΩ pull-up resistor. See chapter 6.4.	-
51	RF_GND*	-	Analog ground	GND (0 V)
52	GND*	-	Digital Ground	GND (0 V)

* **!!! All GND and VCC pins must be connected to ensure reliable operation.**

Table 8: Ball assignments of the JP15-S(X)/-ROM GPS receivers

6.4 Configuration and timing signals

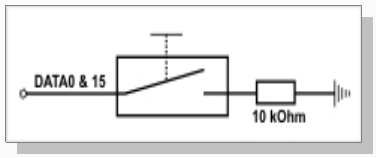
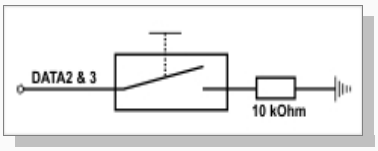
<table>
<tr><th>PIN Name</th><th>Description</th></tr>
<tr><td>M-RST</td><td>This pin provides an active-low (GND) reset input to the board. It causes the board to reset and to start searching for satellites. If not utilized, this input pin may be left open.</td></tr>
<tr><td>PPS</td><td>This pin provides 1 pulse per second output from the board, which is synchronized to within 1 microsecond of GPS time. The output is a CMOS level signal. It is not supported by the XTracX2.2.0 software and in ATP mode.</td></tr>
<tr><td>BOOT_ SELECT</td><td>Set this Pin to HIGH (+3.3 V DC) for reprogramming the Flash of the JP15-T(X) GPS receivers (for instance updating a new firmware for the JP15-T(X)).</td></tr>
<tr><td>DATA0 & DATA15</td><td>A combination between these two pins allows a choice between operating from ROM or FLASH memory. ROM is pre-loaded with GSW2.4.0 firmware while FLASH is pre-loaded with either XTracX2.2.0 or GSW2.4.0 software.
<table>
<tr><th>Function</th><th>DATA0</th><th>DATA15</th></tr>
<tr><td>Internal program (ROM)</td><td>0</td><td>0</td></tr>
<tr><td>External Program (FLASH)
(Runs either XTracX2.2.0 software with configuration 5 or GSW2.4.0 with configuration 6)</td><td>1</td><td>0</td></tr>
<tr><td>Internal Boot (loader)
(For re-programming the Flash with new firmware)</td><td>0</td><td>1</td></tr>
<tr><td>Internal Program (ROM)</td><td>1</td><td>1</td></tr>
</table>
0 = via 10 kΩ to GND (pull down resistor)
1 = Left open (disconnected)

</td></tr>
<tr><td>DATA2 & DATA3</td><td>A combination between these two pins allows a choice of the configuration from ROM on which the GPS receiver starts operation (see table 13 in chapter 7.2.1). The following configuration can be called-up only if ROM is chosen from the DATA0 & DATA15 pins.
<table>
<tr><th>Function</th><th>DATA2</th><th>DATA3</th></tr>
<tr><td>Configuration 1</td><td>0</td><td>0</td></tr>
<tr><td>Configuration 2</td><td>1</td><td>0</td></tr>
<tr><td>Configuration 3</td><td>0</td><td>1</td></tr>
<tr><td>Configuration 4</td><td>1</td><td>1</td></tr>
</table>
0 = via 10 kΩ to GND (pull down resistor)
1 = Left open (disconnected)

</td></tr>
</table>

Table 9: Configuration and timing signals

6.5 Serial communication signals

The board supports two full duplex serial channels. All serial connections are at CMOS level. If you need different voltage levels, use appropriate level shifter, (e.g. MAX 3232 from Maxim) in order to obtain RS232 compatible signal levels (see also chapter 10). All supported baud rates can be controlled from the appropriate screens in SiRFdemo software. You can directly communicate with it through a PC serial port.

PIN Name	Description
SDI1	This is the main receiving channel and is used to receive software commands to the board from SiRFdemo software or from user written software.
SDI2	This is the auxiliary receiving channel and is used to input differential corrections to the board to enable DGPS navigation.
SDO1	This is the main transmitting channel and is used to output navigation and measurement data to SiRFdemo or user written software.
SDO2	This is the auxiliary transmitting channel and is used to output navigation and measurement

	data to SiRFdemo or user written software.

Table 10: Serial communication signals

6.6 DC input signals

PIN Name	Description
VCC	This pin is the main DC power supply for 3 to 3,3 V powered boards JP15-T/-B/-S.
RF_IN	Active antennas have an integrated low-noise amplifier. They can be directly connected to this pin (**RF_IN)**. If an active antenna is connected to **RF_IN**, the integrated low-noise amplifier of the antenna needs to be supplied with the correct voltage through pin **VANT**. **Caution:** Do not connect or disconnect the antenna while the JP15--T/-B/-S is running. **Caution:** The RF_IN is always fed from the input voltage on the VANT. Do not use any input voltage on the RF_IN pin.
V_ANT	This pin is an input and reserved for an external DC power supply for an active antenna. The antenna bias for an external active antenna can be provided in two ways to pin **VANT**. In order to use a 5 V or 12 V active GPS antenna, the **VANT** has to be connected to 2.85V, 5V, or 12V external power supplies, respectively. The other possibility is available when you connect the **VCCRF** output (which provides 2.85 V) to **VANT**, so that an antenna with 3 V supply voltage can be used. **Hint:** The input voltage on the **VANT** should be chosen in according to the antenna to be used. **Note:** The GPS receivers JP15--T/-B/-S have to be connected to active GPS antennas with a maximum current of 25 mA.
VCCRF	This pin is an output, which provides +2.85 V DC, and can be connected to the V_ANT, to supply the connected GPS antenna (2.85 V active antenna). **Note:** The maximum output current on this pin should be limited upto 25 mA to protect the GPS receiver from damage.

Table 11: DC input signals

7 SOFTWARE INTERFACE

A major factor in GPS performance and capabilities is the embedded GPS software. The most suitable GPS software largely depends on the application and performance requirements. Two types of GPS software are available for the JP15 family Receivers – GSW2.4.0 and XTracX2.2.0.

- **GSW2.4.0** – embedded GPS software pre-loaded in the ROM. Based on the configuration of the JP15 family receivers, the GSW2.4.0 software offers maximum flexibility by providing Slow and Fast NMEA data rate, SiRF binary as well as Adaptive TricklePower capabilities. This software can also be loaded in the FLASH memory.
- **XTracX2.2.0** – high sensitivity GPS software pre-loaded in the FLASH. XTracX2.2.0 is designed to extend the operating range of GPS by enabling signal acquisition and tracking in extremely low signal strength environments. These include: urban canyons, undercover parking or roadways, and in many cases, indoor environments. This firmware offers maximum flexibility by providing Adaptive TricklePower capabilities.

7.1 GSW2.4.0 and XtracX2.2.0 Features

Table below lists the features that are available with the JP15 family Receivers running either GSW2.4.0 or XTracX2.2.0:

Feature	Description	GSW2.4.0 Supported	XtracX2.2.0 Supported
SBAS Capability	Improves positional accuracy by using freely available satellite-based correction services called SBAS (Satellite-based Augmentation System).	√	
DGPS Ready	Accepts DGPS corrections in the RTCM SC-104 format.	√	
SnapLock Acquisition	Reacquires satellites within 100 ms if a signal is lost.	√	
SnapStart	Obtains positions in less time when the receiver is powered on.	√	√
FoliageLock	Improves positioning performance and satellite tracking ability in difficult environments such as dense tree coverage.	√	√
TricklePower	Improves battery life using this enhanced power management mode.	√	√
Adaptive TricklePower	Intelligently switches between TricklePower and full power depending on the current GPS signal level	√	
Push-to-Fix	Provides an on demand position fix mode designed to further improve battery life.	√	
Advanced Power mode	Switches between TricklePower and full power depending on the current GPS signal level.		√
SingleSat Positioning	Provides additional fixes in an urban canyon and dense foliage environments.	√	
UART Pause	Saves power by idling the UARTs when they are not in use.	√	√
Dual Multipath Rejection	Improves position accuracy through enhanced multipath rejection	√	√
Almanac to Flash	Improves cold start times by storing the most recent almanac to flash memory.	Flash: Yes ROM: No	
Low Signal Acquisition	Acquires satellites and continues tracking in extremely low signal environments.	√	√
Low Signal Navigation	Continues navigating in extremely low signal environments.	√	√
1 PPS	A timing signal generated every second on the second. Not in ATP mode.	√	
NMEA Support	All SiRF products support a subset of the NMEA-0183 standard for interfacing marine electronic devices.	√	√
SiRF Binary Support	The SiRF Binary protocol is the standard interface protocol used by all SiRF products.	√	√

Table 12: Available Features

7.2 ROM and Flash Memory Operating Modes

The **JP15-B** & **JP15-S** feature two operating modes – a ROM operating mode, and a Flash-operating mode. If the ROM operating mode is selected, then the receiver operates using the GPS software residing in ROM, which cannot be changed. If the Flash operating mode is selected, then the receiver operates using the GPS software residing in Flash. The operating mode can be selected using the combination of both DATA2 and DATA3 pins. The ROM is loaded with GSW2.4.0 and cannot be changed. The Flash memory is user-defined GPS software. Two types of GPS software are available for the JP15 family – GSW2.4.0 and XTracX2.2.0. See chapter 1.2 for more details.

7.2.1 Internal Program (Software Code)

The Internal Program Code resides on 4Mb of ROM embedded in the chip. This GSW2 code supports many of the same features as external Flash based software. See table 13 below. It cannot be modified to support custom user code. The JP15 family will run from either its ROM based code or external Flash. For more details, please refer to the chapters 6.4 (hardware pin configuration) and 10.1.1 (steps to load the correct configuration).

	ROM based *JP15-B & JP15-S*				**FLASH based** *JP15-T(X), JP15-B(X) & JP15-S(X)*	
	Configuration 4	**Configuration 3**	**Configuration 2**	**Configuration 1 (default)**	**Configuration 5**	**Configuration 6**
	Slow NMEA	**Fast NMEA**	**SiRF Binary**	**ATP** (*Duty Cycle 300ms, 1s*)	**XTracX2.2.0** (*ATP 300ms, 1s*)	SiRF FW 2.4.0
UART A	NMEA v2.2	NMEA v2.2	SiRF Binary	NMEA v2.2	NMEA v2.2	NMEA v2.2
UART B	RTCM in	RTCM in	NMEA v2.2	SiRF Binary	Not available	RTCM
UART A Baud	4800 n,8,1	19200 n,8,1	57600 n,8,1	4800 n,8,1	38400 n,8,1	38400 n,8,1
UART B Baud	9600 n,8,1	9600 n,8,1	115200 n,8,1	38400 n,8,1	Not available	9600,n,8,1
NMEA Messages	GGA, GSA, RMC, VTG, GSV@5s, ZDA	GGA, GLL, GSA, GSV, RMC, VTG, ZDA	GGA, GLL, GSA, GSV, RMC, VTG, ZDA	GGA, GLL, GSA, GSV, RMC, VTG, ZDA	GGA, GLL, GSA, GSV, RMC, VTG	GGA, GLL, GSA, GSV, RMC, VTG
GPIO 1						
No Nav	On	On	On	On	1s On, 1s Off	1s On, 1s Off
Nav	100ms On @ 1Hz	100ms On @ 1Hz	100ms On @ 1Hz	100ms On @ 1Hz	On	On
GPIO 2						
No Nav	Off	Off	Off	Off	Off	Off
Nav	On	On	On	On	Off	Off
GPIO 3						
No Nav	Off	Off	Off	Off	Off	Off
Nav	100ms On @ 1Hz	100ms On @ 1Hz	100ms On @ 1Hz	100ms On @ 1Hz	Off	Off
GPIO 13						
No Nav	On	On	On	On	Off	Off
Nav	1s On, 1s Off	1s On, 1s Off	1s On, 1s Off	1s On, 1s Off	Off	Off

Table 13: Output Configurations

7.3 SiRF and NMEA data messages

The FALCOM JP15-T/-B/-S GPS receivers support NMEA-0183 and SiRF binary protocols. A short description of these protocols is provided herein.

For more detailed information, please, refer to the SiRFstarII message set specification available in the section "support/downloads/documentation/SiRF" at FALCOM homepage.

7.3.1 SiRF binary data message

Table 14 lists the messages for the SiRF output

Hex	ASCII	Name	Description
0 x 02	2	Measured Navigation Data	Position, velocity and time
0 x 03	3	True Tracker Data	Not implemented
0 x 04	4	Measured Tracking Data	Satellite and C/No information
0 x 06	6	SW Version	Receiver software
0 x 07	7	Clock Status	Current clock status
0 x 08	8	50 BPS Subframe Data	Standard ICD format
0 x 09	9	Throughput	Navigation complete data
0 x 0A	10	Error ID	Error coding for message failure
0 x 0B	11	Command Acknowledgement	Successful request
0 x 0C	12	Command No Acknowledgement	Unsuccessful request
0 x 0D	13	Visible List	Auto Output
0 x 0E	14	Almanac Data	Response to Poll
0 x 0F	15	Ephemeris Data	Response to Poll
0 x 10	16	Test Mode 1	For use with SiRFtest (Test Mode 1)
0 x 11	17	Differential Corrections	Received from DGPS broadcast
0 x 12	18	Ok To Send	CPU ON/OFF (Trickle Power)
0 x 13	19	Navigation Parameters	Response to Poll
0 x 14	20	Test Mode 2	Additional test data (Test Mode 2)
0 x 1C	28	Nav. Lib. Measurement Data	Measurement Data
0 x 1D	29	Nav. Lib. DGPS Data	Differential GPS Data
0 x 1E	30	Nav. Lib. SV State Data	Satellite State Data
0 x 1F	31	Nav. Lib. Initialization Data	Initialization Data
0 x FF	255	Development Data	Various status messages

Table 14: SiRF Output Messages

Table 15 lists the message list for the SiRF input messages.

Hex	ASCII	Name	Description
0 x 55	85	Transmit Serial Message	User definable message
0 x 80	128	Initialize Data Source	Receiver initialization and associated parameters
0 x 81	129	Switch to NMEA Protocol	Enable NMEA message, output rate and baud rate
0 x 82	130	Set Almanac (upload)	Sends an existing almanac file to the receiver
0 x 84	132	Software Version (Poll)	Polls for the loaded software version
0 x 85	133	DGPS Source Control	DGPS correction source and beacon receiver information
0 x 86	134	Set Main Serial Port	Baud rate, data bits, stop bits and parity
0 x 87	135	Switch Protocol	Obsolete
0 x 88	136	Mode Control	Navigation mode configuration
0 x 89	137	DOP Mask Control	DOP mask selection and parameters
0 x 8A	138	DGPS Mode	DGPS mode selection and timeout value
0 x 8B	139	Elevation Mask	Elevation tracking and navigation masks
0 x 8C	140	Power Mask	Power tracking and navigation masks

0 x 8D	141	Editing Residual	Not implemented
0 x 8E	142	Steady-State Detection – not used	Not implemented
0 x 8F	143	Static Navigation	Configuration for static operation
0 x 90	144	Poll Clock Status (Poll)	Polls the clock status
0 x 91	145	Set DGPS Serial Port	DGPS port baud rate, data bits, stop bits and parity
0 x 92	146	Poll Almanac	Polls for almanac data
0 x 93	147	Poll Ephemeris	Polls for ephemeris data
0 x 94	148	Flash Update	On the fly software update
0 x 95	149	Set Ephemeris (upload)	Sends an existing ephemeris to the receiver
0 x 96	150	Switch Operating Mode	Test mode selection, SV ID and period
0 x 97	151	Set Trickle Power Parameters	Push to fix mode, duty cycle and on time
0 x 98	152	Poll Navigation Parameters	Polls for the current navigation parameters
0 x A5	165	Set UART Configuration	Protocol selection, baud rate, data bits, stop bits and parity
0 x A6	166	Set Message Rate	SiRF binary message output rate
0 x A7	167	Low Power Acquisition Parameters	Low power configuration parameters
0 x B6	182	Set UART Configuration	Obsolete

Table 15: SiRF Input Messages

7.3.2NMEA data message

The JP15 family evaluation receivers are capable of outputting data in the NMEA-0183 format as defined by the National Marine Electronics Association (NMEA), Standard for Interfacing Marine Electronic Devices, Version 2.20, January 1, 1997.

7.3.2.1NMEA output messages

Table 16 lists all NMEA output messages supported by SiRFstarII evaluation receiver and a brief description.

Option	Description
GGA	Time, position and fix type data.
GLL	Latitude, longitude, UTC time of position fix and status.
GSA	GPS receiver operating mode, satellites used in the position solution and DOP values.
GSV	The number of GPS satellites in view satellite ID numbers, elevation, azimuth and SNR values.
RMC	Time, date, position, course and speed data.
VTG	Course and speed information relative to the ground.

Table 16: MEA Output Messages

7.3.2.2NMEA input messages

Message	MID[1]	Description
Set Serial Port	100	Set PORT A parameters and protocol
Navigation Initialization	101	Parameters required for start using X/Y/Z[2]
Set DGPS Port	102	Set PORT B parameters for DGPS input
Query/Rate Control	103	Query standard NMEA message and/or set output rate
LLA Navigation Initialization	104	Parameters required for start using Lat/Lon/Alt[3]
Development Data On/Off	105	Development Data messages On/Off
Set Trickle Power Mode	107	Parameters required for Trickle Power
MSK Receiver Interface	MSK	Command message to a MSK radio-beacon receiver.

Table 17: MEA Input Messages

1.Message Identification (MID).

2.Input co-ordinates must be WGS84.

3.Input co-ordinates must be WGS84.

Note: NMEA input messages 100 to 105 are SiRF proprietary NMEA messages. The MSK NMEA string is as defined by the NMEA 0183 standard.

7.3.2.3Transport Message

Start Sequence	Payload	Checksum	End Sequence
$PSRF<MID>[1]	Data[2]	*CKSUM[3]	<CR> <LF>[4]

1.Message Identifier consists of three numeric characters. Input messages begin with MID 100.

2.Message specific data. Refer to a specific message section for <data>...<data>definition.

3.CHECKSUM is a two-hex character checksum as defined in the NMEA specification. Use of checksums is required on all input messages.

4.Each message is terminated using Carriage Return (CR) Line Feed (LF), which is \r\n, which is hex 0D 0A. Because \r\n are not printable ASCII characters, they are omitted from the example strings, but must be sent to terminate the message and cause the receiver to process that input message.

CheckSum

The checksum is 15-bit checksum of the bytes in the payload data. The following pseudo code defines the algorithm used.

Let message to be the array of bytes to be sent by the transport.

Let ***msgLen*** *be the number of bytes in the message array to be transmitted.*

Clearly to say, the string over which the checksum has to be calculated is between the "$" and "*" (without characters "$" and "").*

Index = first

checkSum = 0

while index < msgLen

checkSum = checkSum + message[index]

checkSum = checkSum AND (2^{15}-1).

Note: All fields in all proprietary NMEA messages are required, none are optional. All NMEA messages are comma delimited.

8 MECHANICAL DRAW

The following chapters describe the mechanical dimensions of JP15-T/-B/-S and give recommendations for integrating of the JP15-T/-B/-S into your application platform. Note that, the absolute maximum dimension of the JP15-T and JP15-B module is: 25.5 mm x 25.5 mm (B x L). While the absolute maximum dimension of the JP15-S module is: 25.5 mm x 16.0 mm (B x L)

Figures 7 and 8 show the top view on JP15-T/-B/-S GPS receivers and provide an overview of the mechanical dimensions of the board, respectively.

Please note that, the JP15/-S have a dimension tolerance: ±0.1 mm.

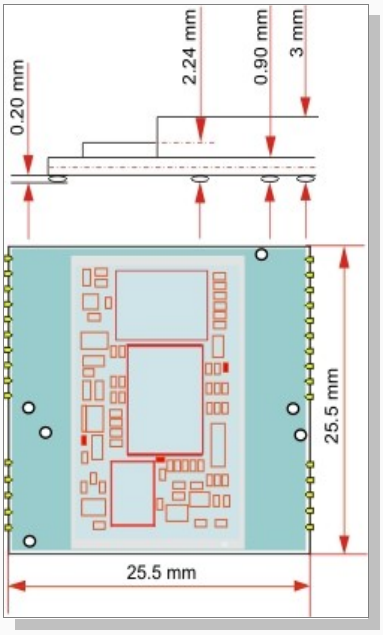


Figure 7: The mechanical draw of the JP15-T/-B

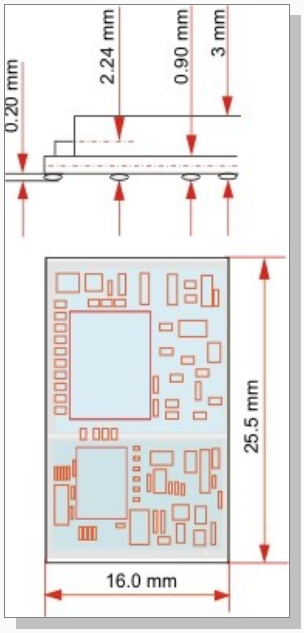


Figure 8: The mechanical draw of the JP15-S

Recommendations for layout, and soldering.

Figure 9 provides an overview of the mechanical dimensions of the JP15-T(-X) (with edge contacts).

Hint: Both GPS units JP15-T(X) and JP7-T(X) are completely identical in PCB layout.

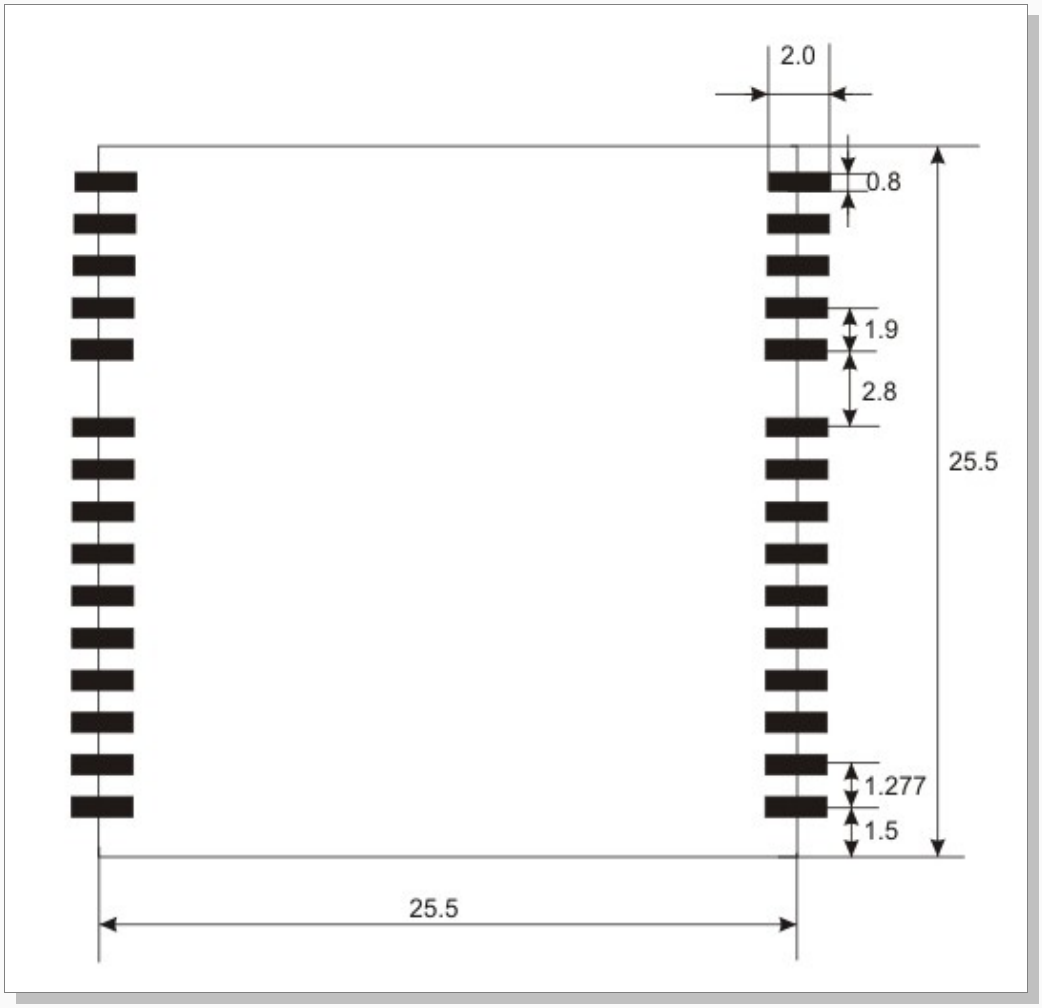


Figure 9: The mechanical draw of the JP15-T(X)

Figure 10 shows the bottom view on JP15-B(X)/-ROM and provides an overview of the mechanical dimensions of the pointed balls.

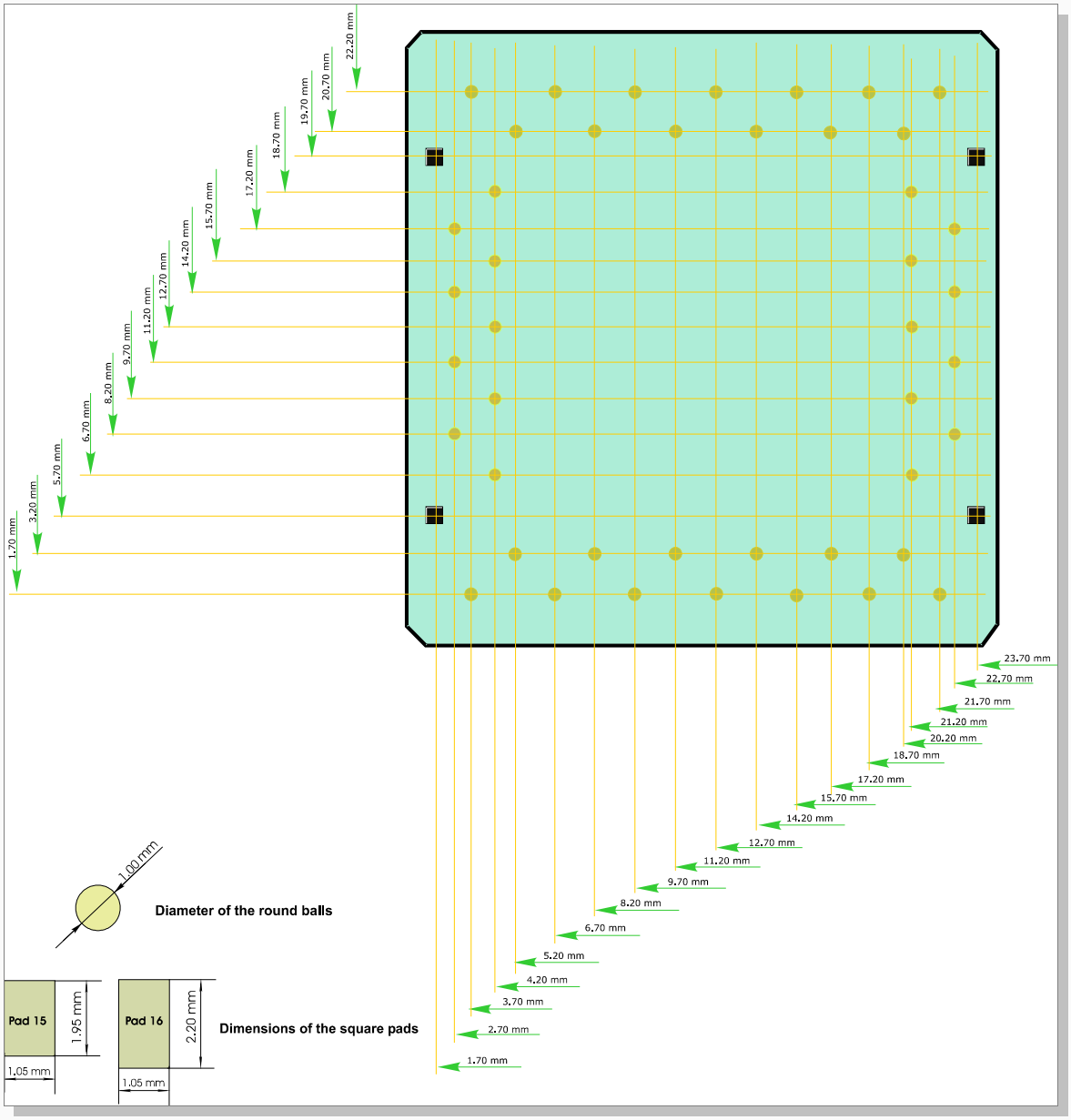


Figure 10: The mechanical draw of the JP15-B(X)/-ROM

Figure 11 shows the bottom view on JP15-S(X)/-ROM and provides an overview of the mechanical dimensions of the pointed balls.

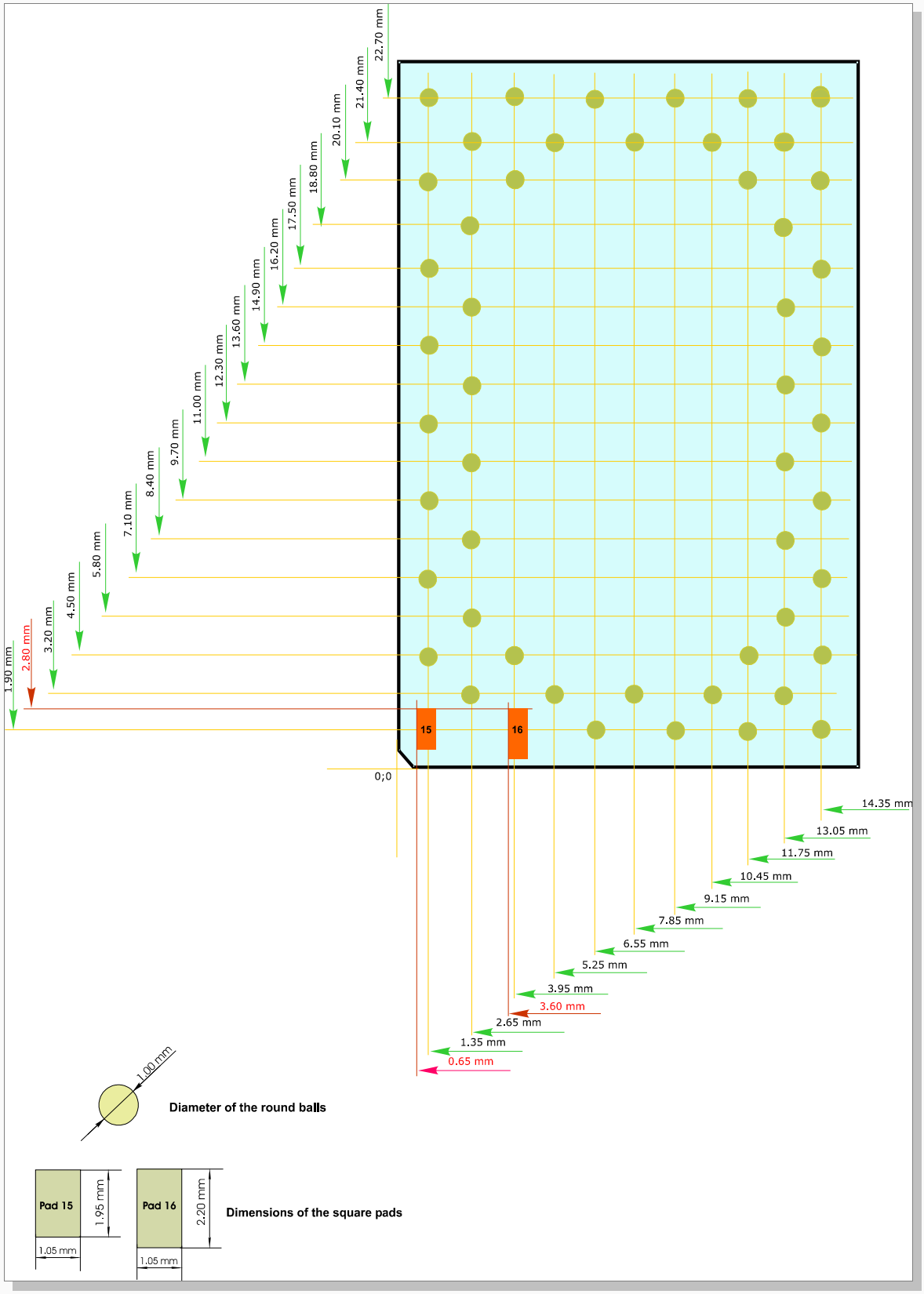


Figure 11: The mechanical draw of the JP15-S(X)/-ROM

9 LAYOUT RECOMMENDATION

9.1 Ground planes

JP15-family GPS receivers need two different ground planes. The pins RF_GND to both unit should be connected to analog ground, the pins GND to digital ground, see tables 6, 7 and 8 respectively.

The two ground planes shall be separated. Planes are connected inside the receiver (see figure 12).

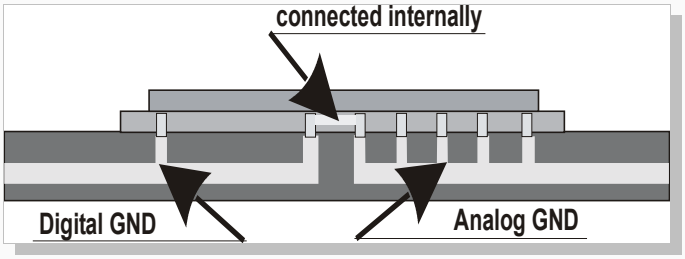


Figure 12: Ground plane of the JP15/-S GPS receivers

9.2 RF connection

The JP15-family GPS receivers are designed to be functional by using either a passive patch antenna or an antenna connector with standard RF cables. In order to make a properly RF connection, the user has to connect the antenna points to the RF pins of the JP15-family or (RF_IN, see tables 6, 7 and 8) and RF grounds (RF_GND), respectively.

9.3 Soldering profile

Figure 13 shows the recommended solder profile for Pb-free JP15 family units.

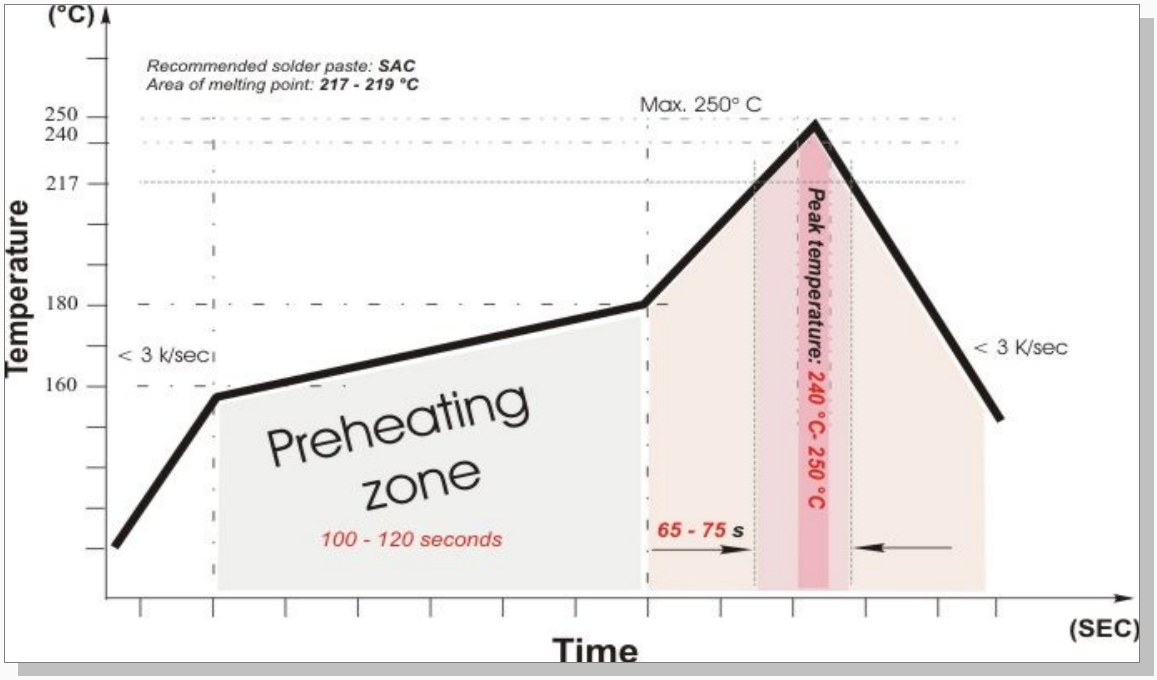


Figure 13: Typical solder conditions (temperature profile, reflow conditions).

Consider for a long time in the soldering zone (with temperature higher than 217 °C) has to be kept as short as possible to prevent component and substrate damages. Peak temperature must not exceed 250 °C.

Please note that this soldering profile is a reference to the slodering machine FALCOM utilizes. This profile can vary by using different paste types, and soldering machines, and it should be adapted to the customer application. NO liability is assumed for any damage to the module caused while soldering.

Reflow profiles in tabular form

Profile Feature	Values
Ramp-Up Rate	< 3 K/second
Preheat- zone – Temperature Range – Time	 160-180°C 100-120 seconds
Peak-zone: – Peak Temperature – Time above 217°C	 240°C .. 250°C max. 65-75 seconds
Ramp-Down Rate	< 3 K/second

Note: JP15 modules can accept only one reflow process

10 FIRST STEPS TO MAKE IT WORKS

For basic operation, only the four connections are necessary. These are:

- The GPS antenna
- Power supply for active antenna
- A RS232 communication cable with a RS232 Level shifter
- Power supply and a backup battery

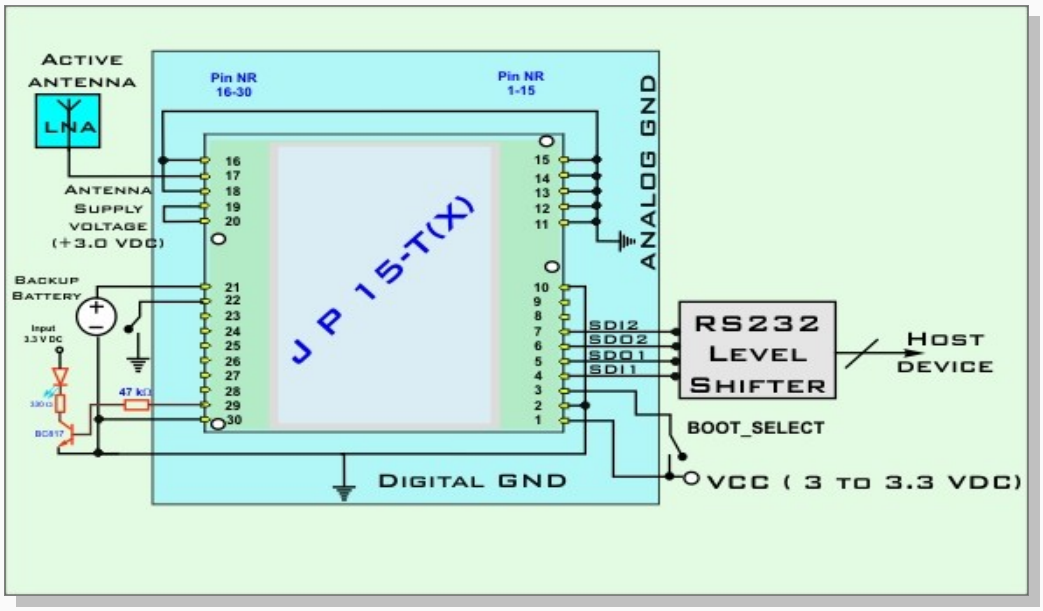


Figure 14: The minimum hardware interface of JP15-T/-S to get started.

To provide a suitable operating environment and to prevent damage avoid:

- Frequent exposure to water
- Extreme temperatures (<-40 or >+85° C)
- High vibration environments

10.1 Installing one of the JP15 family Evaluation Receivers

The same set up connection can also be made to the GPS receiver, but take into consideration the allocations of the receiver's pins (refer to the Tables 1 and 2).

Hardware Requirements	Description
Antenna	The antenna connection is the most critical part of PCB routing. Previously placing the JP15-T/-B/-S on the PCB, secure that the connection to the antenna signals is routed. In order to make it properly functional a control impedance line has to connect the RF_IN signal with antenna feed points or antenna connector, respectively. The routing on the PCB depends on your choice. For optimal operation, the following guidelines when choosing an appropriate location should be considered: ✓Choose a location that allows a unobstructed view of the sky. ✓Avoid mounting the antenna near electrical wires, other antennas, or sources of electrical interference. ✓Do not mount the antenna near transmitting antennas such as radar or satellite communication arrays.
Power	The input power is also very important as far as the minimum and maximum voltage is concerned. The power supply of JP15-T/-B/-S has to be a single voltage source of VCC at 3V to 3.3 VDC. Please, firstly connect the GND pins to target ground, and then apply power connection to the unit (+3 … +3.3 V). If the connection is made properly, the

	board is full powered and the unit begins obtaining its position fix.
Serial Interface	The JP15-T/-B/-S provides two serial interfaces. Each interface is provided with two wires the SDI1 and SDO1 support line and ground for the first serial interface (port A) and SDI2 and SDO2 support line and ground for the second serial interface (port B, if supported by the firmware used). These pins are 3.3 V CMOS compatible. In order to use different voltage levels, an appropriate level shifter has to be used. For example, in order to provide RS232 compatible levels use the 3 V compatible MAX3232 transceiver from Maxim or others based on the required levels. The GPS data will be transmitted through port A (first serial port. You can use port B (second serial port, if supported by the firmware used) to feed in DGPS correction data. Pull-up (100 kΩ) unused SDI inputs.
Active Antenna Bias Voltage	The output voltage at the antenna cable can be used to power the bias voltage of the antenna, provided can make sure that the antenna runs down to 2.7 V bias voltage and the current does not exceed 20 mA.
Backup Battery	In case of a power interruption on pin **VCC** the real-time clock and backed-up SRAM are continually supplied through **V_BAT**. The voltage at this pin has to be +3 V DC ±5%. The RTC will consume less than 10 µA (@ 3 VDC) of current during backup. If you do not use a backup battery, connect this pin to GND or leave it open (floating).

Table 20: Installing one of the JP15 family Evaluation Receivers

The quickest way to get first results with the JP15-T, JP15-B or JP15-S is to use the JP15-T, JP15-B or JP15-S adapter board respectively, together with the Evaluation board and the SiRFdemo program.

The JP15-T/-B/-T Evaluation Box offers a flexible and efficient platform to assist with GPS performance evaluation. It provides a platform on which different configurations can be tested so the best configuration for the intended application can be found.

When you order only the JP15-T, JP15-B or JP15-S GPS receiver, the Evaluation Box with contained components is not included in the delivery package. The Evaluation Box that can be used for evaluation purposes has to be purchased separately.

Figure 15: Evaluation board with connected JP15-T/-B/-S GPS receiver.

The Evaluation Box contains:

- Evaluation Board
- JP15-T/-B/-S or sample (with adapter board)
- Power supply (AC/DC adapter, Type FW738/05, Output 5VDC 1.3 A)
- Active GPS antenna (FAL-ANT-3)
- RS232 cable to your computer.
- A collection of software tools to help with the evaluation process including SiRFDemo and SiRFFlash.
- A complete collection of documentation.

The SiRFdemo manual and software are available on FALCOM's Website for free download:

➔ www.falcom.de ı Support ı Downloads ı Documentation ı SiRF ı SiRFdemo

➔ www.falcom.de ı Support ı Downloads ı Software ı SiRF ı SiRFdemo v3.1.8

10.1.1 Steps to load the correct configuration (for JP15-B(X)/-ROM/-S(X)/-ROM)

This section provides some guidelines and considerations for using the pre-loaded configurations. No general rules exist for performing evaluations because much depends on application requirements. Due to the JP15-B/-S GPS receivers feature two operating modes – a ROM operating mode with different configuration possible, and a Flash operating mode, the diagram below shows the recommended steps to be done when powering up the GPS receiver. The configuration of the hardware determines the configuration type to be currently in use (see Table **13** in chapter 7.2.1). Only one configuration type can run up at a time. Also the baud rate depends on the output configuration you choose.

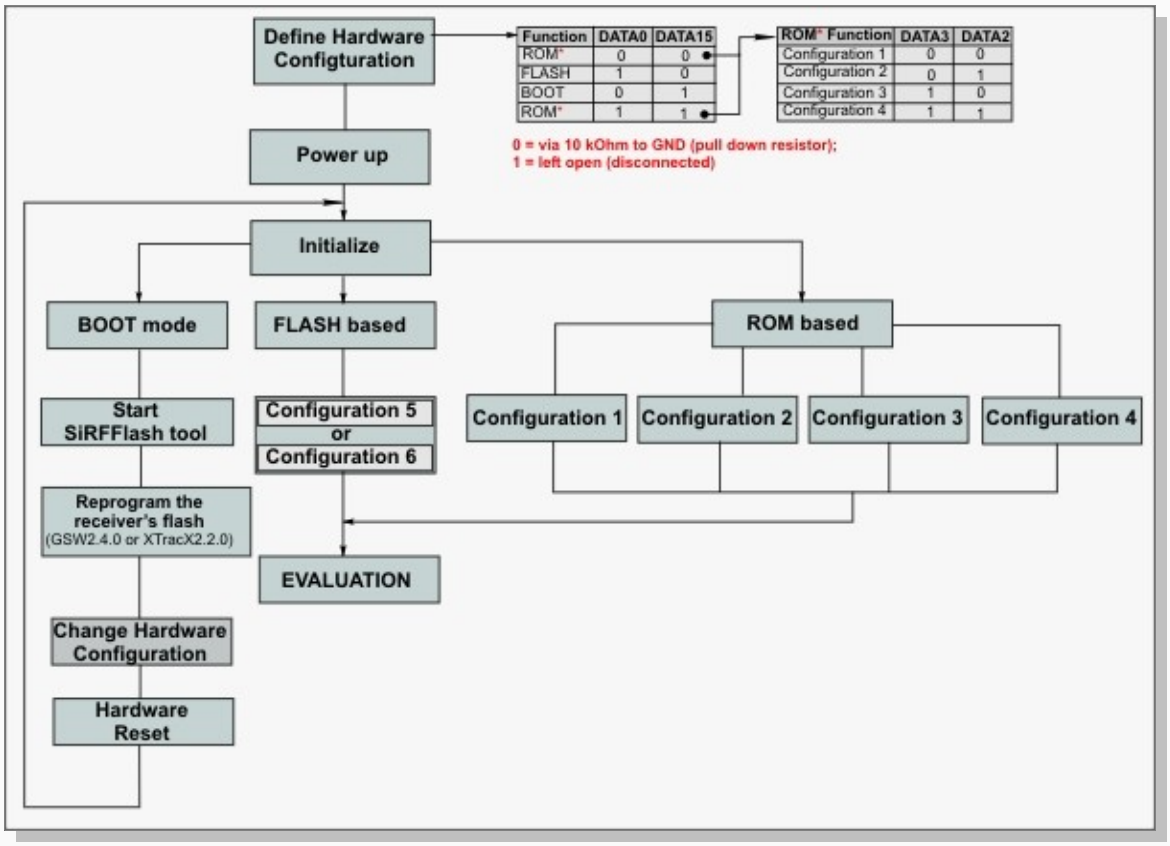


Figure 15: Required steps for loading the correct configuration.