ACCUMALATORS & LOOP UNROLLING

K , L	L=1	L=2	L=3	L=4	L=5	L=6
K=1	2.598373	2.5854024	2.583478	2.582653	2.581955	2.580353
K=2		1.303916		1.302086		1.300428
K=3			0.88588			0.885608
K=4				0.886046		
K=5					0.888493	
K=6						0.886993

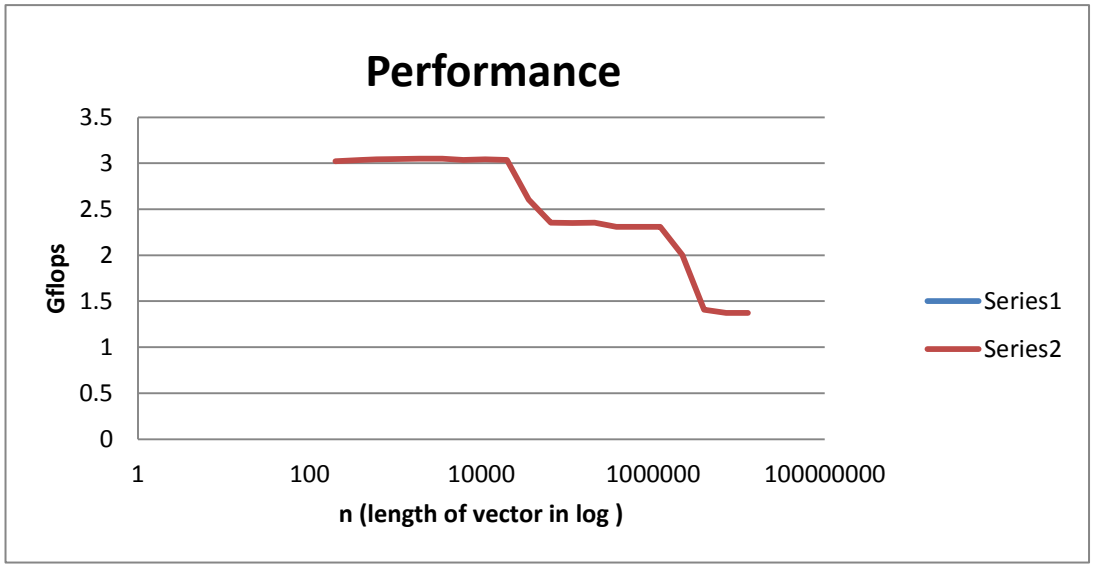
The Code was run in Stampede Supercomputer with Intel Xeon E5 - 2680 Sandy Bridge Microarchitecture. The Latency for addsd instruction is 3 cycles and it has throughput of 1cycles/issue. Thus for K=3 & L=3 it gives best results .It has one FPadd unit .

ACCUMALATORS = ceil (Latency / cycles per issue).

SCALARADD PERFORMANCE RESULTS

NOTE: Ran on Stampede Supercomputer

N	CYCLES	IPC	Gflops
200	0.893571	1.11910525	3.021584
400	0.889132	1.1246924	3.036669
600	0.887606	1.126626	3.04189
1100	0.886273	1.12832051	3.046465
1900	0.885617	1.12915628	3.048722
3500	0.885509	1.129294	3.049094
6200	0.889463	1.12427386	3.035539
11100	0.887642	1.12658031	3.041767
19900	0.88883	1.12507454	3.037701
35800	1.036266	0.96500319	2.605509
64300	1.147004	0.87183654	2.353959
115700	1.147891	0.87116285	2.35214
208300	1.147705	0.87130404	2.352521
374900	1.169614	0.85498293	2.308454
674700	1.169301	0.85521179	2.309072
1214400	1.169369	0.85516206	2.308938
2186000	1.3494	0.74107011	2.000889
3934700	1.91839	0.52127044	1.40743
7082400	1.964399	0.50906155	1.374466
12748300	1.966632	0.50848354	1.372906



ANALYSIS :

1 The code was run in Stampede Supercomputer which follows the Sandy Bridge Architecture.

2 The Sandy Bridge Intel Architecture has the following Hardware parameters

32 kB data + 32 kB instruction L1 cache (3 clocks)
256 kB L2 cache (8 clocks) per core
64-byte cache line size

3 The graph shows that there are three points of discontinuity .
The first being at n=19900
The second one at n= 1214400.
The third one at n=3934700

4 This is because till n=19900 , the entire data fits in the cache . The perf report for for the points of discontinuity is given below .
A double takes 8 bytes and thus we need 19900 x 8 = 159200 bytes
Thus out of 159200 bytes, 32768 bytes fit in the L1 cache and remaining 126462 bytes in the L2 cache . As n increases the entire data doesn't fit in the cache and thus the performance decreases as memory latency increases. Also at n=19900 , the number of accesses to the L2 cache is less than at n=35800 . It takes 3clocks for L1 cache access and 8 clocks for L2 cache. Similar is the case at other points of discontinuity.

5 The scalaradd code consumes approx. 17000 bytes . Thus it entirely fits in the 32 KB icache.

6 # PERF REPORT

Cache misses	N
2250	19900
3225	38500
80060	1214400
3690994	2186000
13635386	3934700

NOTE : All the values are approximated .