Assignment LS2

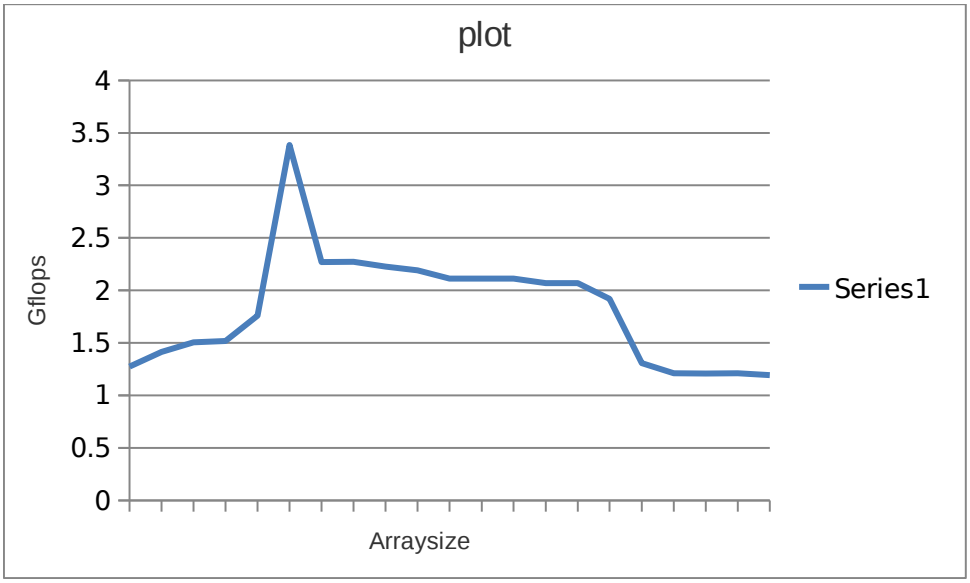
Question 1

Part (a)

FP +	UNROLLING FACTOR (L)					
K(Accumulator)	1	2	3	4	5	6
1	6.200316	6.201994	6.195033	6.187895	6.195499	6.185669
2	0	1.458311	0	1.440683	0	1.440711
3	0	0	0.981445	0	0	0.968584
4	0	0	0	0.971354	0	0
5	0	0	0	0	0	0.975341,0
6	0	0	0	0	0	0.970044

The above table suggests that as the number of accumulators is increasing along with loop unrolling the performance improves .The processor on which I ran the code is **Intel Xeon(R) X5680 3.30 GHz** for which the **latency for floating point add instruction is 3 cycles and cycles/issue is 1.**The theoretical value given by the formula is K = d latency / cycles per issue e is 3/1 = 3 = K .Now from the table for K=3 the timing is 0.981445 but it should not be less than 1 theoretically.

Part(b)



Analysis :

We see that as the array size increases the number of floating point operations per second reaches a peak and then falls off this might be because all the floating point add units in the pipeline have be fully exploited and from then onwards they are overloaded by the exponential number of floating point operations. Also it can be attributed to the number of cache misses using the perfexpert tool the following was observed.

L2d misses : 1.1 %

L3d misses : 9.3 %