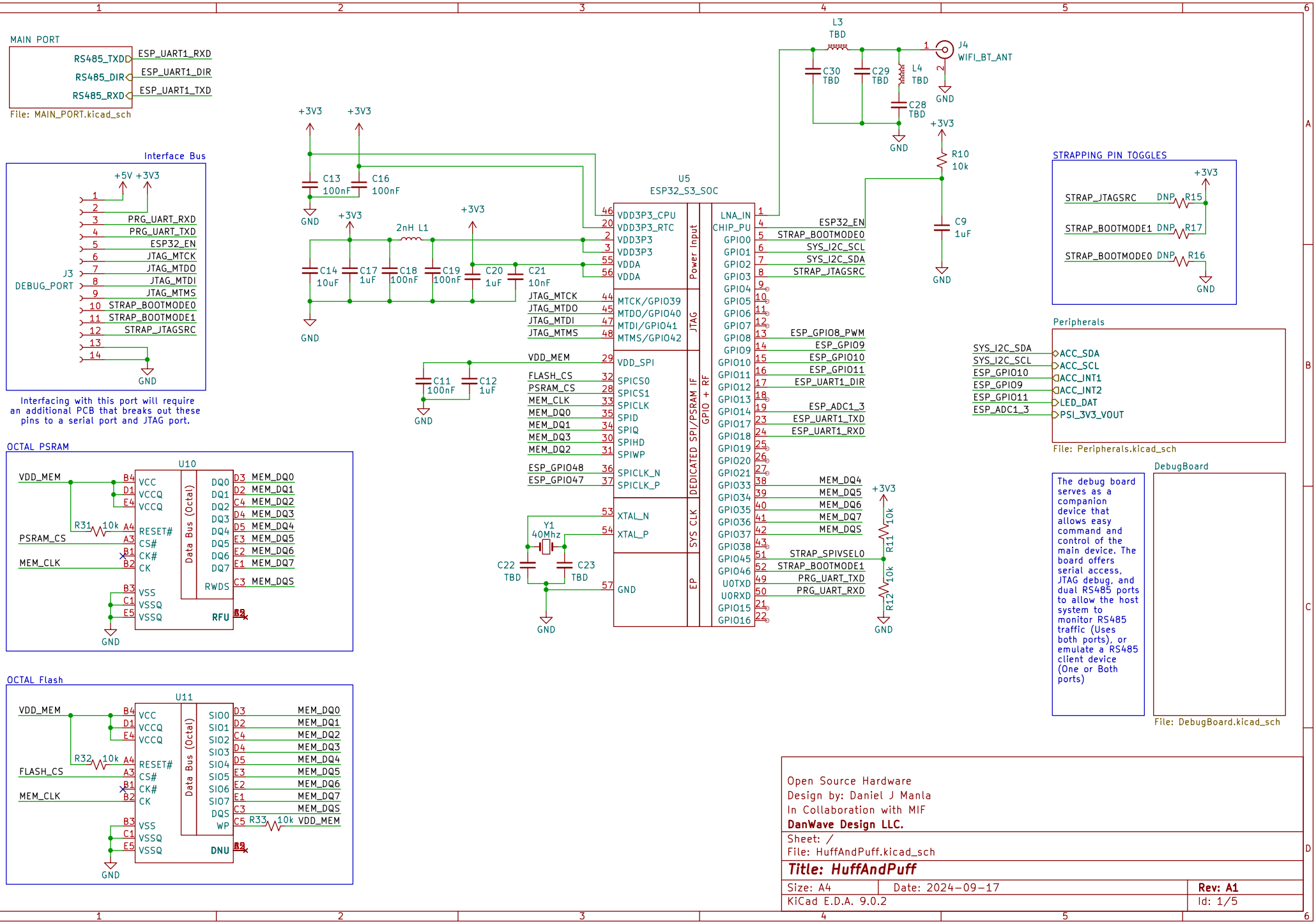
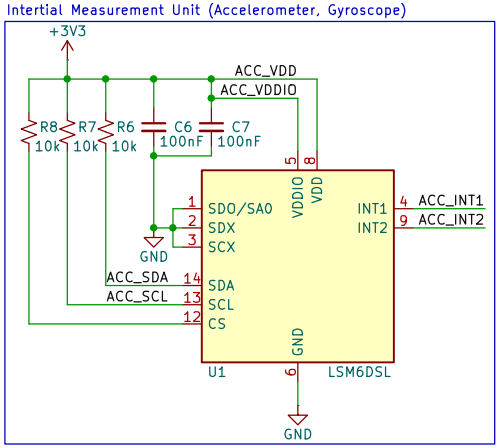

MAIN PORT
RS485_TXD
RS485_DIR
RS485_RXD
ESP_UART1_RXD
ESP_UART1_DIR
ESP_UART1_TXD
File: MAIN_PORT.kicad_sch
Interface Bus
+5V
+3V3
PRG_UART_RXD
PRG_UART_TXD
ESP32_EN
JTAG_MTCK
JTAG_MTDO
J3
DEBUG_PORT
JTAG_MTDI
JTAG_MTMS
STRAP_BOOTMODE0
STRAP_BOOTMODE1
STRAP_JTAGSRC
GND
Interfacing with this port will require an additional PCB that breaks out these pins to a serial port and JTAG port.
OCTAL PSRAM
U10
VDD_MEM
PSRAM_CS
MEM_CLK
R31
10k
RESET#
CS#
CK#
CK
VCC
VCCQ
VSS
VSSQ
Data Bus (Octal)
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
RWDS
MEM_DQ0
MEM_DQ1
MEM_DQ2
MEM_DQ3
MEM_DQ4
MEM_DQ5
MEM_DQ6
MEM_DQ7
MEM_DQS
RFU
OCTAL Flash
U11
FLASH_CS
R32
SIO0
SIO1
SIO2
SIO3
SIO4
SIO5
SIO6
SIO7
DQS
WP
R33
VDD_MEM
DNU
+3V3
C13
100nF
C16
100nF
2nH L1
C14
10uF
C17
1uF
C18
100nF
C19
100nF
C20
1uF
C21
10nF
C11
100nF
C12
1uF
U5
ESP32_S3_SOC
VDD3P3_CPU
VDD3P3_RTC
VDD3P3
VDDA
MTCK/GPIO39
MTDO/GPIO40
MTDI/GPIO41
MTMS/GPIO42
VDD_SPI
SPICS0
SPICS1
SPICLK
SPID
SPIQ
SPIHD
SPIWP
SPICLK_N
SPICLK_P
XTAL_N
XTAL_P
EP
Power Input
JTAG
DEDICATED SPI/PSRAM IF
SYS CLK
GPIO + RF
JTAG_MTCK
JTAG_MTDO
JTAG_MTDI
JTAG_MTMS
VDD_MEM
FLASH_CS
PSRAM_CS
MEM_CLK
MEM_DQ0
MEM_DQ1
MEM_DQ3
MEM_DQ2
ESP_GPIO48
ESP_GPIO47
Y1
40Mhz
C22
TBD
C23
TBD
LNA_IN
CHIP_PU
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO17
GPIO18
GPIO19
GPIO20
GPIO21
GPIO33
GPIO34
GPIO35
GPIO36
GPIO37
GPIO38
GPIO45
GPIO46
U0TXD
U0RXD
GPIO15
GPIO16
ESP32_EN
SYS_I2C_SCL
SYS_I2C_SDA
STRAP_JTAGSRC
ESP_GPIO8_PWM
ESP_GPIO9
ESP_GPIO10
ESP_GPIO11
ESP_UART1_DIR
ESP_ADC1_3
ESP_UART1_TXD
ESP_UART1_RXD
MEM_DQ4
MEM_DQ5
MEM_DQ6
MEM_DQ7
MEM_DQS
STRAP_SPIVSEL0
STRAP_BOOTMODE1
PRG_UART_TXD
PRG_UART_RXD
L3
TBD
J4
WIFI_BT_ANT
C30
TBD
C29
TBD
L4
TBD
C28
TBD
R10
10k
C9
1uF
R11
10k
R12
10k
STRAPPING PIN TOGGLES
STRAP_JTAGSRC
STRAP_BOOTMODE1
STRAP_BOOTMODE0
DNP
R15
R17
R16
Peripherals
SYS_I2C_SDA
SYS_I2C_SCL
ESP_GPIO10
ESP_GPIO9
ESP_GPIO11
ESP_ADC1_3
ACC_SDA
ACC_SCL
ACC_INT1
ACC_INT2
LED_DAT
PSI_3V3_VOUT
File: Peripherals.kicad_sch
DebugBoard
The debug board serves as a companion device that allows easy command and control of the main device. The board offers serial access, JTAG debug, and dual RS485 ports to allow the host system to monitor RS485 traffic (Uses both ports), or emulate a RS485 client device (One or Both ports)
File: DebugBoard.kicad_sch
Open Source Hardware
Design by: Daniel J Manla
In Collaboration with MIF
DanWave Design LLC.
Sheet: /
File: HuffAndPuff.kicad_sch
Title: HuffAndPuff
Size: A4
Date: 2024-09-17
Rev: A1
KiCad E.D.A. 9.0.2
Id: 1/5

ACC_SDA
ACC_SCL
ACC_INT1
ACC_INT2

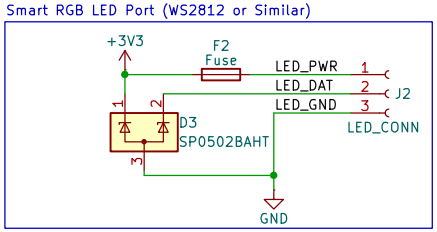
LED_DAT

PSI_3V3_VOUT

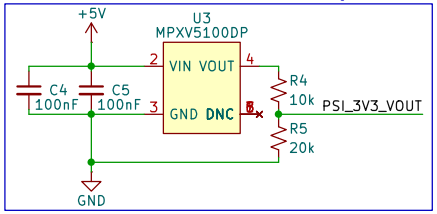
Intertial Measurement Unit (Accelerometer, Gyroscope)



Smart RGB LED Port (WS2812 or Similar)



Dual Port Differential Pressure Sensor, Analog 3.3V Out

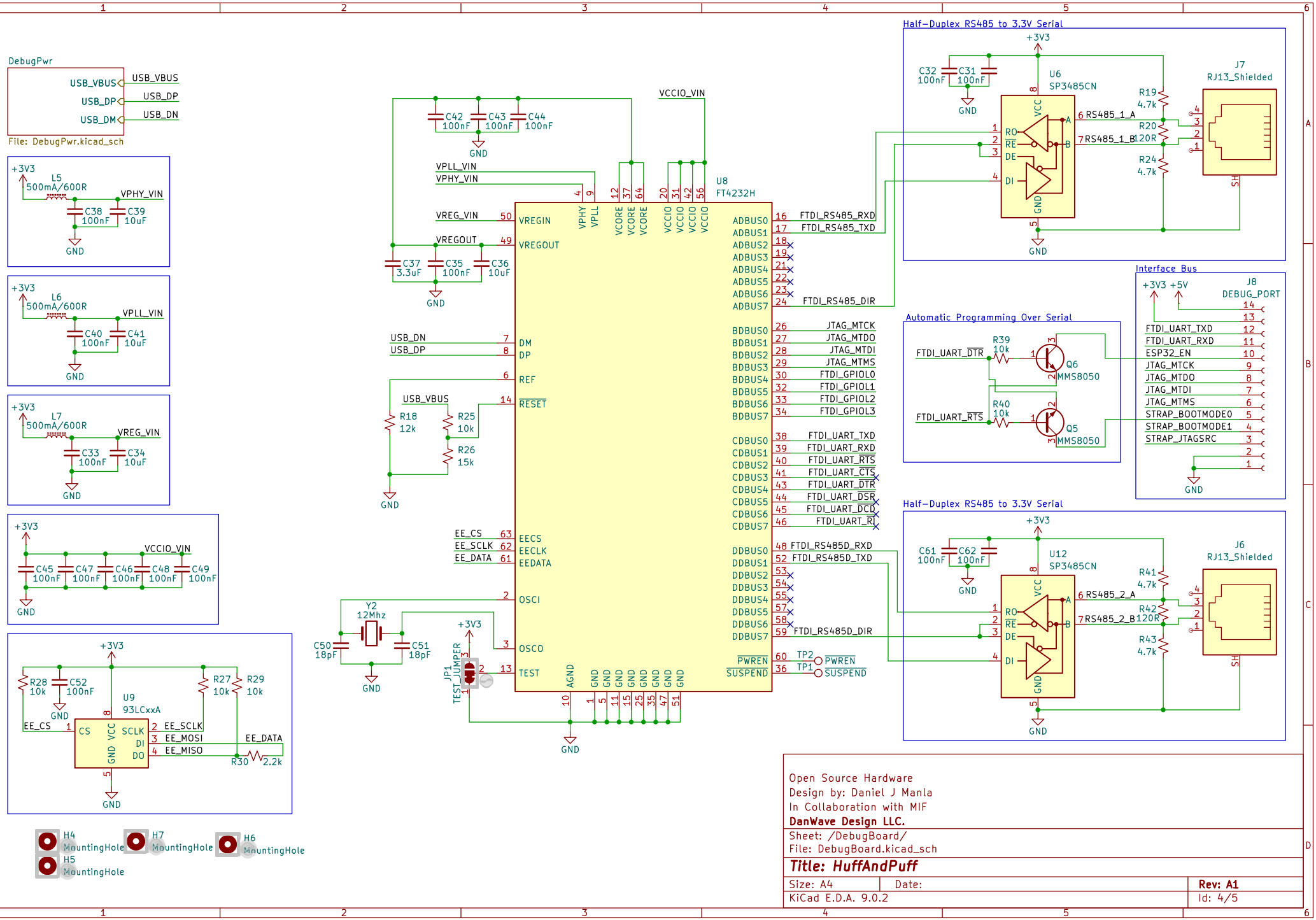


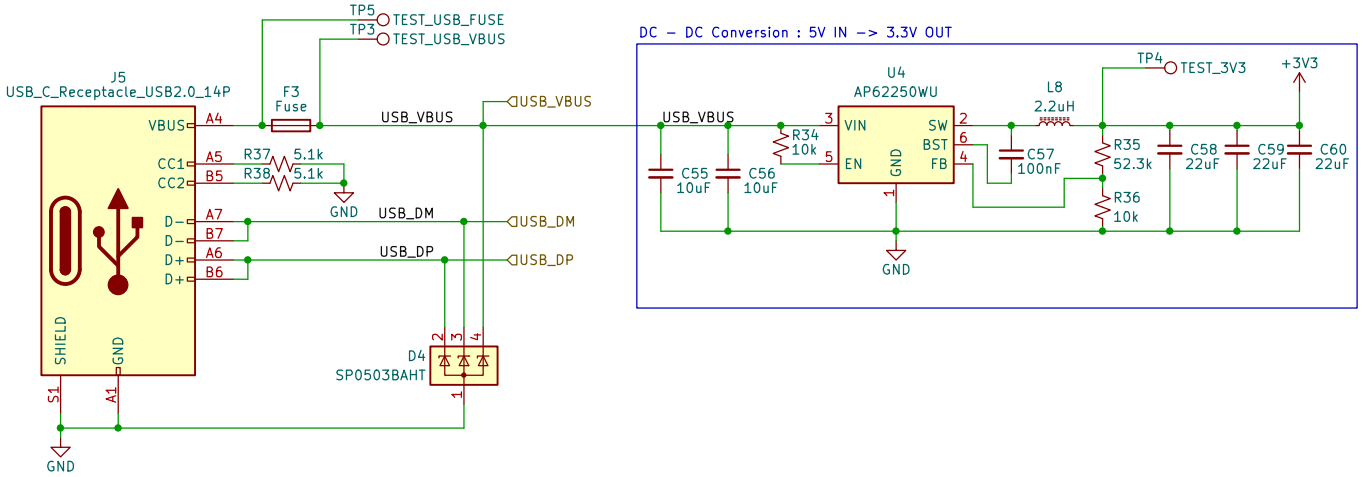
Open Source Hardware
Design by: Daniel J Manla
In Collaboration with MIF
DanWave Design LLC.

Sheet: /Peripherals/
File: Peripherals.kicad_sch

Title: HuffAndPuff

Size: A4	Date:	**Rev: A1**
KiCad E.D.A. 9.0.2		Id: 3/5


DebugPwr
USB_VBUS
USB_DP
USB_DN
File: DebugPwr.kicad_sch
+3V3
L5
500mA/600R
VPHY_IN
C38 100nF
C39 10uF
GND
L6
VPLL_IN
C40 100nF
C41 10uF
L7
VREG_IN
C33 100nF
C34 10uF
VCCIO_IN
C45 100nF
C47 100nF
C46 100nF
C48 100nF
C49 100nF
R28 10k
C52 100nF
U9
93LCxxA
EE_CS
EE_SCLK
EE_MOSI
EE_MISO
EE_DATA
R27 10k
R29 10k
R30 2.2k
H4 MountingHole
H5 MountingHole
H7 MountingHole
H6 MountingHole
C42 100nF
C43 100nF
C44 100nF
VPLL_VIN
VPHY_VIN
U8
FT4232H
VREG_IN
VREGOUT
C37 3.3uF
C35 100nF
C36 10uF
USB_DN
USB_DP
R18 12k
R25 10k
R26 15k
Y2
12Mhz
C50 18pF
C51 18pF
JP1
TEST_JUMPER
VREGIN
VPHY
VPLL
VCORE
VCCIO
DM
DP
REF
RESET
EECS
EECLK
EEDATA
OSCI
OSCO
TEST
AGND
ADBUS0 FTDI_RS485_RXD
ADBUS1 FTDI_RS485_TXD
ADBUS7 FTDI_RS485_DIR
BDBUS0 JTAG_MTCK
BDBUS1 JTAG_MTDO
BDBUS2 JTAG_MTDI
BDBUS3 JTAG_MTMS
BDBUS4 FTDI_GPIOL0
BDBUS5 FTDI_GPIOL1
BDBUS6 FTDI_GPIOL2
BDBUS7 FTDI_GPIOL3
CDBUS0 FTDI_UART_TXD
CDBUS1 FTDI_UART_RXD
CDBUS2 FTDI_UART_RTS
CDBUS3 FTDI_UART_CTS
CDBUS4 FTDI_UART_DTR
CDBUS5 FTDI_UART_DSR
CDBUS6 FTDI_UART_DCD
CDBUS7 FTDI_UART_RI
DDBUS0 FTDI_RS485D_RXD
DDBUS1 FTDI_RS485D_TXD
DDBUS7 FTDI_RS485D_DIR
PWREN
SUSPEND
TP2 PWREN
TP1 SUSPEND
Half-Duplex RS485 to 3.3V Serial
U6
SP3485CN
C32 100nF
C31 100nF
R19 4.7k
R20 120R
R24 4.7k
RS485_1_A
RS485_1_B
J7
RJ13_Shielded
Automatic Programming Over Serial
FTDI_UART_DTR
FTDI_UART_RTS
R39 10k
R40 10k
Q6 MMS8050
Q5 MMS8050
Interface Bus
J8
DEBUG_PORT
FTDI_UART_TXD
FTDI_UART_RXD
ESP32_EN
JTAG_MTCK
JTAG_MTDO
JTAG_MTDI
JTAG_MTMS
STRAP_BOOTMODE0
STRAP_BOOTMODE1
STRAP_JTAGSRC
Half-Duplex RS485 to 3.3V Serial
U12
SP3485CN
C61 100nF
C62 100nF
R41 4.7k
R42 120R
R43 4.7k
RS485_2_A
RS485_2_B
J6
RJ13_Shielded
Open Source Hardware
Design by: Daniel J Manla
In Collaboration with MIF
DanWave Design LLC.
Sheet: /DebugBoard/
File: DebugBoard.kicad_sch
Title: HuffAndPuff
Size: A4
Date:
Rev: A1
KiCad E.D.A. 9.0.2
Id: 4/5



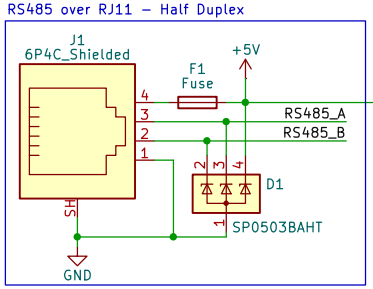
Open Source Hardware
Design by: Daniel J Manla
In Collaboration with MIF
DanWave Design LLC.

Sheet: /DebugBoard/DebugPwr/
File: DebugPwr.kicad_sch

Title: HuffAndPuff

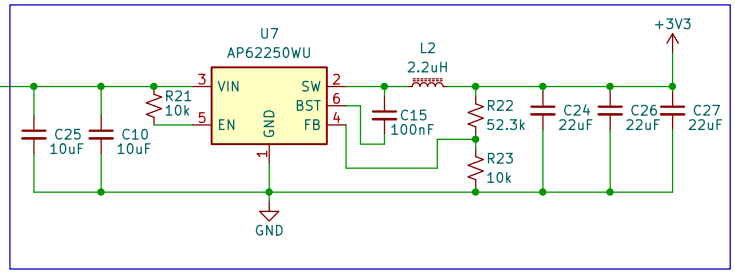
Size: A4	Date:	**Rev: A1**
KiCad E.D.A. 9.0.2		Id: 5/5

RS485 over RJ11 – Half Duplex

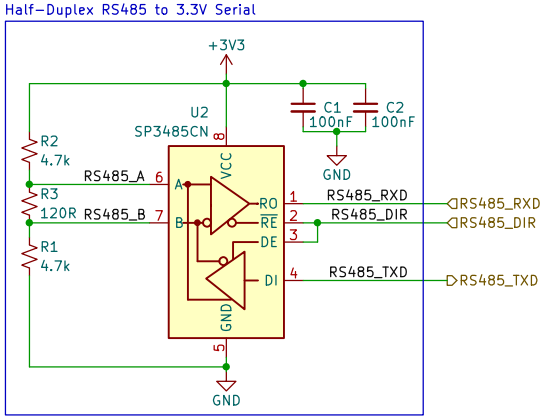


Utilize pins 2 and 3 as they are a twisted pair in typical phone cabling. Pins 4 and 1 are also twisted which may have negligible benefits to power delivery.

DC – DC Conversion : 5V IN –> 3.3V OUT



Half-Duplex RS485 to 3.3V Serial



Open Source Hardware
Design by: Daniel J Manla
In Collaboration with MIF
DanWave Design LLC.

Sheet: /MAIN PORT/
File: MAIN_PORT.kicad_sch

Title: HuffAndPuff

Size: A4	Date: 2024-09-05	**Rev: A1**
KiCad E.D.A. 9.0.2		Id: #/5