

# ***Measuring the maximum clock frequency of a circuit with Quartus II: TimeQuest tool***

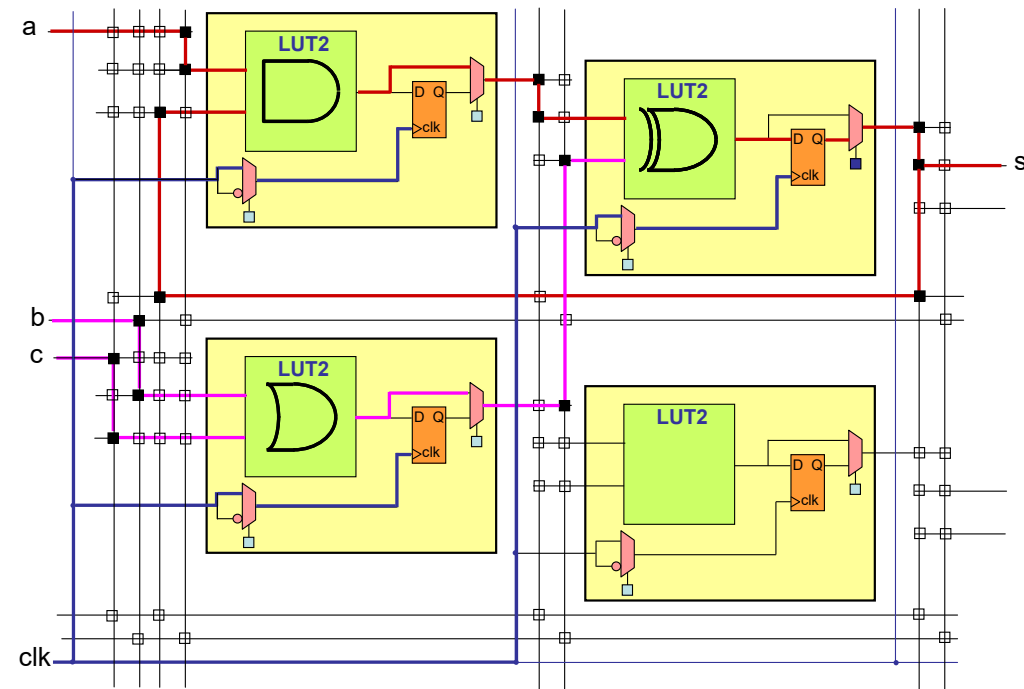
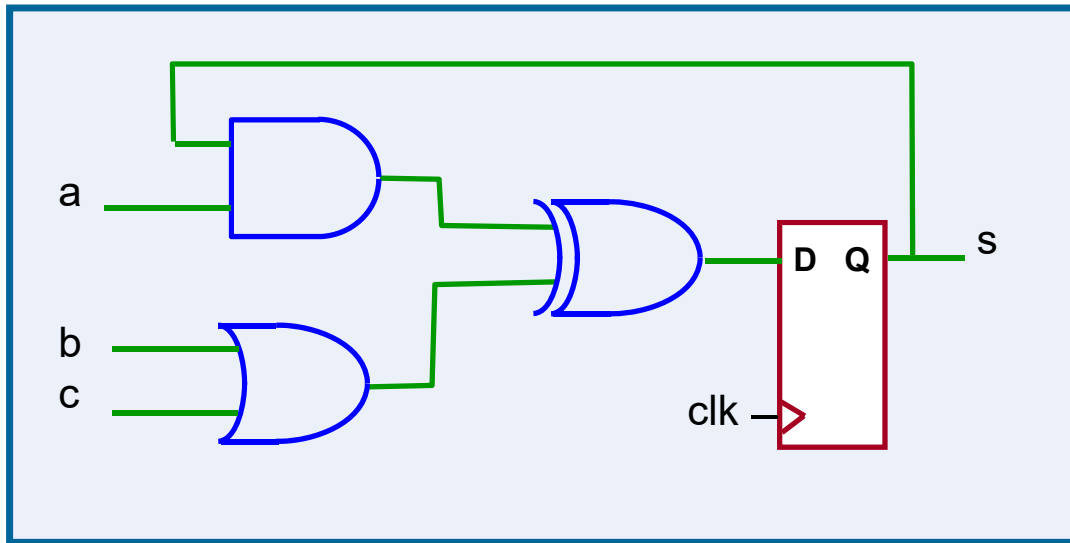
**Procesado Digital de la Señal  
en FPGA**

2020/2021

# Timing

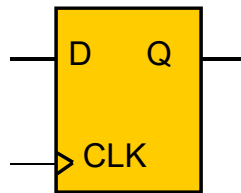
What introduce delays in a circuit implemented on an FPGA device?

- Combinational logic: LUTs, carry propagation logic & embedded multipliers
- Registers
- Routing resources: wires, routing muxes, switches

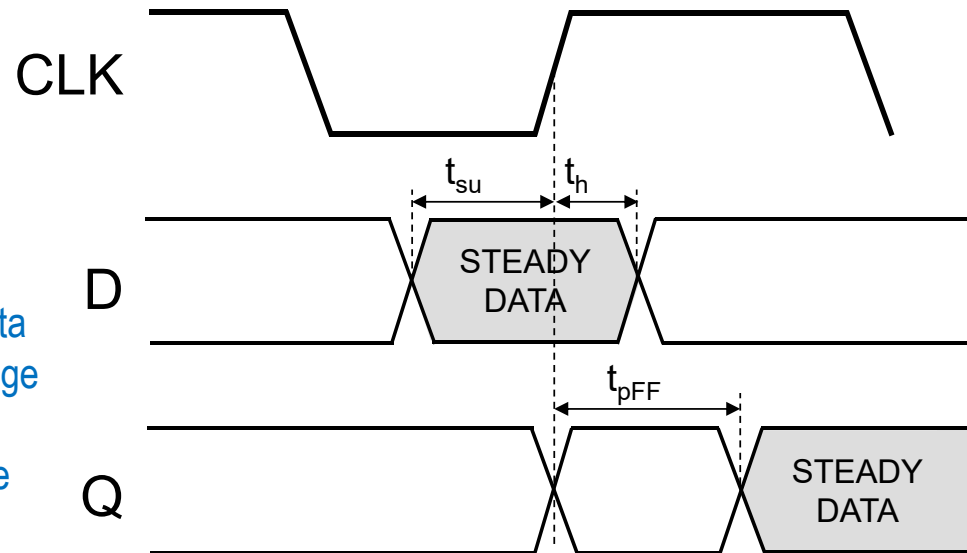


# Timing

## Flip-flop timing parameters



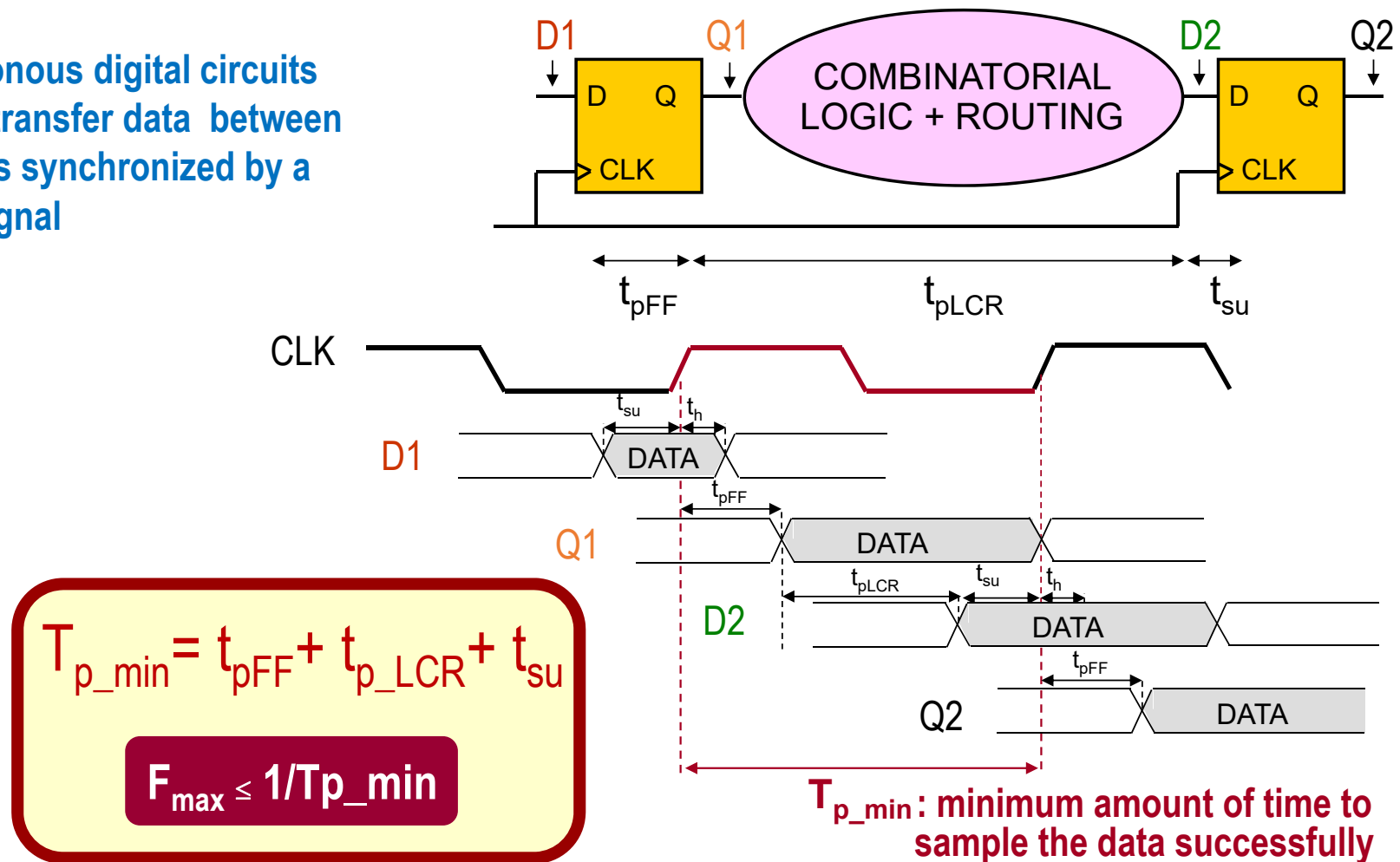
- $t_{su}$  (**set-up time**): amount of time the data must be held steady before the clock edge
- $t_h$  (**hold time**): amount of time the data must be held steady after the clock edge
- $t_{pFF}$  (**propagation time**) is the clock-to-output delay



- Setup and hold times must be guaranteed to sample the data properly
- If setup and hold times are violated  
⇒ Metastable behavior (unpredictable output)

# Timing: Maximum working frequency?

Synchronous digital circuits  
always transfer data between  
registers synchronized by a  
clock signal

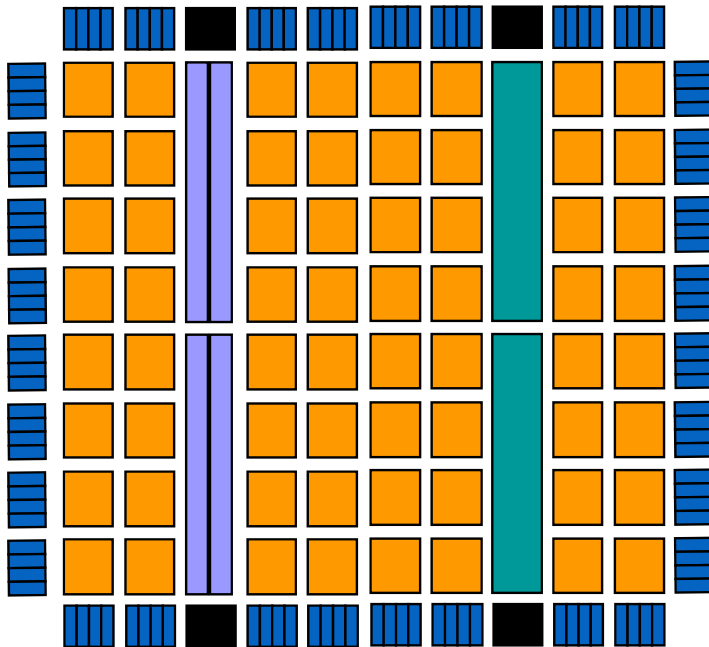


# Working frequency in FPGAs?

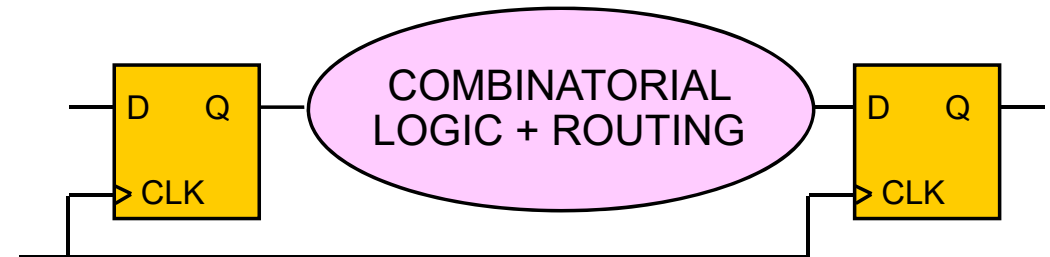
It depends on:

- the target technology (e.g. Cyclone IV  $f_{\text{clk}} < 250$  MHz)
- the critical path of the implemented circuit

**FPGA device: 28 nm, 1V**



**Critical path**

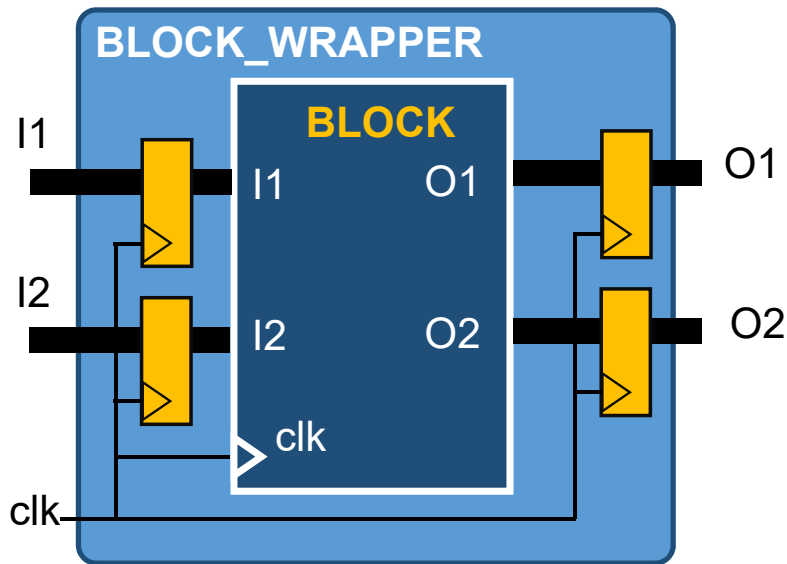


$$T_{p\_min} = t_{pFF} + t_{p\_LCR} + t_{su}$$

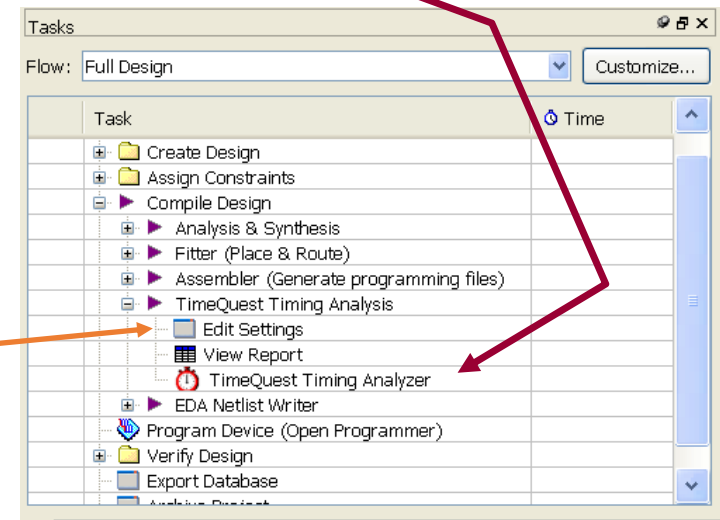
$$F_{max} \leq 1/T_{p\_min}$$

# How to measure the max. working fclk of a block?

1. Build a wrapper to instance the block and register all the inputs and outputs
2. Write the create\_clock constraint in a .sdc file to fix the target clock frequency
3. Run the STA tool: TimeQuest tool

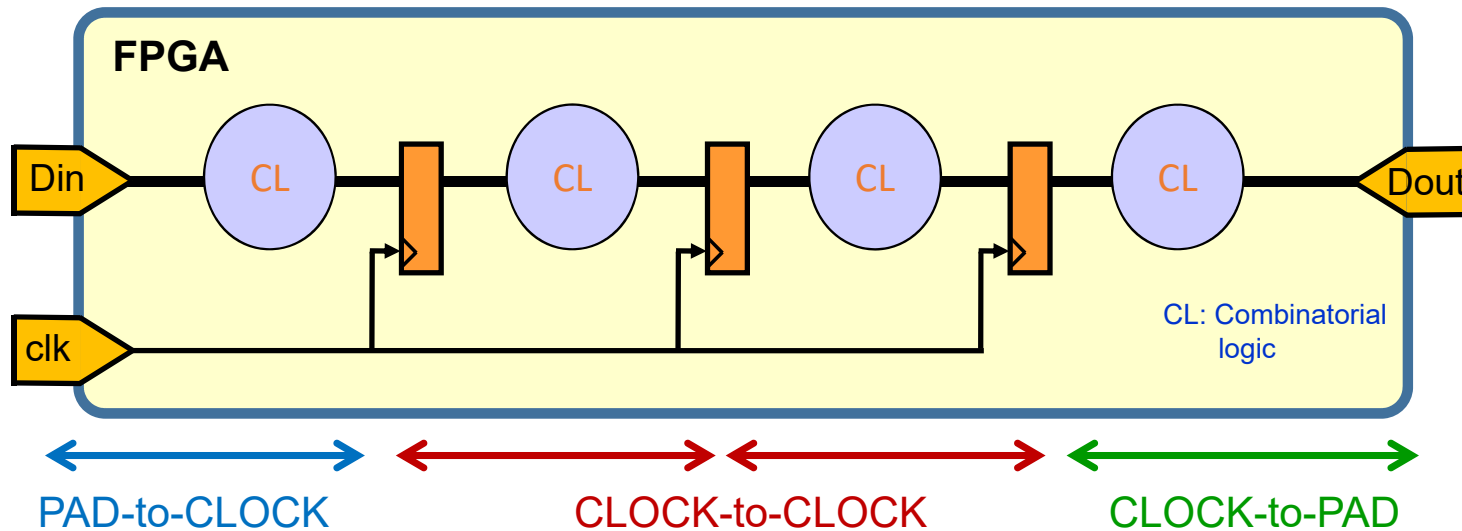


Quatus II provides the **TimeQuest** tool to analyze the timing of the circuit



A constrain file `file_name.sdc` has to be added including the **timing** constraints

# SDC timing constraints



```
set_time_format -unit ns
```

```
create_clock -name clock_m -period 20 [get_ports {clk}]
```

Specify the clock period

```
set_input_delay -clock { clock_m } -max 3 [get_ports {Din}]  
set_input_delay -clock { clock_m } -min 2 [get_ports {Din}]
```

Specify external delay  
feeding into the FPGA input

```
set_output_delay -clock { clock_m } -max 3 [get_ports {Dout}]  
set_output_delay -clock { clock_m } -min 2 [get_ports {Dout}]
```

Specify the delay from the  
FPGA output to the  
external device

file.sdc

# How to know if a circuit runs at fclk?

The screenshot shows the TimeQuest Timing Analyzer interface. The 'Report' pane on the left lists various reports, with 'Fmax Summary' selected. The 'Tasks' pane on the left shows a sequence of steps: 'Open Project...', 'Netlist Setup', 'Create Timing Netlist', 'Read SDC File', 'Update Timing Netlist', 'Reset Design', 'Set Operating Conditions...', 'Reports', 'Slack', 'Report Setup Summary', 'Report Hold Summary', 'Report Recovery Summary', 'Report Removal Summary', 'Report Minimum Pulse Width', 'Report Max Skew Summary', 'Datasheet', 'Report Fmax Summary', 'Report Datasheet', 'Device Specific', and 'Report TCCS'. The 'Fmax Summary' report is displayed in the main window, showing a table with columns: Fmax, Restricted Fmax, Clock Name, and Note. The table contains one row: 1, 212.04 MHz, 212.04 MHz, clock. A red arrow points from the text 'Max frequency' to the '212.04 MHz' value in the 'Fmax' column. Below the report, a circuit diagram is shown within a red rounded rectangle. The diagram consists of two orange rectangular blocks labeled 'D Q' (representing D-type flip-flops) connected by a blue oval labeled 'Combinatorial logic & routing'. A red arrow points from the text 'Paths between registers are only taken into account for fmax calculus' to the diagram. At the bottom of the screenshot, a text box explains: 'This panel reports FMAX for every clock in the design, regardless of the user. computed for paths where the source and destination registers or ports are c clocks, including generated clocks, are ignored. For paths between a clock a rising and falling edges are scaled along with FMAX such that the duty cycle'.

TimeQuest Timing Analyzer - /home/jvalls/FPGA/Quartus/ISC/STA/STA - STA

File View Netlist Constraints Reports Script Tools Window Help

Report

- TimeQuest Timing Analyzer S
- Advanced I/O Timing
- SDC File List
- Fmax Summary

Tasks

- Open Project...
- Netlist Setup
- Create Timing Netlist
- Read SDC File
- Update Timing Netlist
- Reset Design
- Set Operating Conditions...
- Reports
- Slack
- Report Setup Summary
- Report Hold Summary
- Report Recovery Summary
- Report Removal Summary
- Report Minimum Pulse Width
- Report Max Skew Summary
- Datasheet
- Report Fmax Summary
- Report Datasheet
- Device Specific
- Report TCCS

	Fmax	Restricted Fmax	Clock Name	Note
1	212.04 MHz	212.04 MHz	clock	

Max frequency

Paths between registers are only taken into account for fmax calculus

This panel reports FMAX for every clock in the design, regardless of the user. computed for paths where the source and destination registers or ports are c clocks, including generated clocks, are ignored. For paths between a clock a rising and falling edges are scaled along with FMAX such that the duty cycle



# How to know if a circuit runs at fclk?

TimeQuest Timing Analyzer - B:/FPGA/Quartus/ISC/CIC\_2S\_14/CIC\_2S - CIC\_2S

File View Netlist Constraints Reports Script Tools Window Help

Search altera.com

Report

- TimeQuest Timing Analyzer Summary
  - Advanced I/O Timing
    - Fmax Summary

Tasks

- Open Project...
- Netlist Setup
  - Create Timing Netlist
  - Read SDC File
  - Update Timing Netlist
- Reset Design
- Set Operating Conditions...
- Reports
  - Slack
    - Report Setup Summary
    - Report Hold Summary
    - Report Recovery Summary
    - Report Removal Summary
    - Report Minimum Pulse Width
    - Report Max Skew Summary
  - Datasheet
    - Report Fmax Summary
    - Report Datasheet
  - Device Specific
    - Report TCCS
    - Report RSKM
    - Report DDR
    - Report Metastability
  - Dagnostic
    - Report Clocks
    - Report Clock Transfers

Fmax Summary

	Fmax	Restricted Fmax	Clock Name	Note
1	343.29 MHz	250.0 MHz	clk	limit due to minimum period restriction (max I/O toggle rate)

The circuit could run faster, but it is limited by the maximum supportable clock frequency

for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are scaled along with FMAX, such that the duty cycle (in terms of a percentage) is maintained. Altera recommends that you always use clock constraints and other slack reports for sign-off analysis.

# Setup critical path analysis

The screenshot displays the TimeQuest Timing Analyzer interface. The main window shows the 'Set Operating Conditions' panel with 'Slow 1200mV 85C Model' selected. The 'Report' panel on the left shows a tree view where 'Report Timing...' is highlighted under 'Custom Reports'. A 'Report Timing' dialog box is open on the right, showing the 'Setup' analysis type. The 'From clock' and 'To clock' are both set to 'clk'. The 'Report number of paths' is set to 1. The 'Detail level' is set to 'Full path'. The 'Report panel name' is 'Report Timing'. The 'File options' are set to 'Overwrite'. The 'Tcl command' is shown at the bottom: `lock { clk } -setup -npaths 1 -detail full_path -panel_name {Report Timing} -multi_corner`.

TimeQuest Timing Analyzer - D:/madd/madd - madd

File View Netlist Constraints Reports Script Tools Window Help

Set Operating Conditions

Slow 1200mV 85C Model

	Fmax	Restricted Fmax	Clock Name
1	125.09 MHz	125.09 MHz	clk

Report

- TimeQuest Timing Analyzer Summary
- Advanced IO Timing
- SDC File List
- Fmax Summary
  - Multi Corner Summary (1/3 corners)
  - Slow 1200mV 85C Model
  - Slow 1200mV 0C Model
  - Fast 1200mV 0C Model

Tasks

- Report Ignored Constraints
- Check Timing
- Report Partitions
- Custom Reports
  - Report Timing...
  - Report Timing Tree
  - Report Minimum Pulse Width...
  - Report False Path...
  - Report Path...

Report Timing

Clocks

From clock: clk

To clock: clk

Targets

From:

Through:

To:

Analysis type

Setup

Hold

Recovery

Removal

Paths

Report number of paths: 1

Maximum number of paths per endpoint:

Maximum slack limit: ns

Pairs only

Output

Detail level: Full path

Show routing

Report panel name: Report Timing

Enable multi corner reports

File name:

File options

Overwrite Append

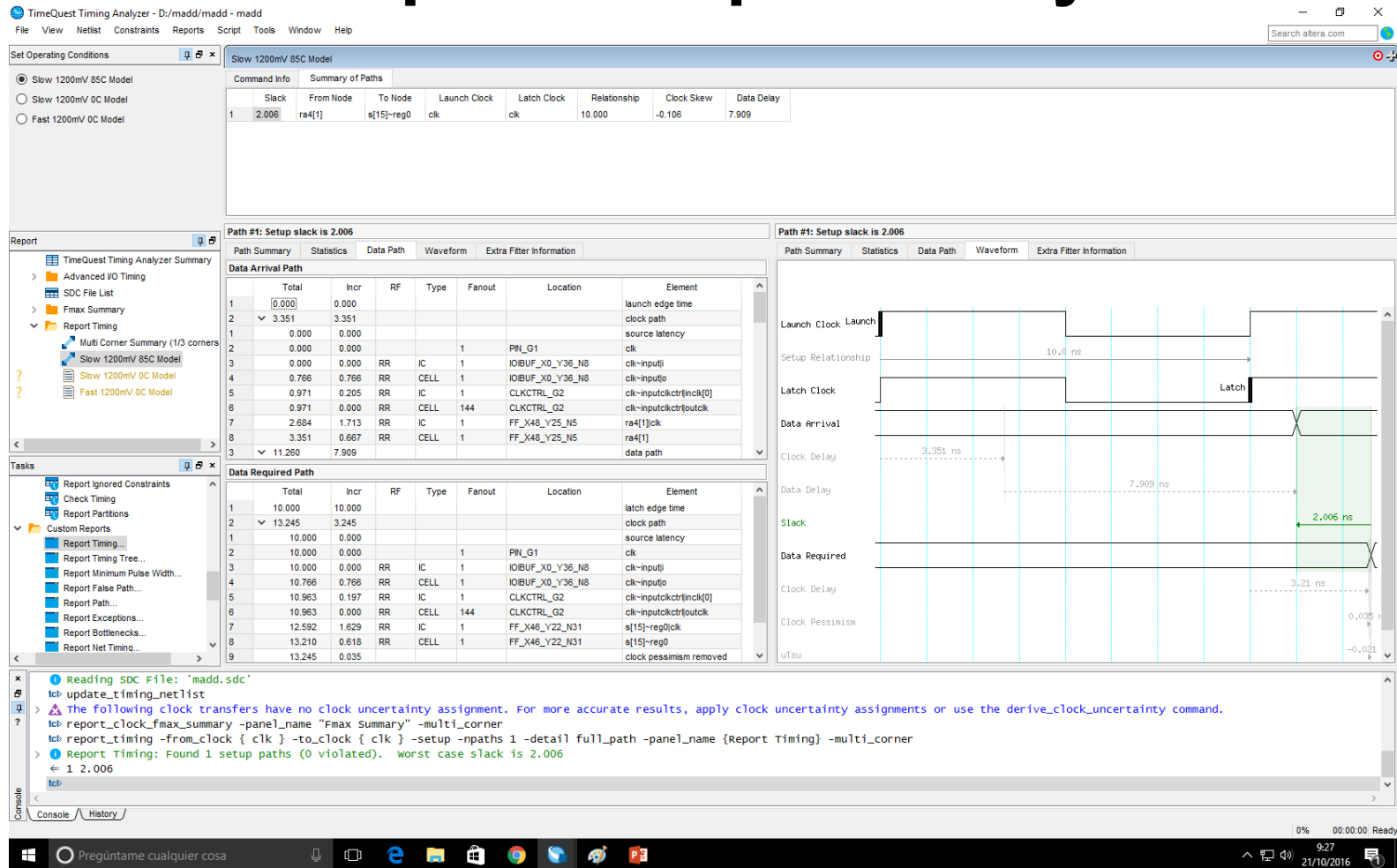
Open

Console

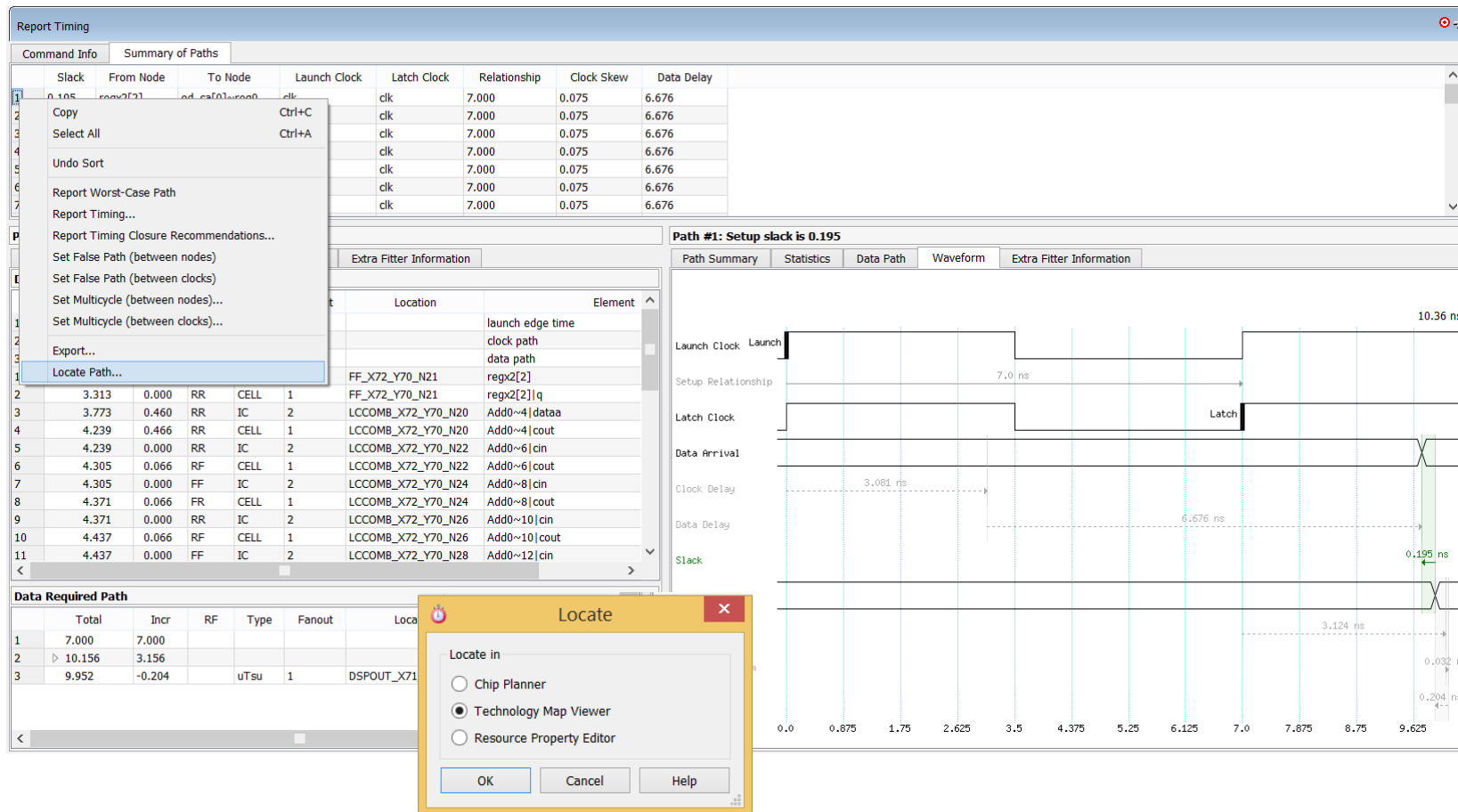
Tcl command: lock { clk } -setup -npaths 1 -detail full\_path -panel\_name {Report Timing} -multi\_corner

Report Timing Close Help

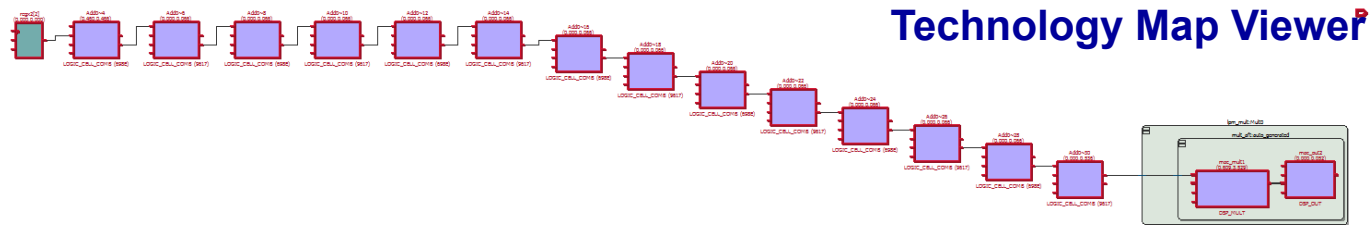
## Setup critical path analysis



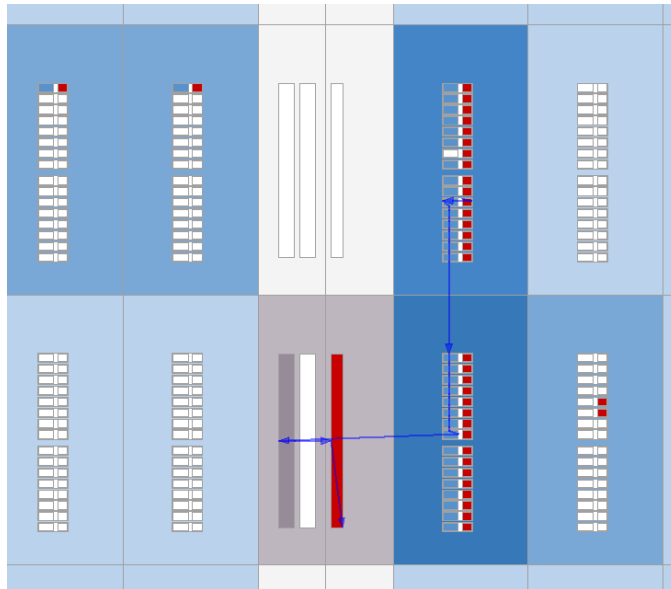
# Setup critical path analysis



## Setup critical path analysis



# Chip Planner



## Resource Property Editor

