Measuring the maximum clock frequency of a circuit with Quartus II: TimeQuest tool

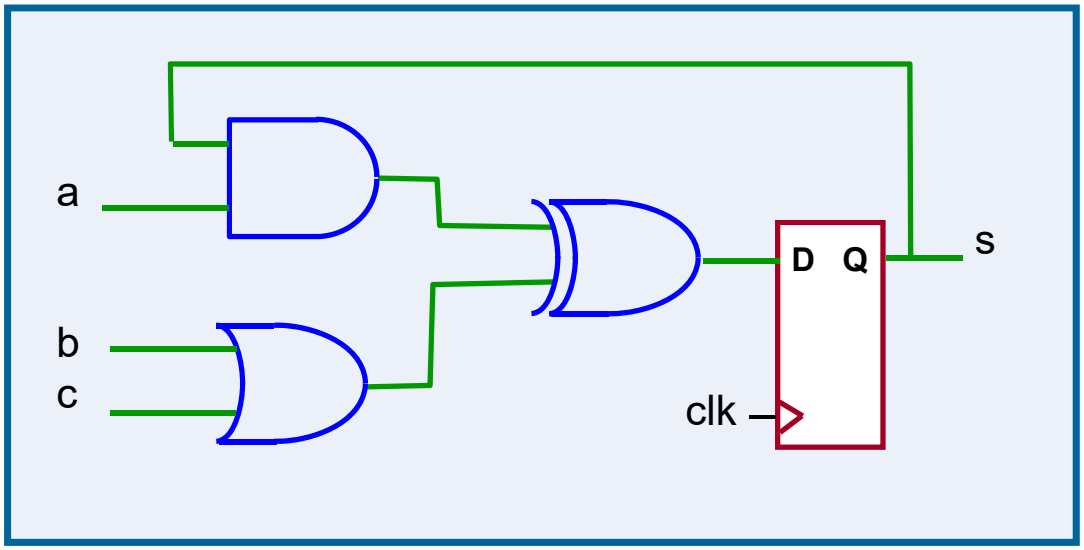
Procesado Digital de la Señal en FPGA

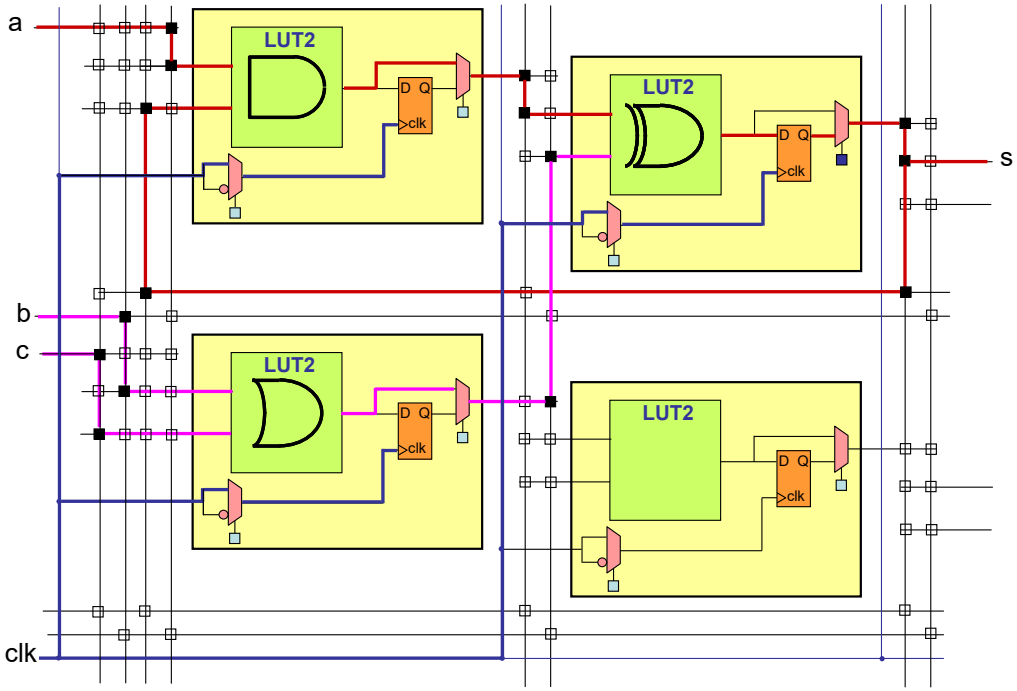
2020/2021

Timing

What introduce delays in a circuit implemented on an FPGA device?

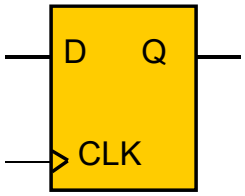
- Combinational logic: LUTs, carry propagation logic & embedded multipliers
- Registers
- Routing resources: wires, routing muxes, switches



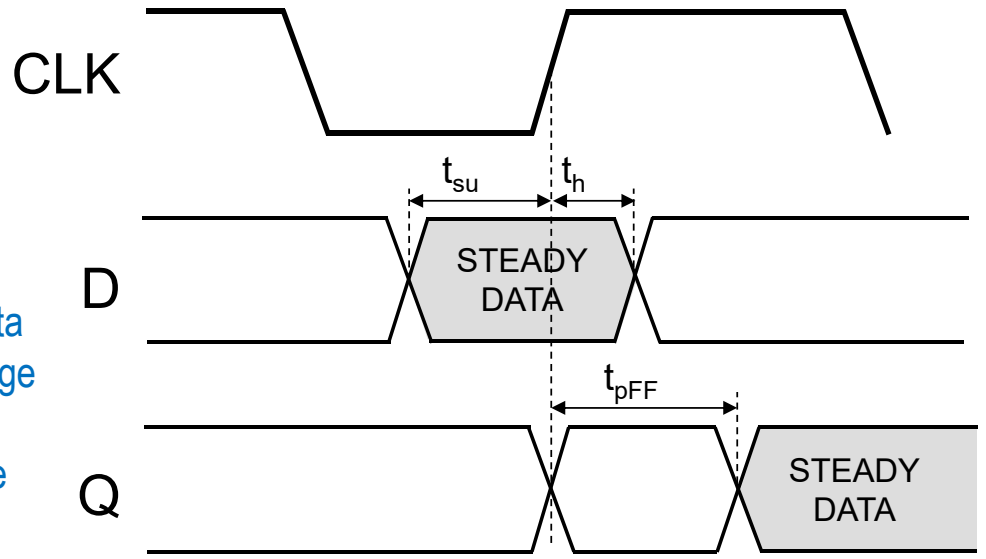


Timing

Flip-flop timing parameters



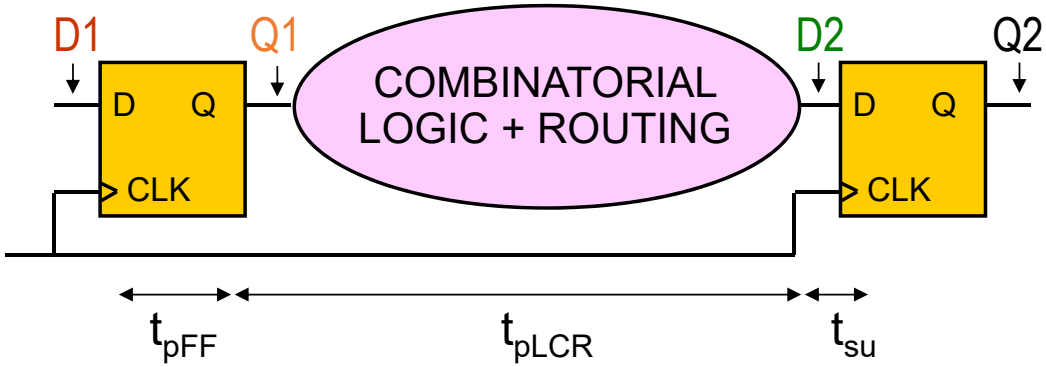
- t_{su} **(set-up time)**: amount of time the data must be held steady before the clock edge
- t_h **(hold time)**: amount of time the data must be held steady after the clock edge
- t_{pFF} **(propagation time)** is the clock-to-output delay

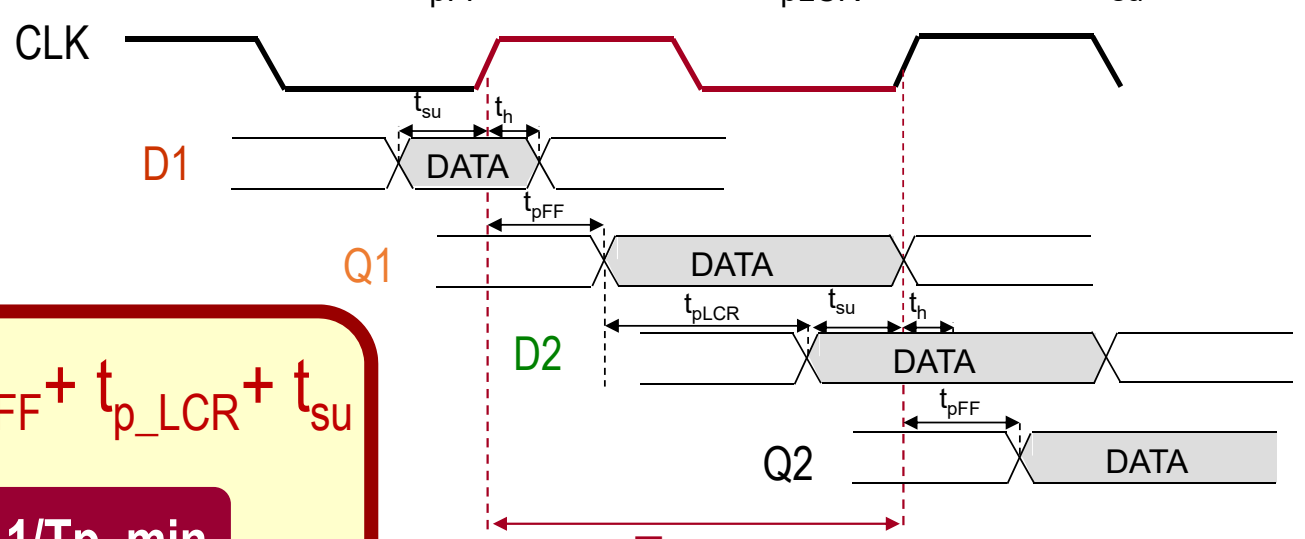


- **Setup and hold times must be guarantee to sample the data properly**
- **If setup and hold times are violated**
  $\Rightarrow$ Metastable behavior (unpredectible output)

Timing: Maximum working frequency?

Synchronous digital circuits always transfer data between registers synchronized by a clock signal





$T_{p\_min} = t_{pFF} + t_{p\_LCR} + t_{su}$

$F_{max} \leq 1/Tp\_min$

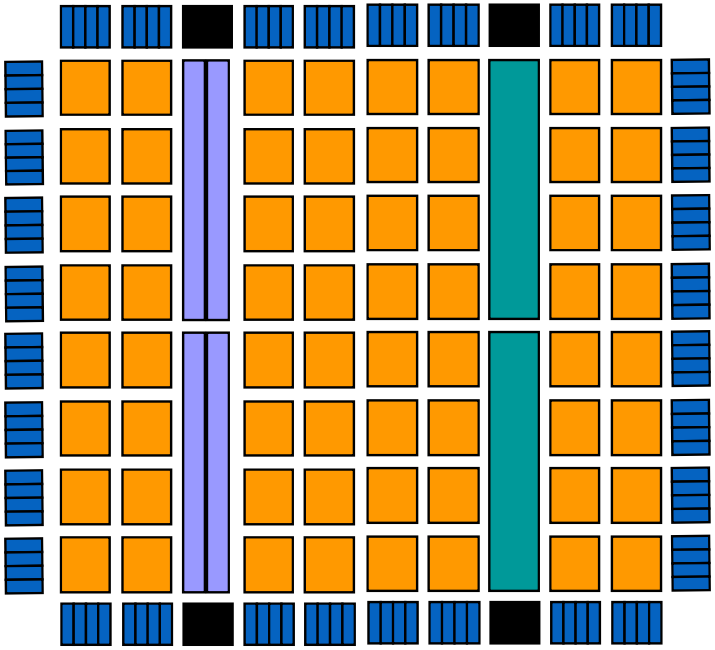
T_{p_min}: minimum amount of time to sample the data successfully

Working frequency in FPGAs?

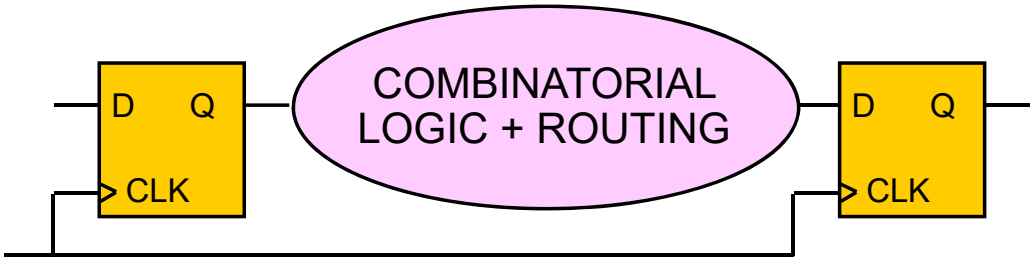
It depends on:

- the target technology (*e.g.* Cyclone IV $f_{clk} < 250$ MHz)
- the critical path of the implemented circuit

FPGA device: 28 nm, 1V



Critical path

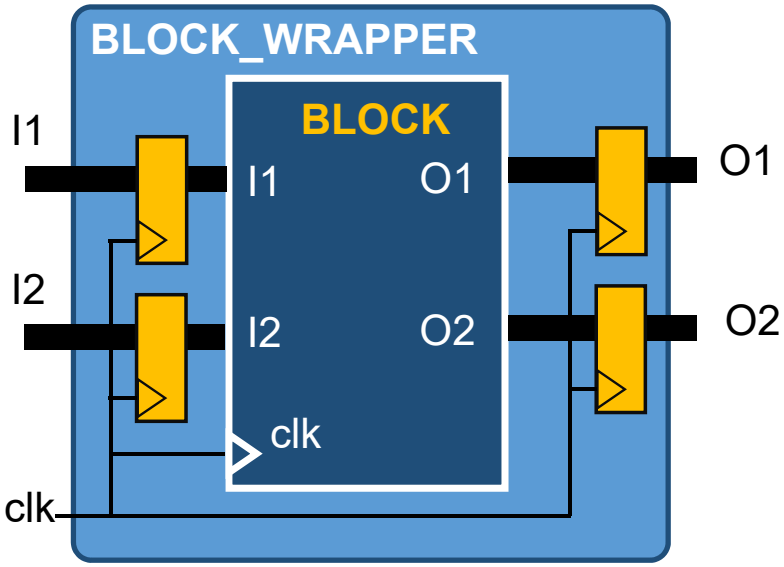


$$T_{p\_min} = t_{pFF} + t_{p\_LCR} + t_{su}$$

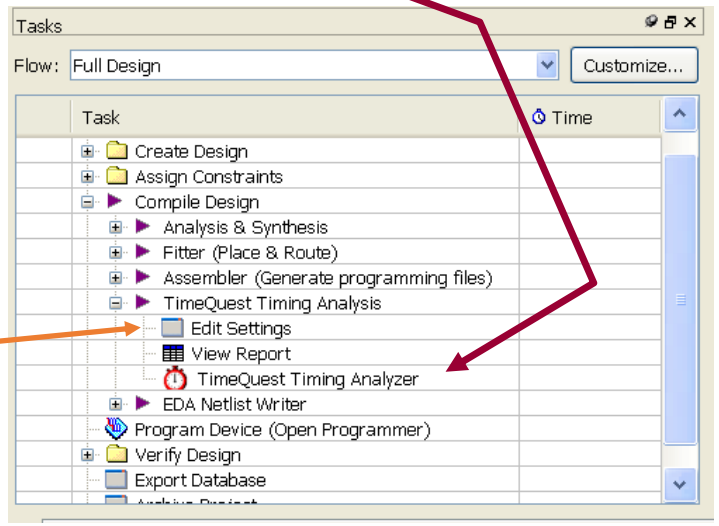
$$F_{max} \leq 1/Tp\_min$$

How to measure the max. working fclk of a block?

1. Build a wrapper to instance the block and register all the inputs and outputs
2. Write the create_clock constraint in a .sdc file to fix the target clock frequency
3. Run the STA tool: TimeQuest tool

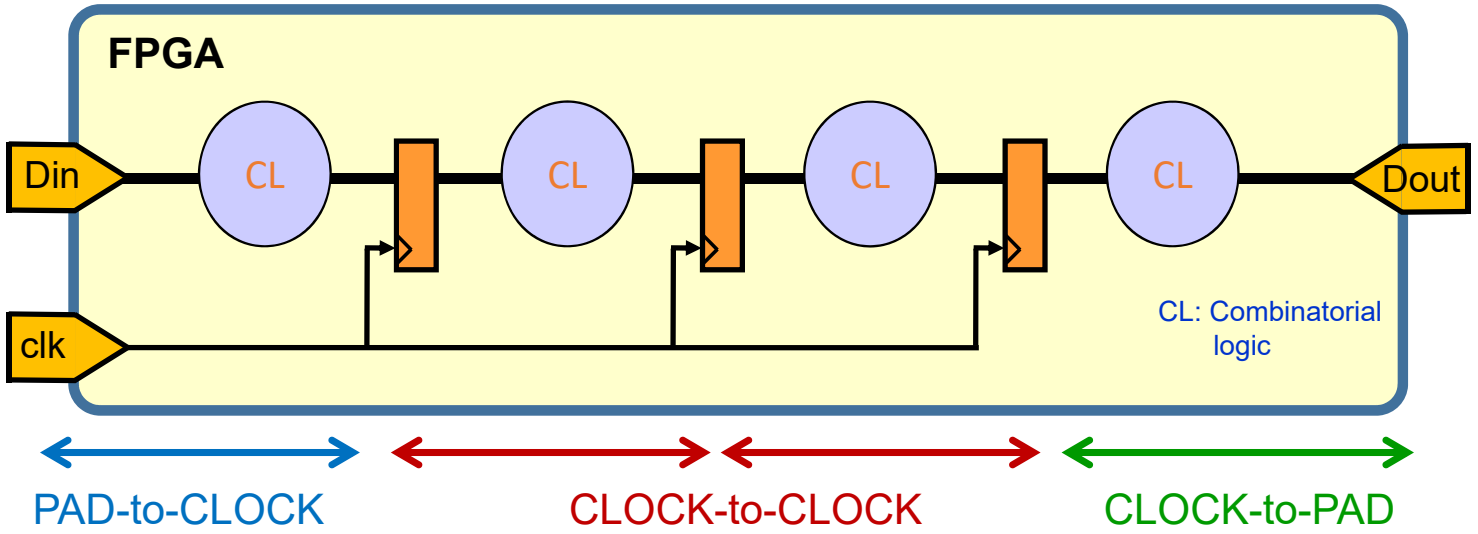


Quatus II provides the TimeQuest tool to analyze the timing of the circuit



A constrain file file_name.sdc has to be added including the timing constrains

SDC timing constrains




```
set_time_format -unit ns
create_clock -name clock_m -period 20 [get_ports {clk}]

set_input_delay -clock { clock_m } -max 3 [get_ports {Din}]
set_input_delay -clock { clock_m } -min 2 [get_ports {Din}]

set_output_delay -clock { clock_m } -max 3 [get_ports {Dout}]
set_output_delay -clock { clock_m } -min 2 [get_ports {Dout}]
```

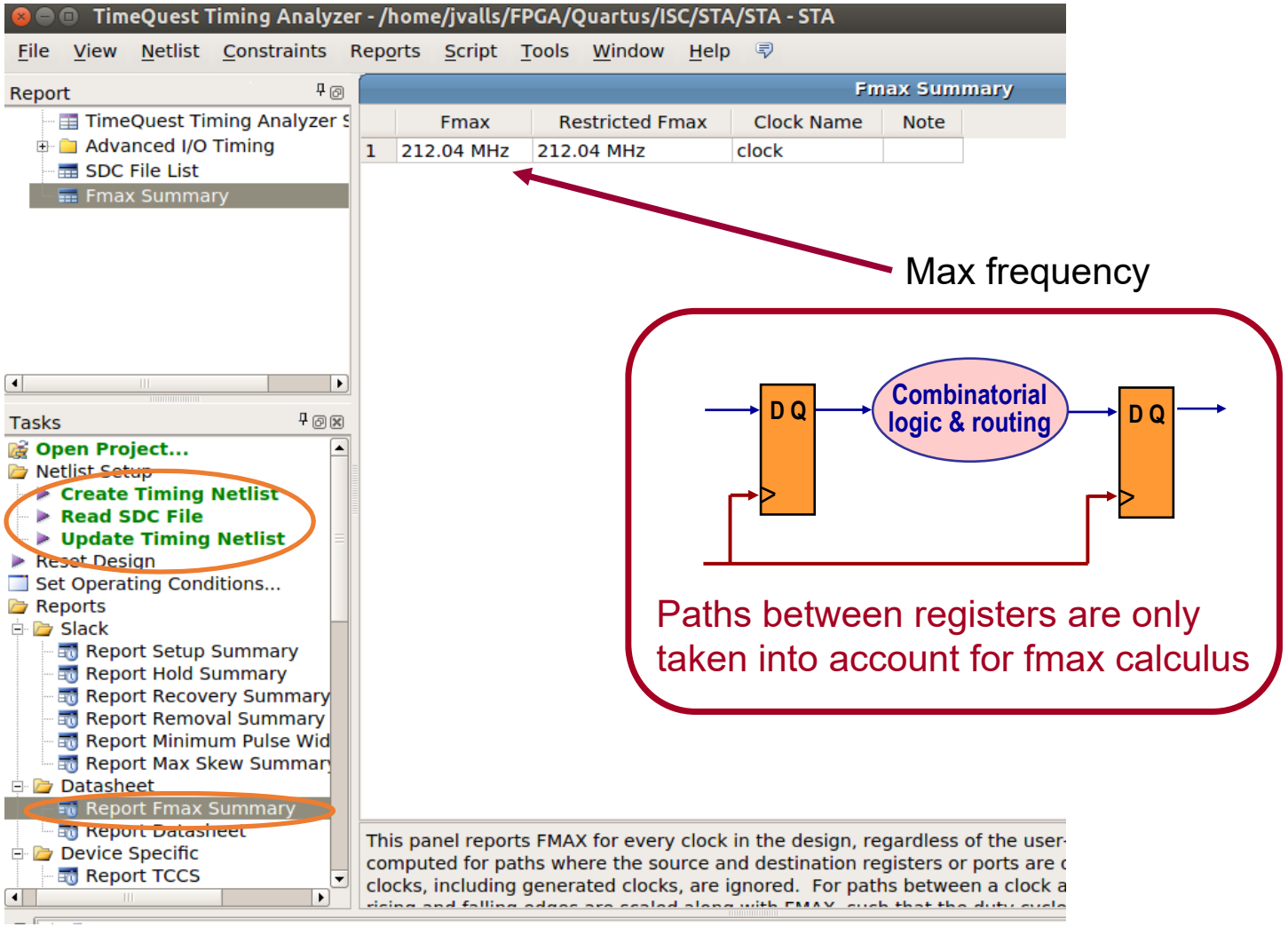
file.sdc

Specify the clock period

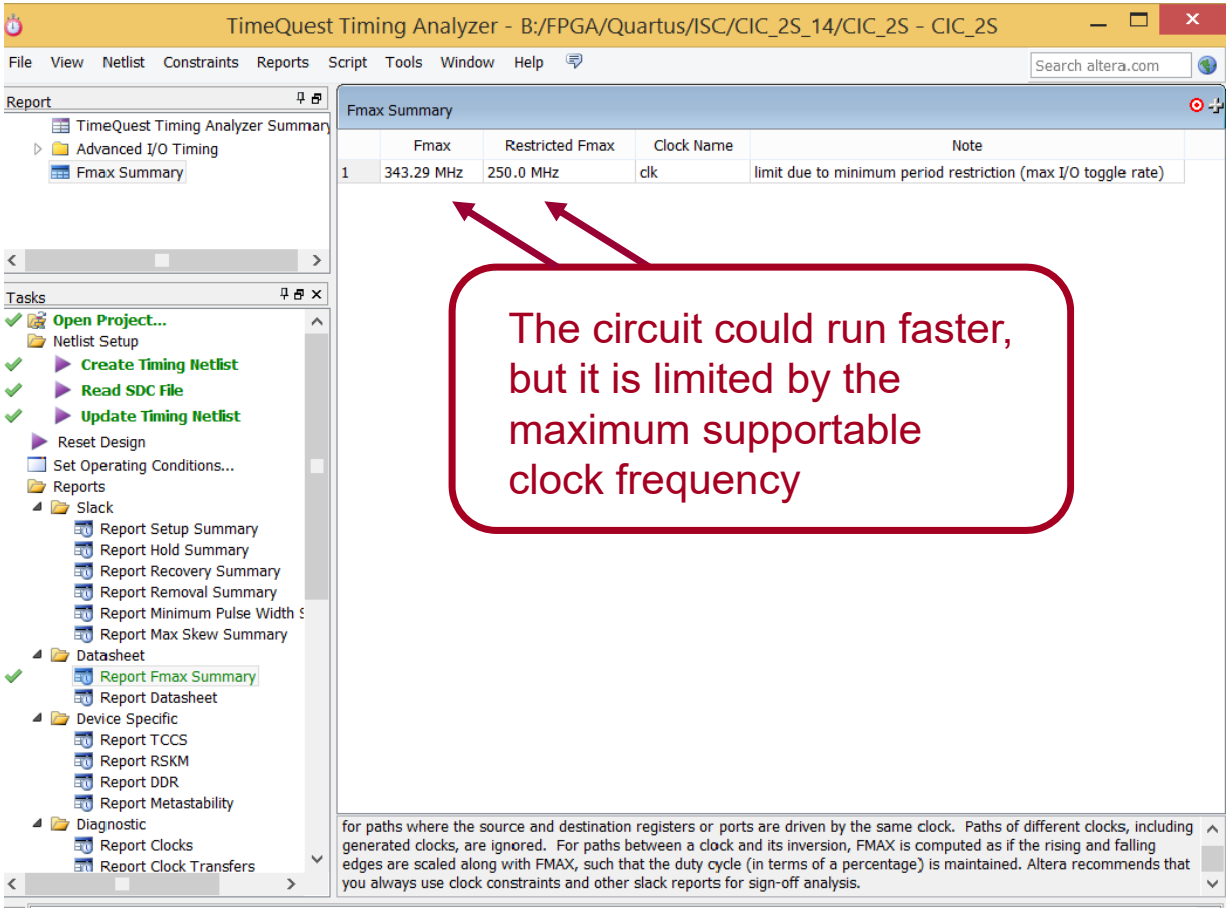
Specify external delay feeding into the FPGA input

Specify the delay from the FPGA output to the external device

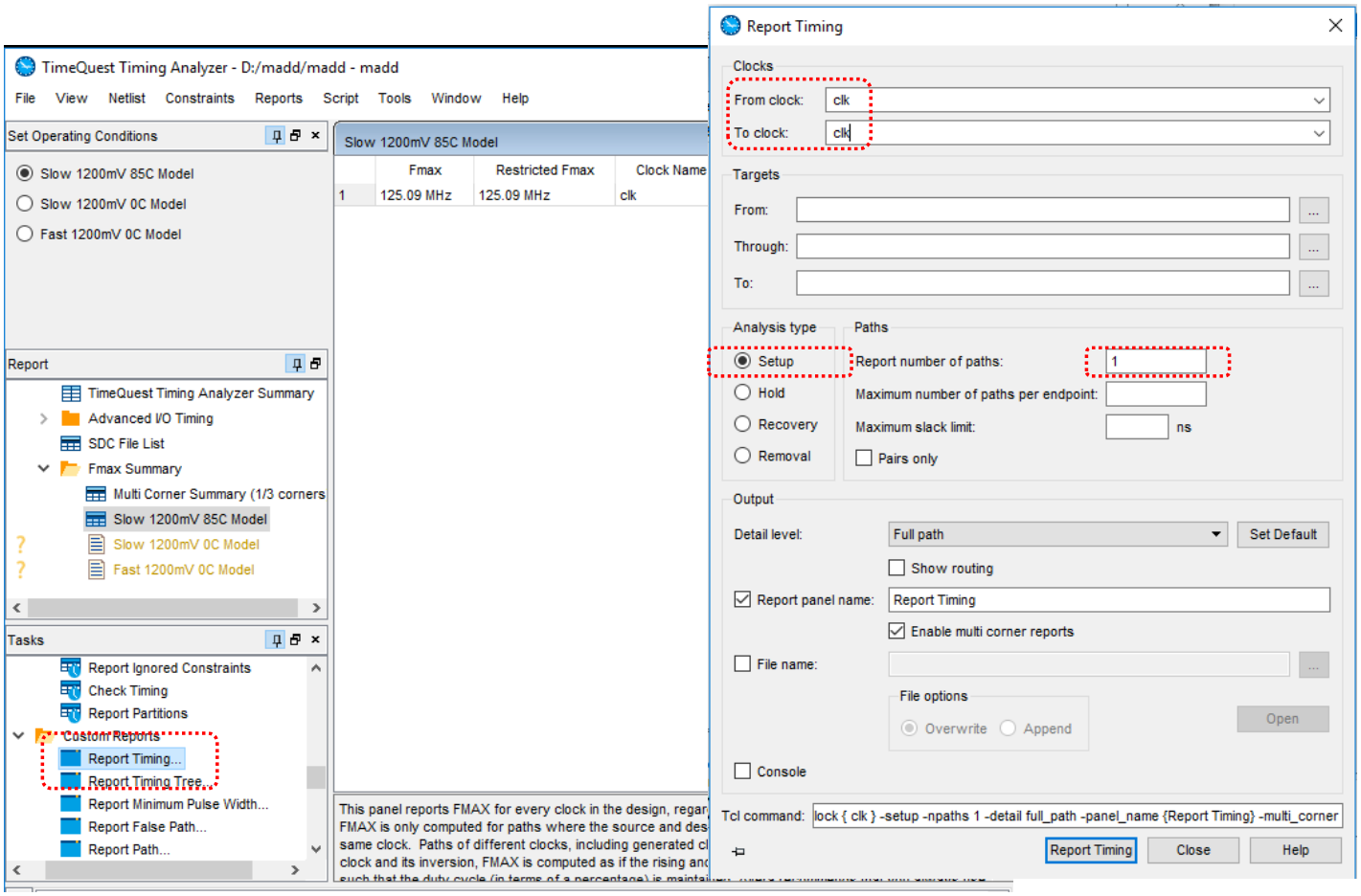
How to know if a circuit runs at fclk?



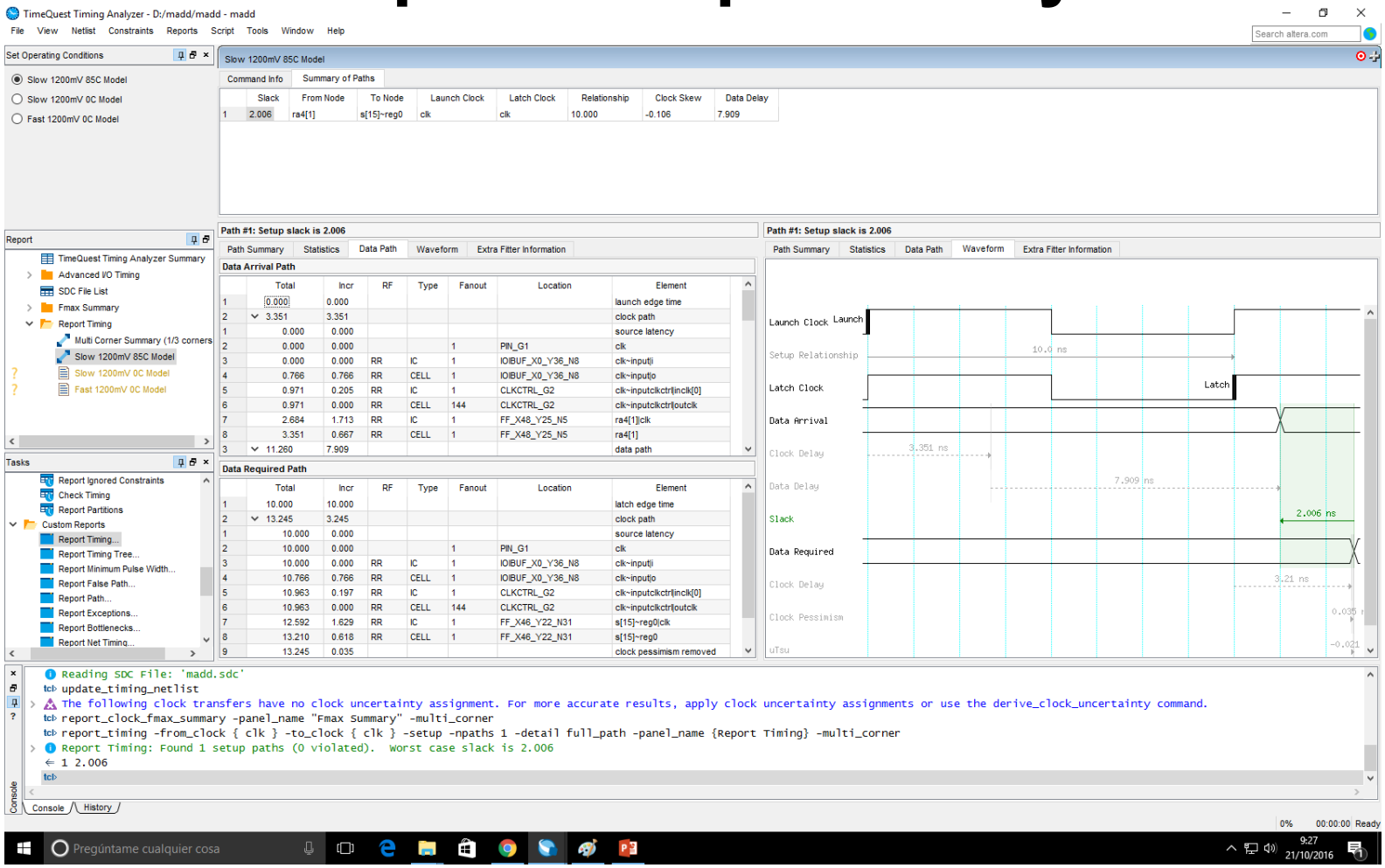
How to know if a circuit runs at fclk?



Setup critical path analysis



Setup critical path analysis



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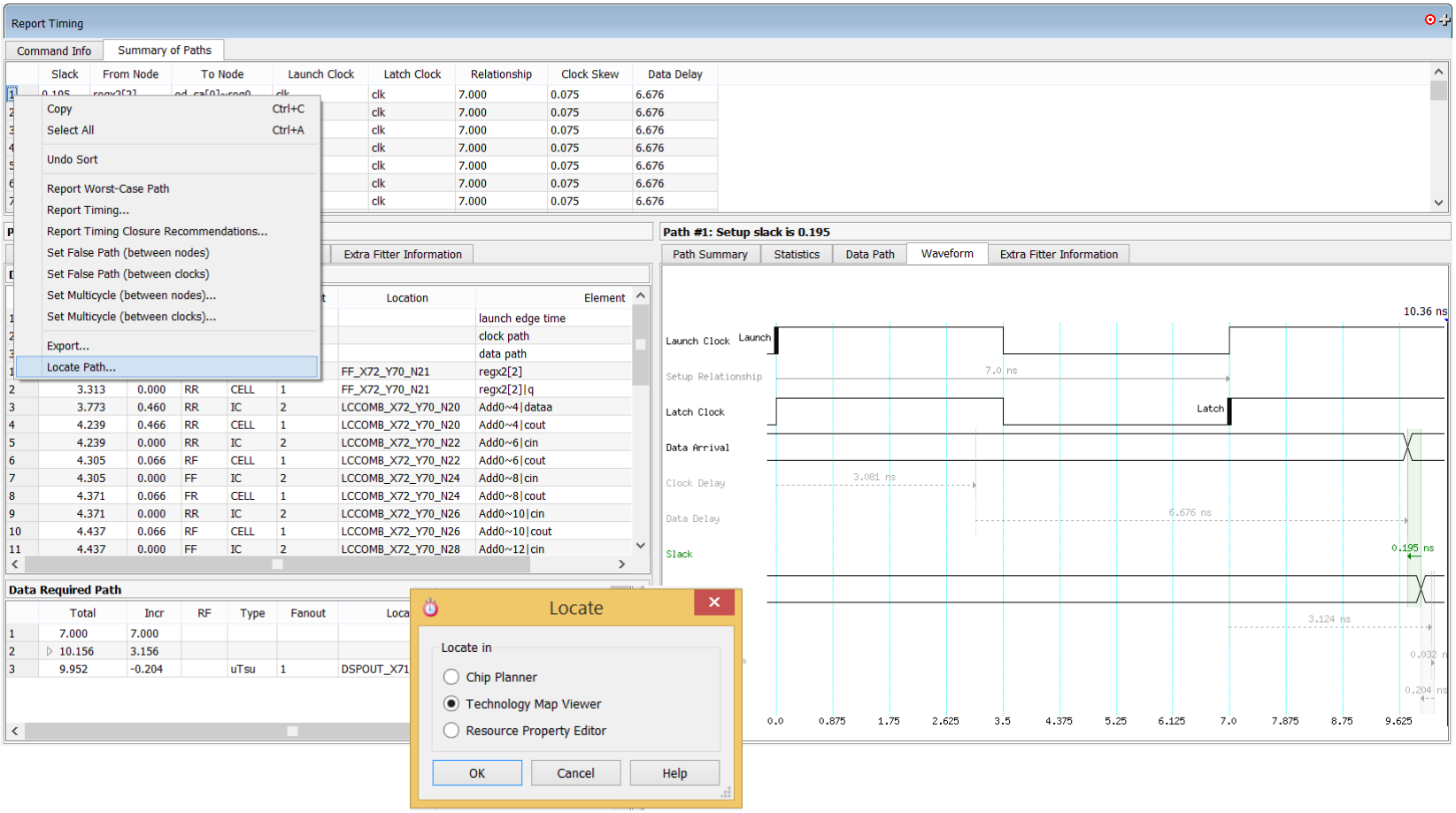
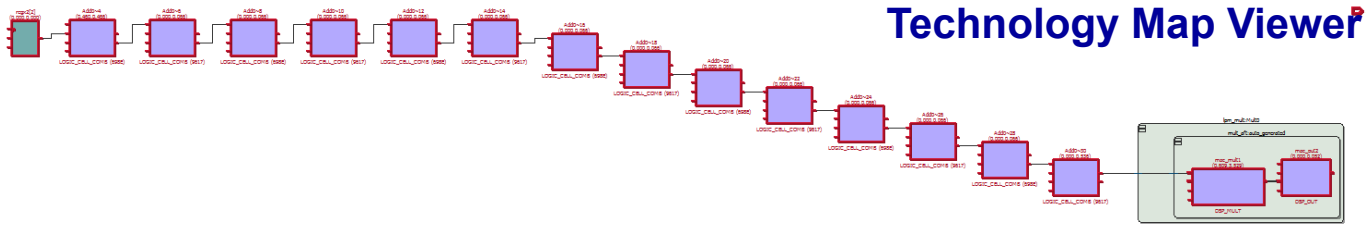
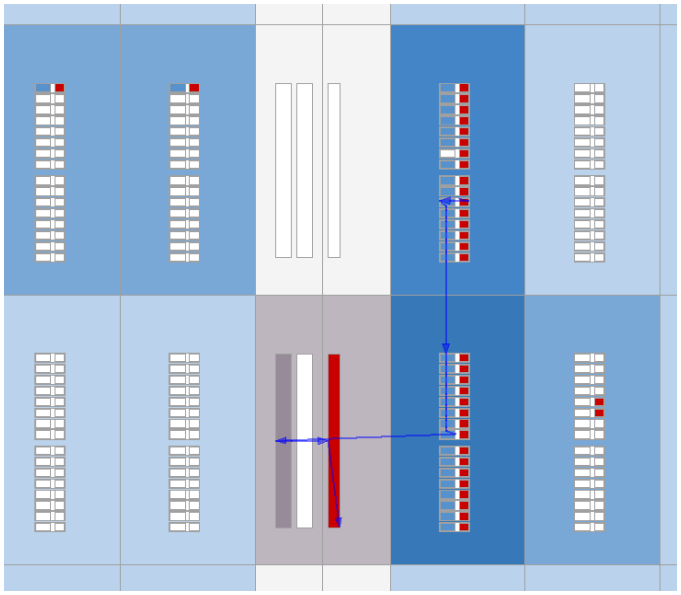


Setup critical path analysis

Technology Map Viewer



Chip Planner



Resource Property Editor