Senior Project Possible Test Plan

Quad Bilateral Switches:

ATmega328PB — PD3, PD2, PD1, PD0

296-2063-5-ND

Pins: Vcc 14, 13, 12, 11, 10, 9, 8 (top)
1, 2, 3, 4, 5, 6, 7 (bottom)

Outputs: A, B, C, D
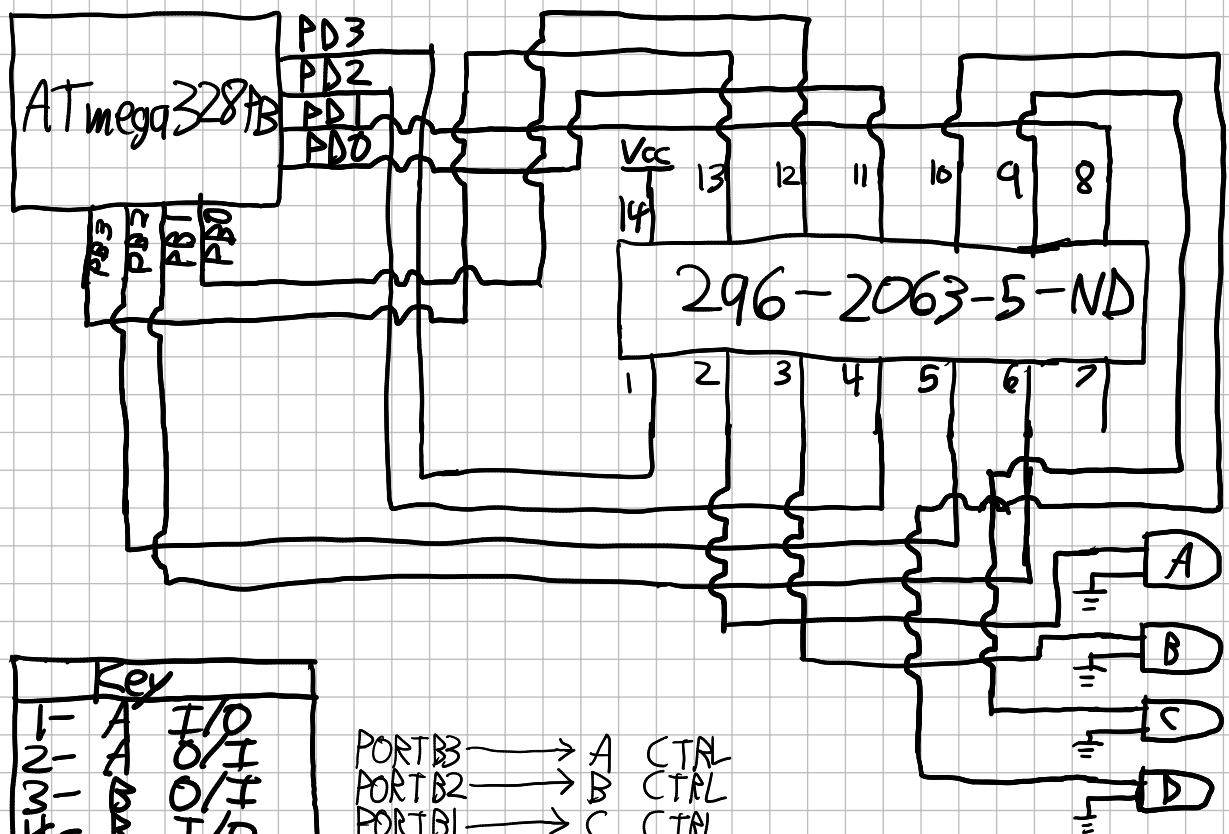
Key		
1 —	A	I/O
2 —	A	O/I
3 —	B	O/I
4 —	B	I/O
5 —	B	CTRL
6 —	C	CTRL
7 —	Vss	
8 —	C	I/O
9 —	C	O/I
10 —	D	O/I
11 —	D	I/O
12 —	D	CTRL
13 —	A	CTRL
14 —	VDD	

# of Parts: 10

PORTB3 ⟶ A CTRL
PORTB2 ⟶ B CTRL
PORTB1 ⟶ C CTRL
PORTD0 ⟶ D CTRL
PORTD3 ⟶ A I/O
PORTD2 ⟶ B I/O
PORTD1 ⟶ C I/O
PORTD0 ⟶ D I/O

Test Plans:

Power Source Setups:

— V_{CC} ⟶ V_{DD}
— fixed 3.7V ⟶ V_{DD}
— fixed 3.3V ⟶ V_{DD}

11/13/19

Analog 1V-10V −47±3dB Microphone

FET

ECM C_1 C_2

Terminal 1

C

R_L

Output

+ V_S

GND

Terminal 2

C

R

V_S

Multimeter

+ −
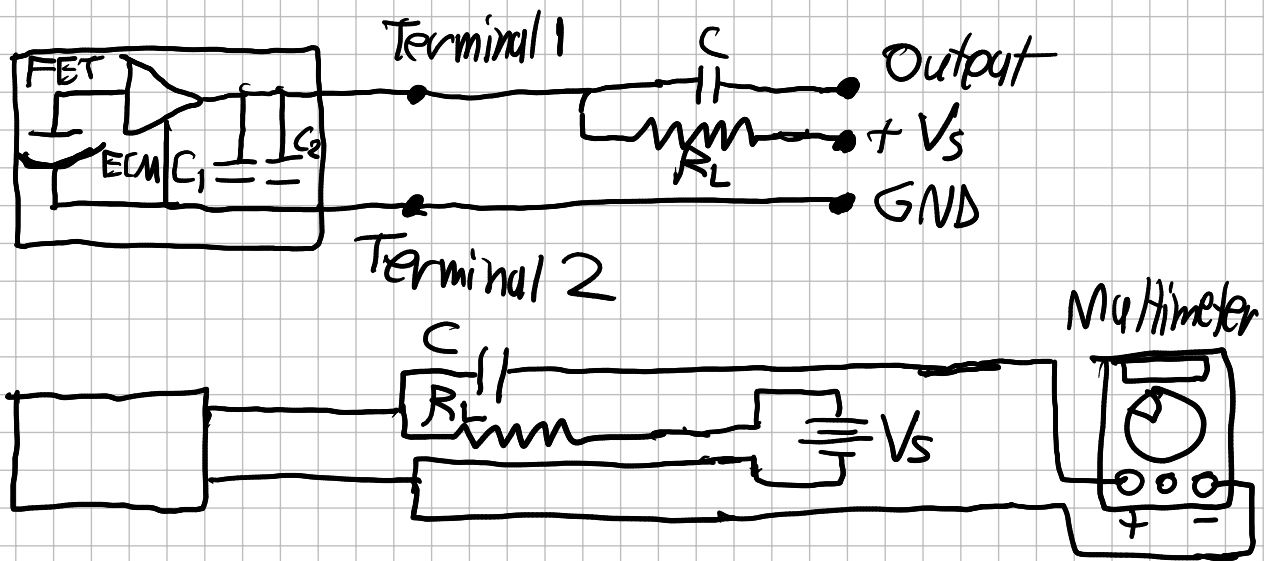
$C_1 = 10\ pF$ $C_2 = 33\ pF$ $R_L = 2.2\ k\Omega$

$C = ???$

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