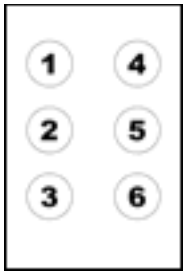
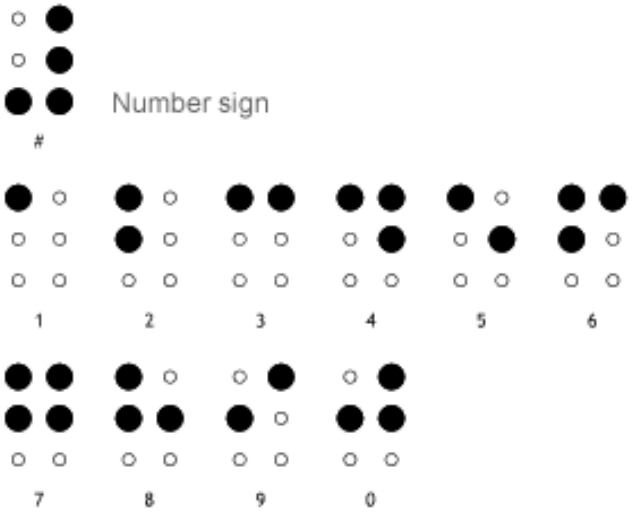
ECE 171
Fall 2014
Project 1

The basic grid of a Braille alphabet character consists of six dots, positioned like the figure six on a die, in two parallel vertical lines of three dots each. The dots can be selectively raised so that a blind person can read by sensing the bumps with his/her fingertips.



All countries (except France) represent numbers using the same Braille characters as the letter symbols A to J but prefaced with the number sign character.



Design a circuit that converts a BCD digit to a Braille symbol. Your circuit should generate the six Braille dots using B1 through B6. A 1 indicates the dot is raised (solid black in the diagrams above).

Your circuit should use SOP form. Be sure to show truth tables, K-maps, and reduced equations. Describe your circuit using a Verilog behavioral dataflow description and simulate it by writing a testbench. Assume the device has a propagation delay of 10 time units.

You can compile and simulate your Verilog program using the Verilogger software system or any other Verilog environment. Save and print the simulator timing diagram so that you can include it in your final report.

After you get your behavioral dataflow model working and verified, create a Verilog structural description for the same design and verify it. You may use any of the actual logic gates in the 74HCT family. Be sure to model your design using actual 74HCT family propagation delay values for the devices you chose. This means specifically that your Verilog program must assign t_{PLH} and t_{PHL} values to every gate. You can get these from the 74HCT data sheets, which can be found on the Texas Instruments web site (www.ti.com) – click on "Logic" under Find Products. Some are also available via links on the course page. You do not need to use SOP form for the structural description, but if the logic you implement for the structural description differs from the equations you obtained for the dataflow model, you need to show how you derived them.

Note that this means that your total propagation delay will be determined by actual devices and will differ from the dataflow design you did. You can use the same testbench that you used to verify your dataflow description (though you may need to change the timing).

This final report must include

1. A brief problem description
    a. The problem your circuit solves
    b. Specific requirements
2. The project deliverables (exactly what you are generating)
3. Approach/methodology (the steps you will take to solve the problem)
4. Your design work ("black box" diagram, truth table, K-map, reduced equations)
5. Verilog source code listings (for both designs and the testbench)
6. The timing diagram showing how your design performed
7. A schematic with reference designators and bill of materials
8. A statement indicating the worst-case propagation delay of your circuit (indicating the input and output and delay).

While your schematic may be hand-drawn, you will receive 5 points extra credit if you use a schematics capture package to produce it. See the Resources page on the class web site for several alternatives.

Your report must be typed, stapled and submitted on 8.5 x 11 inch paper. Do not use any kind of report cover. K-maps can be hand-drawn.