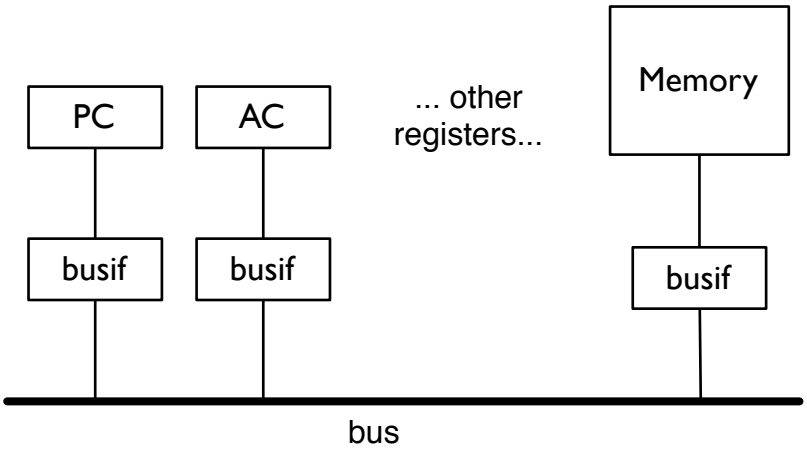
Homework 5

Building the MARIE Architecture: Part 1

Due Date: 11:59 p.m., Tuesday, March 8th

For this homework, you will build a *bus interface*, or "busif." This is a chip that you will use in future homeworks to connect the various components of the MARIE archtecture to the bus. The basic idea looks like this:



The bus interface is how each component in the MARIE architecture "talks" to the bus.

Interface and Behavior

The `busif` chip has the following inputs and outputs:

- A 16-bit connection to the bus. Because Logisim doesn't support bi-directional pins, our bus interface part will have an input and an ouput.
- A 3-bit ID input. This will be hard-wired to a number which identifies the component in bus transactions.
- A 3-bit write control input. When this matches the ID, the bus interface should place the component's data on the bus.
- A 3-bit read control input. When this matches the ID, the bus interface asserts a read output to the component.
- A single-bit read output controled by the read control just described.
- 16-bit read and write connections for the component.

Steps

Take advantage of the built-in parts in Logisim!

1. Take the `part_1.circ` file from the shared drive.
2. Make sure you put your name at the top of the circuit.
3. Implement the bus interface logic in the `busif` subcircuit.
4. Test it, to make sure that you can transfer values between registers based on their bus ID.
5. Copy your circuit to a new folder named *Homework 05* in your turn-in directory.