Name:

Lab 1 Checkoff Sheet

Be prepared to show relevant measurements and diagrams as requested in each problem. You may get checked off per problem, rather than the whole lab at once, but you don't have get checked off before proceeding to the next exercise. Collect signoff initials for each problem on this sheet and when completed, have staff enter your online grade.

Exercise 1. _____

Exercise 2. _____

Exercise 3. _____

Exercise 4. _____

Exercise 5. _____

Exercise 6. _____

Lab 1: Report Template

This report template is useful to prepare for each exercise's checkoff. Fill in answers for the questions requested by exercise; you may use a different sheet of paper if more convenient, but be sure to follow the template. Be sure to prepare relevant diagrams as requested by each problem.

Exercise 1: TTL/CMOS Static Electrical Characteristics

Low Voltage Measurement (In = 1) for 74LS00:

High Voltage Measurement (In = 0) for 74LS00:

Low Voltage Measurement (In = 1) for 74HC00:

High Voltage Measurement (In = 0) for 74HC00:

For each of these measurements, does the output satisfy the ranges specified in the appropriate datasheets? Explain.

What problems could arise from using the LS series with the HC series (at +5V supply)?

Exercise 2: Build your own ring oscillator

Please draw out the waveform showing the output for the 5-inverter oscillator ring. Be sure to label the maximum and minimum voltages, and label the appropriate time intervals.

What is the average TTL inverter propagation delay? Show calculations and briefly explain.

Estimate the period of oscillation for a 3 inverter ring, rather than 5? Explain. What was your measured result?

What happens if you add a long piece of wire to the 3 inverter ring? Explain what causes this to happen.

What is the voltage measurement when you connect the output to the input of a single inverter? What is the significance of this voltage?

Exercise 3: Glitches

What is the length of the glitch measured in this exercise?

Why does this glitch occur, and what is the lesson learned from this exercise?

Under what conditions is it a bad idea to use a glitchy signal as an input?

Exercise 4: Asynchronous Counters

Please draw a high level diagram showing the flip-flop arrangement of a typical asynchronous counter, emphasizing the source of each clk input for each flip-flop.

What is your measurement for the clk to MSB delay? From this measurement, show calculations for the clk-to-q delay for a typical flip-flop in the LS393, and explain the derivation.

Exercise 5: Synchronous Counter

Draw a high level diagram showing the flip-flop arrangement of a typical synchronous counter, emphasizing the source of each clk input for each flip-flop.

Explain how the RCO signal of the low-order counter is used to control the high-order counter.

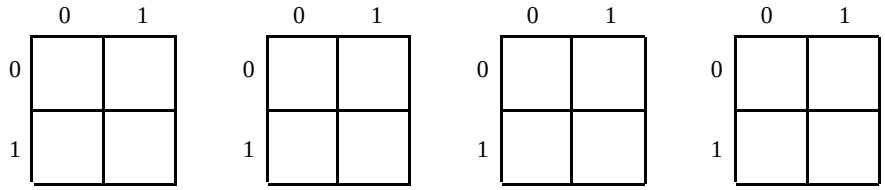
How long does it take, after the rising edge of the clock, for the A output to change state? For the B output to change state? Explain why they are the same/different.

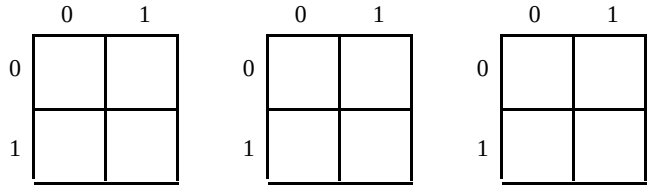
Show your logic analyzer trace of the A, B, C, D and RCO outputs to the TA. Can you observe any glitches on RCO? Explain under what circumstance you might expect RCO glitches to occur.

Explain some differences between the 74LS163 and the 74LS393 in terms of design and performance. How many flip-flops and how much logic is required to implement the counter?

Exercise 6: Designing Combinational Logic

Draw out the 7 Karnaugh maps corresponding to the different outputs, and circle the implicants that generate the Minimal Sum of Products equation. Write down the MSOP equations below each Karnaugh map. Be sure to label each Karnaugh map with the name of the appropriate segment.





Using only inverters (74LS04) and 2-input NAND gates (74LS00), draw a schematic that implements the equations above. Add pin numbers to your diagram and then implement it on your protoboard. What's the propagation delay of your circuit?