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525.742.8VL System-on-a-Chip FPGA Design Laboratory

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Lab 1B: VHDL/Synchronous Design Refresher

**Questions**

1. *Question 1: Which of the signals in your dac interface component need to be routed to the codec? What FPGA pin should each of those signals be assigned to in your constraints file in order to accomplish this?*
   1. The sdata, lrck, bclk, and mclk all must be routed from the dac interface component to the codec. This is described in the SSM2603 datasheet on page 15,
      1. “On the PBDAT input pin, the digital audio interface can receive digital audio data for playback mode operation. The digital audio data stream on PBDAT comprises left- and right-channel audio data that is time domain multiplexed. The PBLRC is the digital audio frame clock signal that separates left- and right-channel data on the PBDAT lines. The BCLK signal acts as the digital audio clock. Depending on whether the SSM2603 is in master or slave mode, the BCLK signal is either an input or an output signal. During a playback operation, PBDAT and PBLRC must be synchronous to the BCLK signal to avoid data corruption.”
   2. From the above, PBDAT (pin R18) is our sdata, PBLRC (pin T19) is our lrck, BCLK (pin R19) is bclk, and MCLK (master clock, pin R17) is mclk.
2. *Question 2: Assume you have an I2C interface to write to the CODEC configuration registers (we’ll get to that next week). What values (in binary “0b…” or hex “0x…”) should we put in R4 and R5 in order to enable digital samples coming from your component to be converted to analog by the Digital to Analog Converter (DAC) and played over the line out port of your board? How do these values compare to the register defaults? Note there are other registers we will need to configure before this will work, but we’re only asking you to set R4 and R5.* 
   1. Given the register map for R4 and R5, we want to set R4 = 000011010, that is changing the default so that the DACSEL bit is high and we use the DAC. The SIDETONE\_ATT and SIDETONE\_EN can remain low, the ADC can be left unused (INSEL and Bypass low), the mic can remain muted (MUTEMIC and MICBOOST low). R5 can be changed from the default 0000001000 to 000000110 so that DACMU is set low and the DAC is no longer muted. By changing bits 1 and 2, the user implements digital de-emphasis and selects a 48 kHz sampling rate.